
# NHUMD3/2/12 series

## 80 V, 100 mA NPN/PNP resistor-equipped double transistors

Rev. 1 — 24 July 2020 Product data sheet

## 1. General description

NPN/PNP Resistor-Equipped double Transistor (RET) family in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

**Table 1. Product overview**

| Type number | R1 | R2 | Package | | NPN/NPN complement: | PNP/PNP complement: |
|---|---|---|---|---|---|---|
| | kΩ | kΩ | Nexperia | JEITA | | |
| NHUMD3 | 10 | 10 | SOT363 | SC-88 | NHUMH11 | NHUMB11 |
| NHUMD2 | 22 | 22 | | | NHUMH1 | NHUMB1 |
| NHUMD12 | 47 | 47 | | | NHUMH2 | NHUMB2 |

## 2. Features and benefits

- 100 mA output current capability
- High breakdown voltage
- Built-in resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

## 3. Applications

- Digital applications
- Cost saving alternative for BC846 / BC856 series in digital applications
- Controlling IC inputs
- Switching loads

## 4. Quick reference data

**Table 2. Quick reference data**

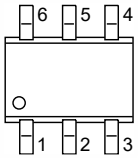
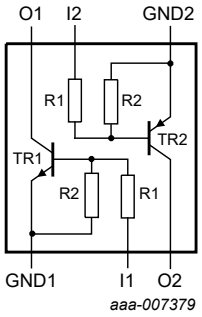
*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Per transistor, for the PNP transistor with negative polarity** | | | | | | |
| $V_{CEO}$ | collector-emitter voltage | open base | - | - | 80 | V |
| $I_O$ | output current | | - | - | 100 | mA |

nexperia

## 5. Pinning information

**Table 3. Pinning**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | GND1 | GND (emitter) TR1 |  |  |
| 2 | I1 | input (base) TR1 | | |
| 3 | O2 | output (collector) TR2 | | |
| 4 | GND2 | GND (emitter) TR2 | | |
| 5 | I2 | input (base) TR2 | | |
| 6 | O1 | output (collector) TR1 | | |



## 6. Ordering information

**Table 4. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| NHUMD3 | SC-88 | plastic surface-mounted package; 6 leads | SOT363 |
| NHUMD2 | | | |
| NHUMD12 | | | |

## 7. Marking

**Table 5. Marking**

| Type number | Marking code [1] |
|---|---|
| NHUMD3 | 6M% |
| NHUMD2 | 6Q% |
| NHUMD12 | 6S% |

[1] % = placeholder for manufacturing site code

# 8. Limiting values

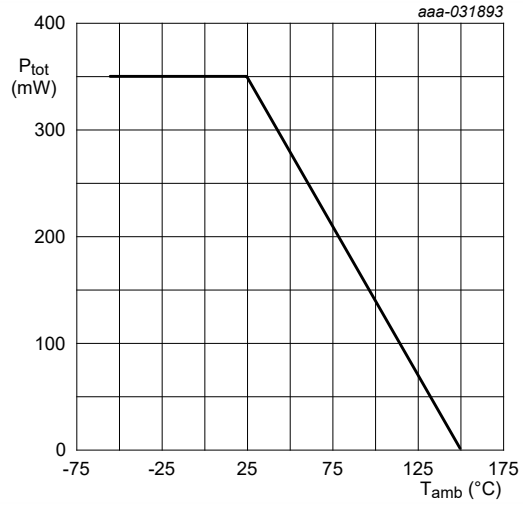
**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Per transistor, for the PNP transistor with negative polarity** | | | | | | |
| $V_{CBO}$ | collector-base voltage | open emitter | | - | 80 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | | - | 80 | V |
| $V_{EBO}$ | emitter-base voltage | open collector | | - | 10 | V |
| $V_I$ | input voltage | | | | | |
| | NHUMD3, TR1 (NPN) | | | -10 | +40 | V |
| | NHUMD3, TR2 (PNP) | | | -40 | +10 | V |
| | NHUMD2, TR1 (NPN) | | | -10 | +60 | V |
| | NHUMD2, TR2 (PNP) | | | -60 | +10 | V |
| | NHUMD12, TR1 (NPN) | | | -10 | +80 | V |
| | NHUMD12, TR2 (PNP) | | | -80 | +10 | V |
| $I_O$ | output current | | | - | 100 | mA |
| $P_{tot}$ | total power dissipation | $T_{amb}$ ≤ 25 °C | [1] | - | 235 | mW |
| **Per device** | | | | | | |
| $P_{tot}$ | total power dissipation | $T_{amb}$ ≤ 25 °C | [1] | - | 350 | mW |
| $T_j$ | junction temperature | | | - | 150 | °C |
| $T_{amb}$ | ambient temperature | | | -55 | 150 | °C |
| $T_{stg}$ | storage temperature | | | -65 | 150 | °C |

[1] Device mounted on an FR4 Printed-Circuit-Board (PCB); single-sided copper; tin-plated and standard footprint.




FR4 PCB, single-sided copper, standard footprint

**Fig. 1. Per device: Power derating curve SOT363 (SC-88)**

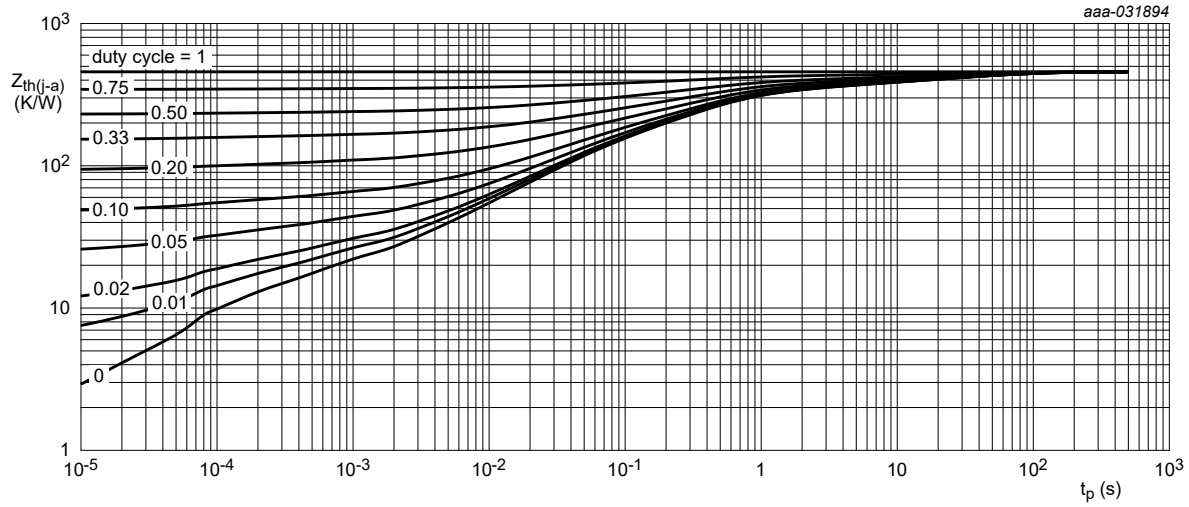
# 9. Thermal characteristics

**Table 7. Thermal characteristics**

*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Per transistor** | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 532 | K/W |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | | | - | - | 150 | K/W |
| **Per device** | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 358 | K/W |

[1] Device mounted on an FR4 Printed-Circuit-Board (PCB); single-sided copper; tin-plated and standard footprint.




FR4 PCB, single-sided copper, tin-plated and standard footprint

**Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

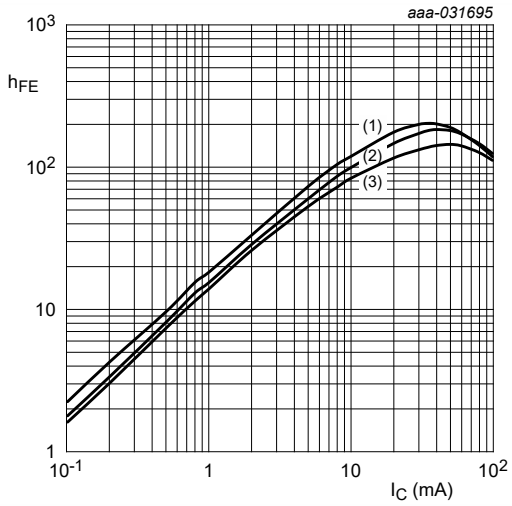
# 10. Characteristics

**Table 8. Characteristics**

*$T_{amb}$ = 25 °C unless otherwise specified.*

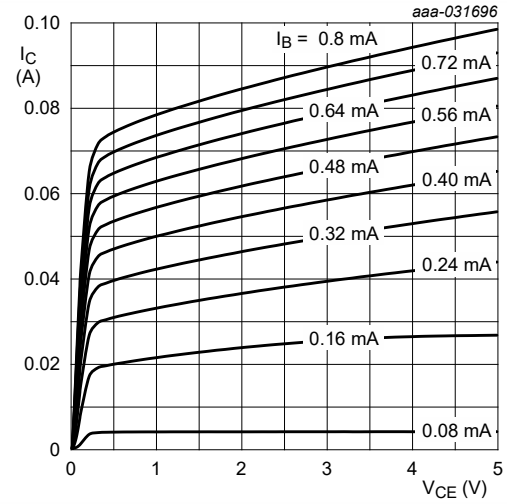
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Per transistor, for the PNP transistor with negative polarity** | | | | | | |
| $V_{(BR)CBO}$ | collector-base breakdown voltage | $I_C$ = 100 µA; $I_E$ = 0 A | 80 | - | - | V |
| $V_{(BR)CEO}$ | collector-emitter breakdown voltage | $I_C$ = 2 mA; $I_B$ = 0 A | 80 | - | - | V |
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = 80 V; $I_E$ = 0 A | - | - | 100 | nA |
| $I_{CEO}$ | collector-emitter cut-off current | $V_{CE}$ = 60 V; $I_B$ = 0 A | - | - | 100 | nA |
| | | $V_{CE}$ = 60 V; $I_B$ = 0 A; $T_j$ = 150 °C | - | - | 5 | µA |
| $I_{EBO}$ | emitter-base cut-off current | | | | | |
| | NHUMD3 | $V_{EB}$ = 7 V; $I_C$ = 0 A | - | - | 600 | µA |
| | NHUMD2 | | - | - | 270 | µA |
| | NHUMD12 | | - | - | 130 | µA |
| $h_{FE}$ | DC current gain | | | | | |
| | NHUMD3 | $V_{CE}$ = 5 V; $I_C$ = 10 mA | 50 | - | - | |
| | NHUMD2 | | 70 | - | - | |
| | NHUMD12 | | 100 | - | - | |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = 10 mA; $I_B$ = 0.5 mA | - | - | 100 | mV |
| $V_{I(off)}$ | off-state input voltage | $V_{CE}$ = 5 V ; $I_C$ = 100 µA | - | 1.15 | 0.8 | V |
| $V_{I(on)}$ | on-state input voltage | | | | | |
| | NHUMD3 | $V_{CE}$ = 0.3 V ; $I_C$ = 10 mA | 2.5 | 1.8 | - | V |
| | NHUMD2 | | 3 | 2.3 | - | V |
| | NHUMD12 | | 5 | 3.3 | - | V |
| R1 | bias resistor 1 (input) [1] | | | | | |
| | NHUMD3 | | 7 | 10 | 13 | kΩ |
| | NHUMD2 | | 15.4 | 22 | 28.6 | kΩ |
| | NHUMD12 | | 33 | 47 | 61 | kΩ |
| R2/R1 | bias resistor ratio [1] | | 0.8 | 1 | 1.2 | |
| $f_T$ | transition frequency | $V_{CE}$ = 5 V; $I_C$ = 10 mA; f = 100 MHz [2] | | | | |
| | TR1 (NPN) | | - | 170 | - | |
| | TR2 (PNP) | | - | 150 | - | |
| $C_c$ | collector capacitance | $V_{CB}$ = 10 V; $I_E$ = $i_e$ = 0 A; f = 1 MHz | | | | |
| | TR1 (NPN) | | - | - | 2.5 | pF |
| | TR2 (PNP) | | - | - | 3 | pF |

[1] See section "Test information" for resistor calculation and test conditions
[2] Characteristics of built-in transistor



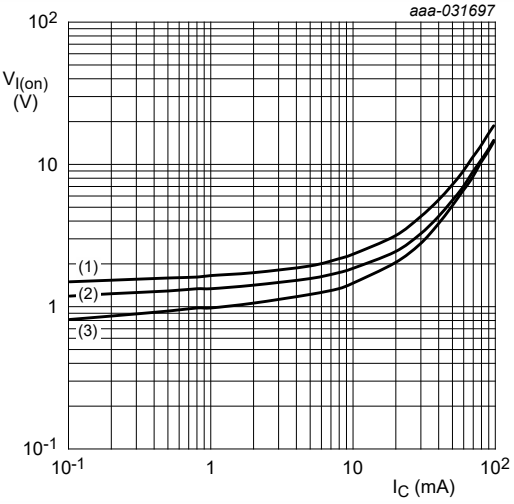

$V_{CE}$ = 5 V
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 3. NHUMD3, TR1 (NPN): DC current gain as a function of collector current; typical values**



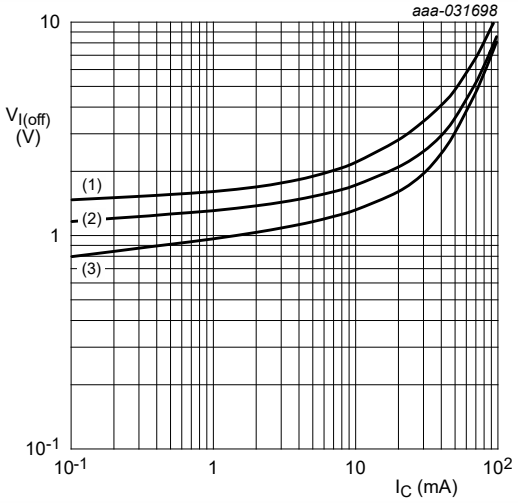

$T_{amb}$ = 25 °C

**Fig. 4. NHUMD3, TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values**



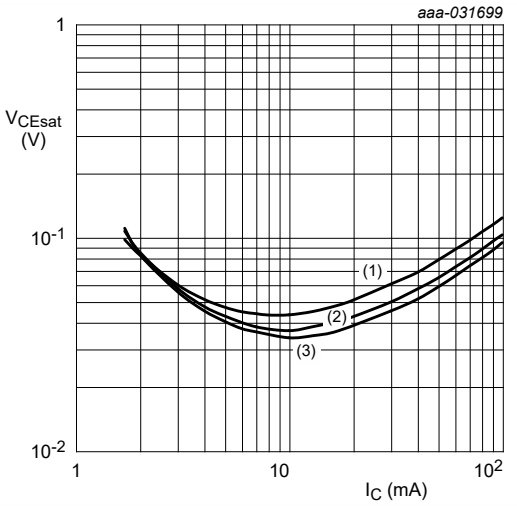

$V_{CE}$ = 0.3 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 5. NHUMD3, TR1 (NPN): On-state input voltage as a function of collector current; typical values**



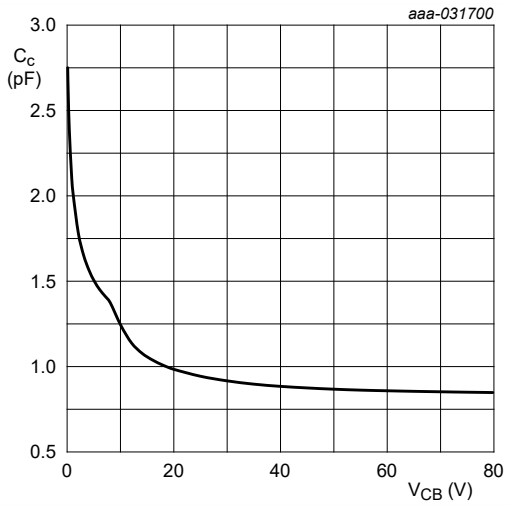

$V_{CE}$ = 5 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 6. NHUMD3, TR1 (NPN): Off-state input voltage as a function of collector current; typical values**



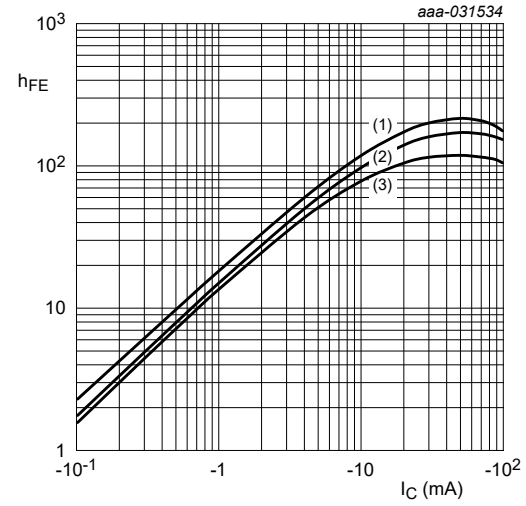

$I_C/I_B$ = 20
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 7. NHUMD3, TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



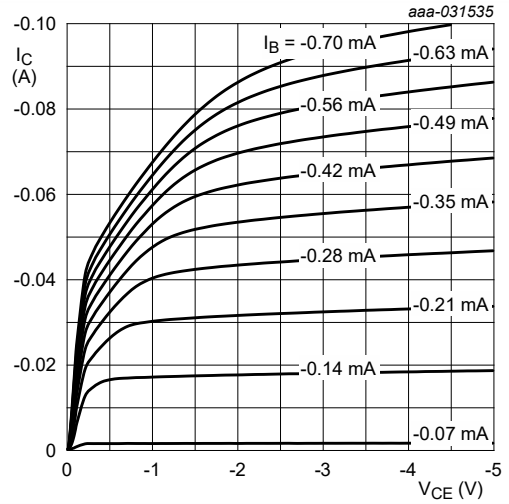

f = 1 MHz
$T_{amb}$ = 25 °C

**Fig. 8. NHUMD3, TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values**



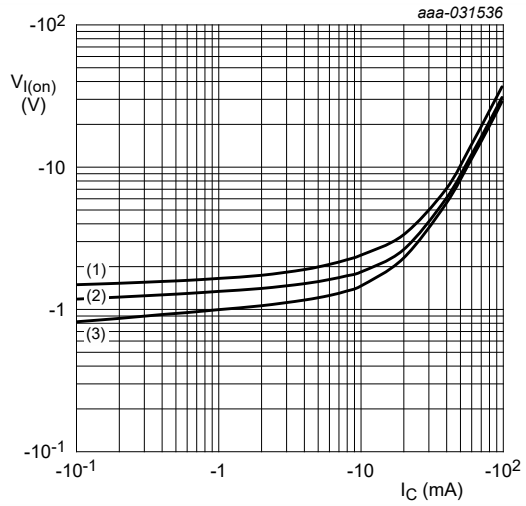

$V_{CE}$ = -5 V
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 9. NHUMD3, TR2 (PNP): DC current gain as a function of collector current; typical values**



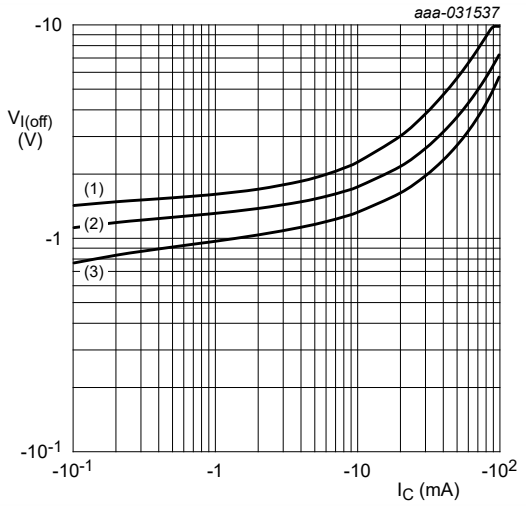

$T_{amb}$ = 25 °C

**Fig. 10. NHUMD3, TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values**



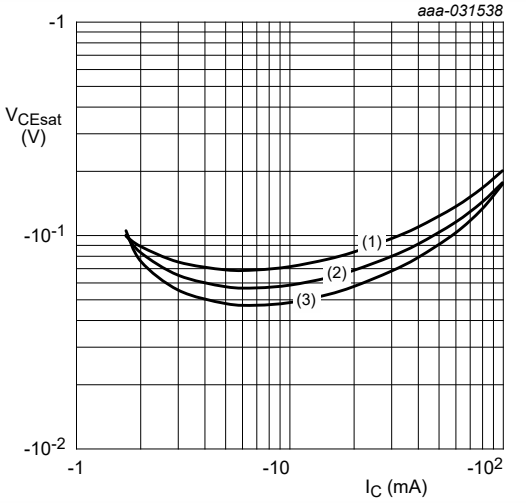

$V_{CE}$ = -0.3 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 11. NHUMD3, TR2 (PNP): On-state input voltage as a function of collector current; typical values**



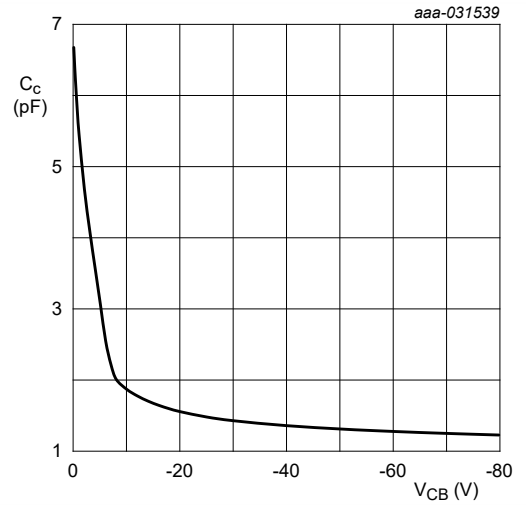

$V_{CE}$ = -5 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 12. NHUMD3, TR2 (PNP): Off-state input voltage as a function of collector current; typical values**



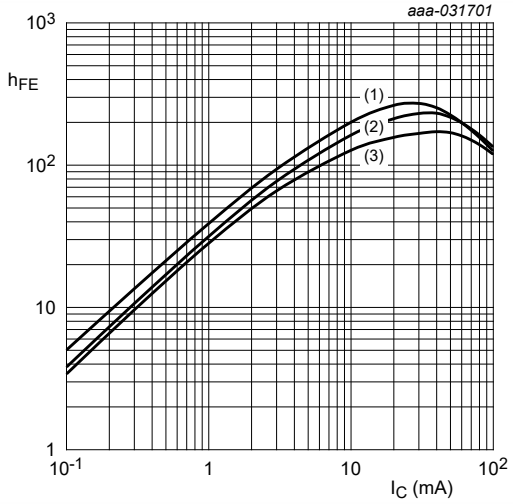

$I_C/I_B$ = 20
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 13. NHUMD3, TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



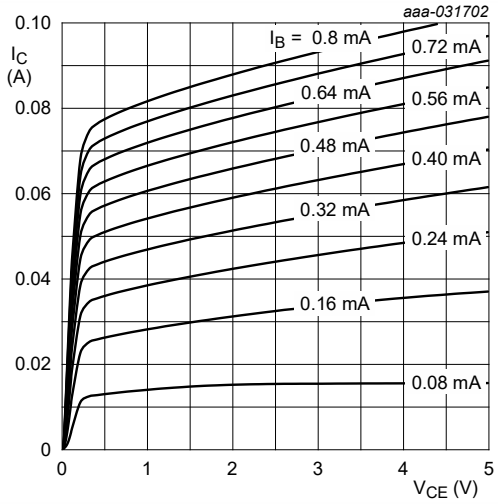

f = 1 MHz
$T_{amb}$ = 25 °C

**Fig. 14. NHUMD3, TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values**



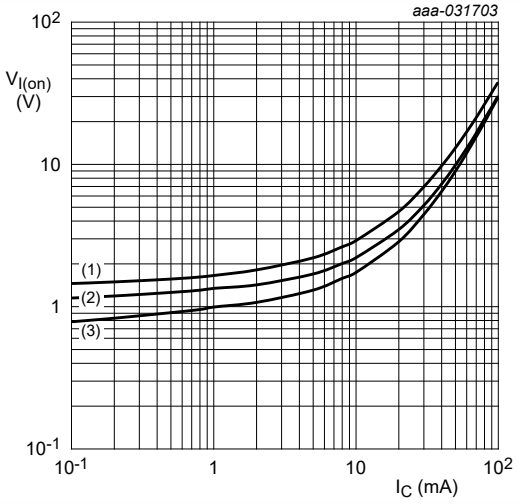

$V_{CE}$ = 5 V
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 15. NHUMD2, TR1 (NPN): DC current gain as a function of collector current; typical values**



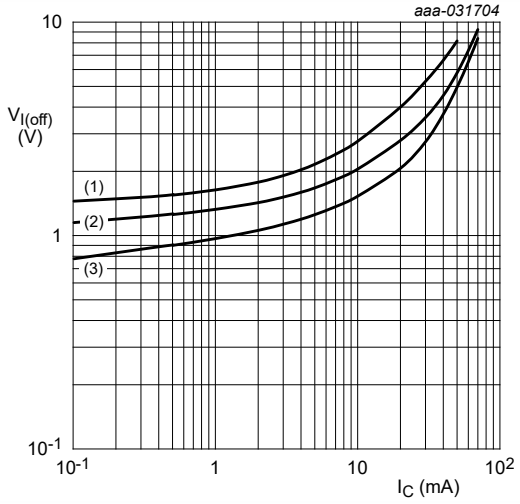

$T_{amb}$ = 25 °C

**Fig. 16. NHUMD2, TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values**



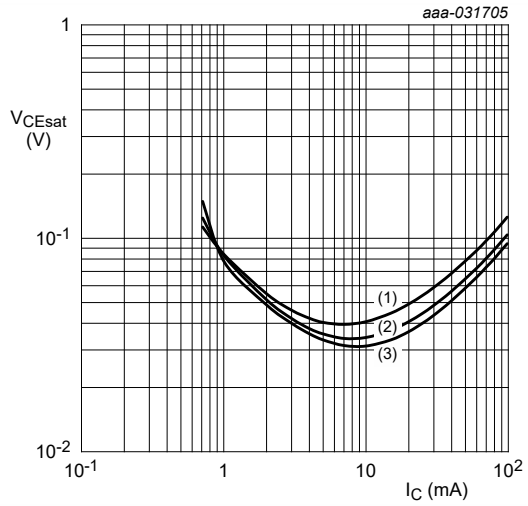

$V_{CE}$ = 0.3 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 17. NHUMD2, TR1 (NPN): On-state input voltage as a function of collector current; typical values**



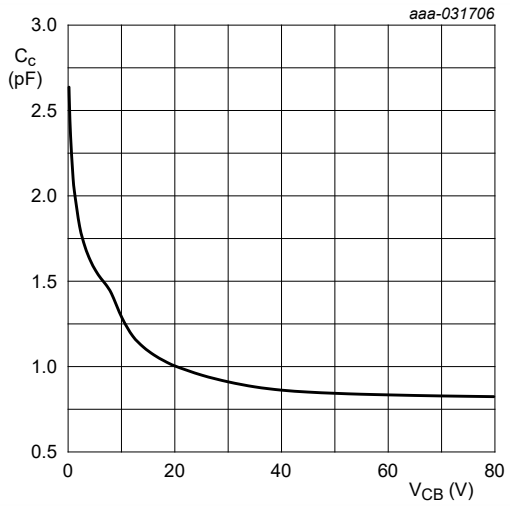

$V_{CE}$ = 5 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 18. NHUMD2, TR1 (NPN): Off-state input voltage as a function of collector current; typical values**



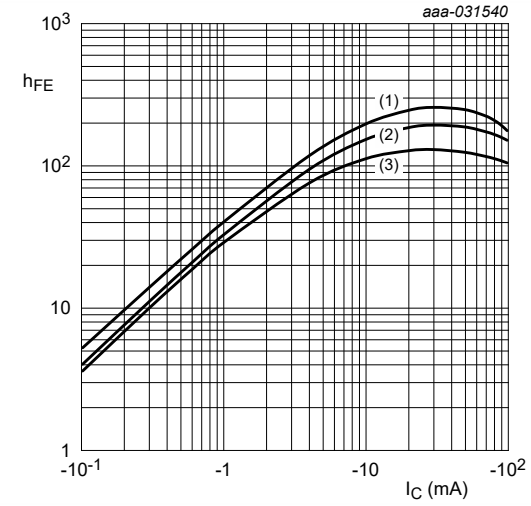

$I_C/I_B$ = 20
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 19. NHUMD2, TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



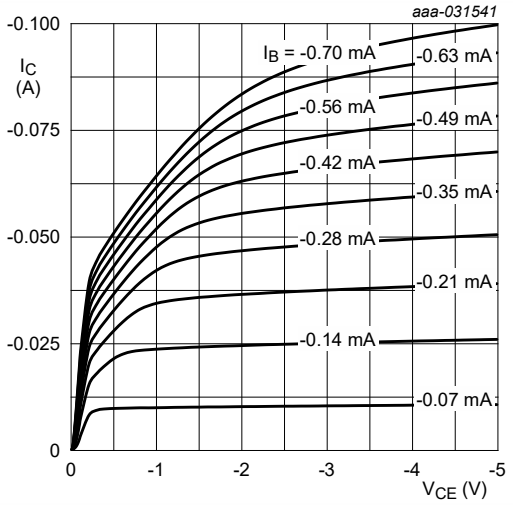

f = 1 MHz
$T_{amb}$ = 25 °C

**Fig. 20. NHUMD2, TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values**



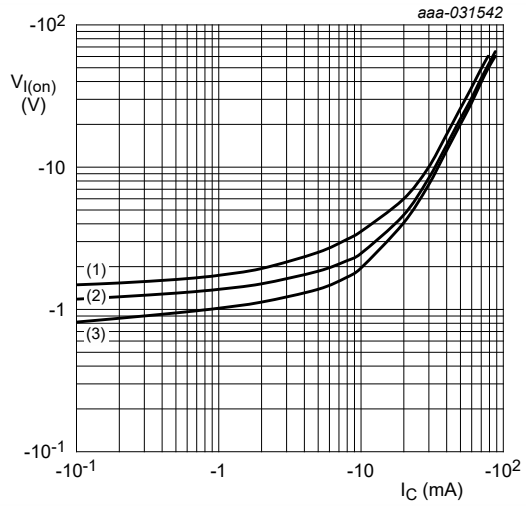

$V_{CE}$ = -5 V
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 21. NHUMD2, TR2 (PNP): DC current gain as a function of collector current; typical values**



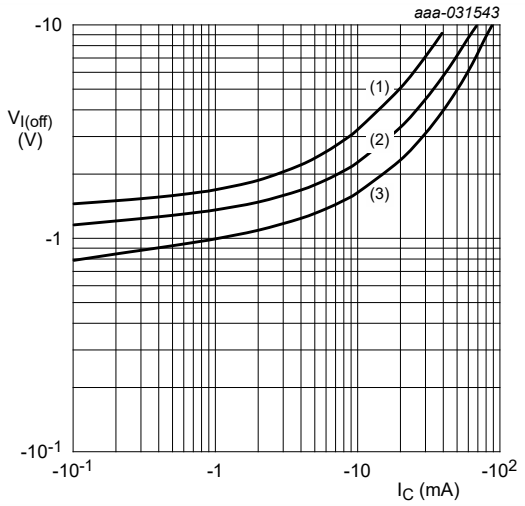

$T_{amb}$ = 25 °C

**Fig. 22. NHUMD2, TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values**



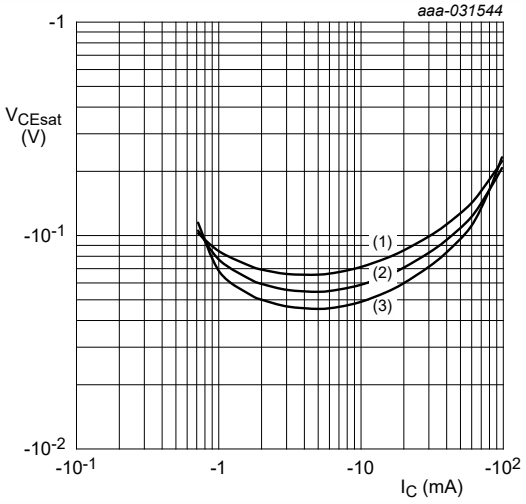

$V_{CE}$ = -0.3 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 23. NHUMD2, TR2 (PNP): On-state input voltage as a function of collector current; typical values**



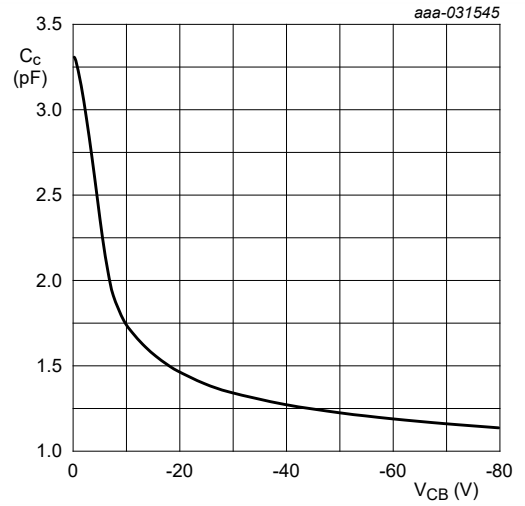

$V_{CE}$ = -5 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 24. NHUMD2, TR2 (PNP): Off-state input voltage as a function of collector current; typical values**



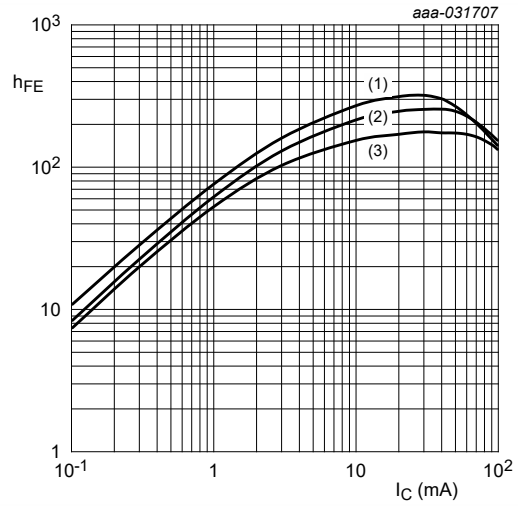

$I_C/I_B$ = 20
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 25. NHUMD2, TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



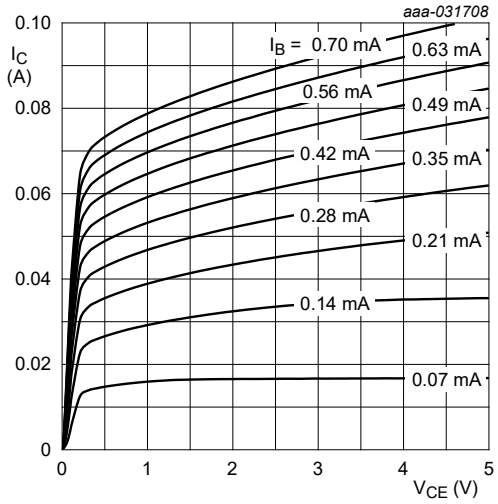

f = 1 MHz
$T_{amb}$ = 25 °C

**Fig. 26. NHUMD2, TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values**



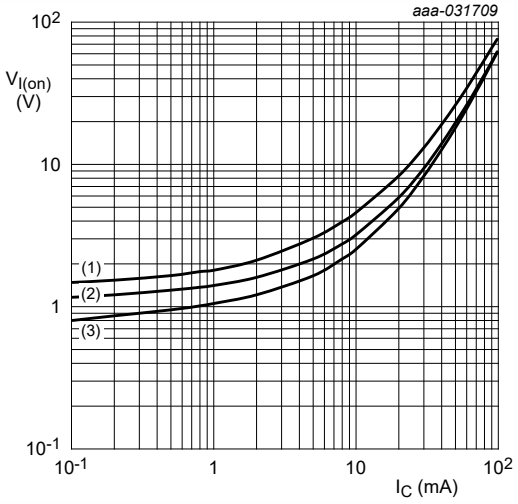

$V_{CE}$ = 5 V
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 27. NHUMD12, TR1 (NPN): DC current gain as a function of collector current; typical values**



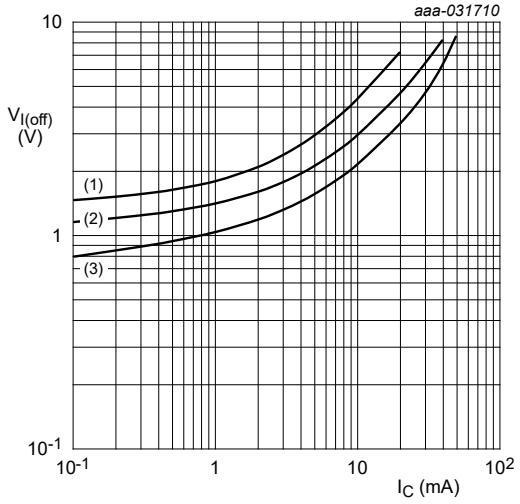

$T_{amb}$ = 25 °C

**Fig. 28. NHUMD12, TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values**



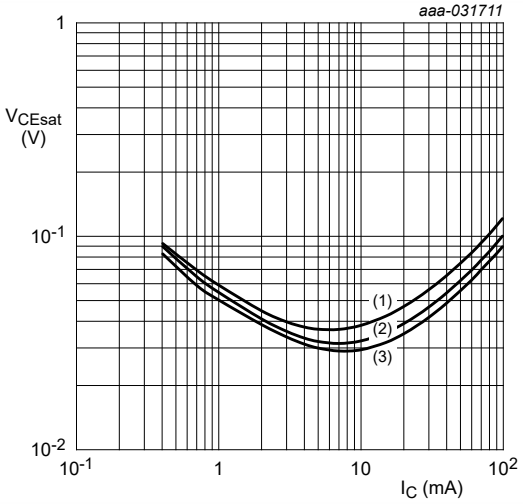

$V_{CE}$ = 0.3 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 29. NHUMD12, TR1 (NPN): On-state input voltage as a function of collector current; typical values**



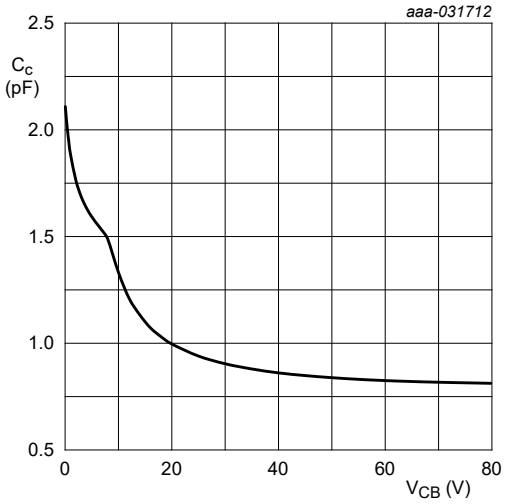

$V_{CE}$ = 5 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 30. NHUMD12, TR1 (NPN): Off-state input voltage as a function of collector current; typical values**



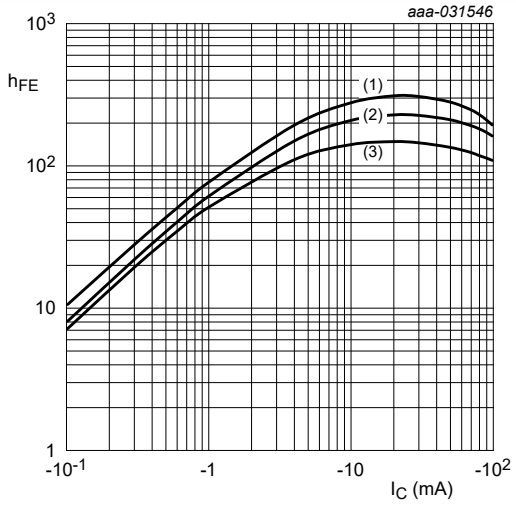

$I_C/I_B$ = 20
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 31. NHUMD12, TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



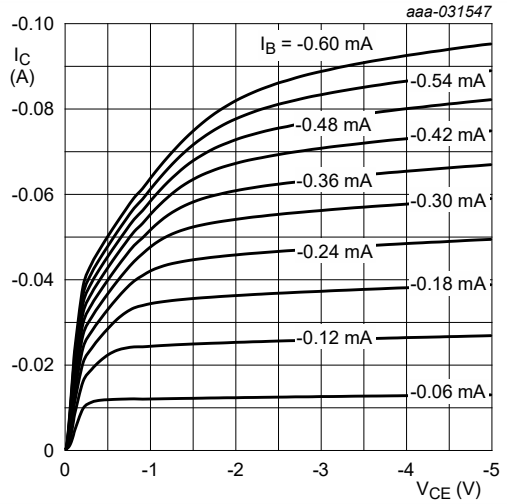

f = 1 MHz
$T_{amb}$ = 25 °C

**Fig. 32. NHUMD12, TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values**



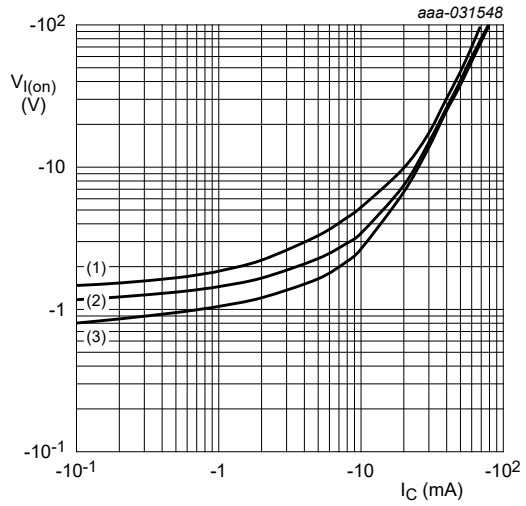

$V_{CE}$ = -5 V
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 33. NHUMD12, TR2 (PNP): DC current gain as a function of collector current; typical values**



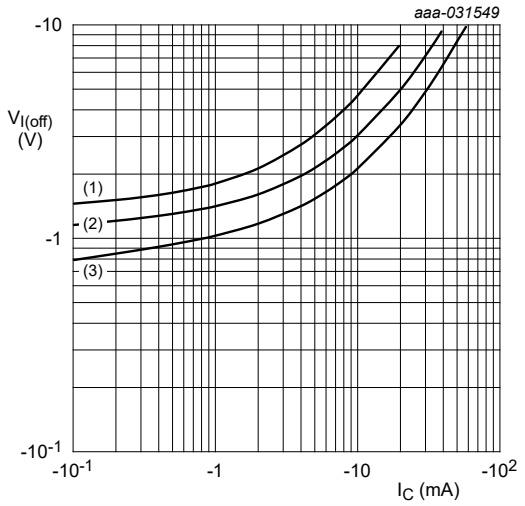

$T_{amb}$ = 25 °C

**Fig. 34. NHUMD12, TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values**



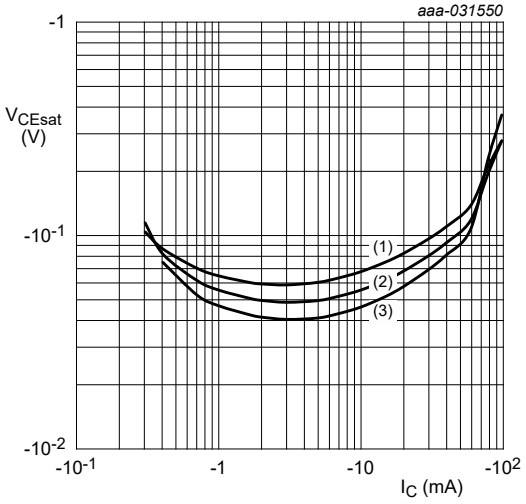

$V_{CE}$ = -0.3 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 35. NHUMD12, TR2 (PNP): On-state input voltage as a function of collector current; typical values**



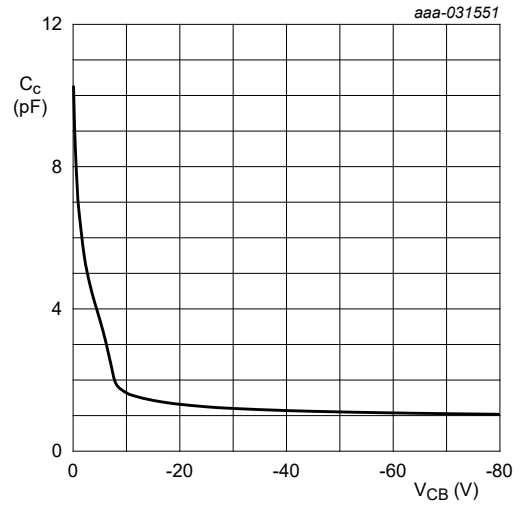

$V_{CE}$ = -5 V
(1) $T_{amb}$ = -40 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = 100 °C

**Fig. 36. NHUMD12, TR2 (PNP): Off-state input voltage as a function of collector current; typical values**



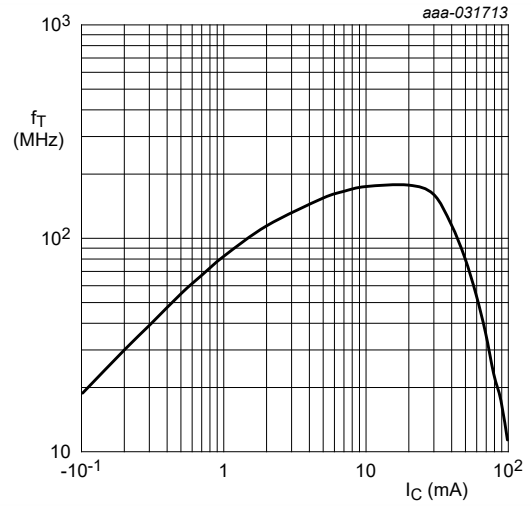

$I_C/I_B$ = 20
(1) $T_{amb}$ = 100 °C
(2) $T_{amb}$ = 25 °C
(3) $T_{amb}$ = -40 °C

**Fig. 37. NHUMD12, TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



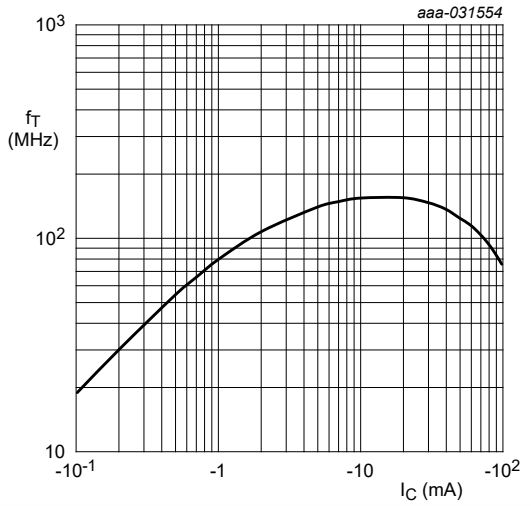

f = 1 MHz
$T_{amb}$ = 25 °C

**Fig. 38. NHUMD12, TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values of built-in transistor**




f = 100 MHz
$V_{CE}$ = 5 V
$T_{amb}$ = 25 °C

**Fig. 39. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor**




f = 100 MHz
$V_{CE}$ = -5 V
$T_{amb}$ = 25 °C

**Fig. 40. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor**

# 11. Test information

## Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

## Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_{I4}) - V(I_{I3})}{R1 \cdot (I_{I4} - I_{I3})} - 1$$

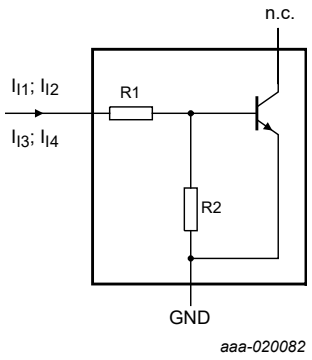



**Fig. 41. TR1 (NPN): Resistor test circuit**

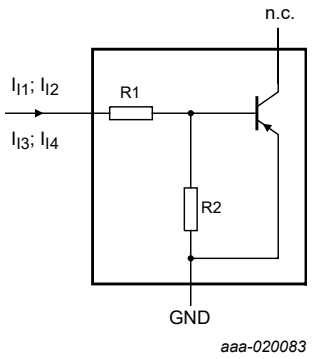



**Fig. 42. TR2 (PNP): Resistor test circuit**

## Resistor test conditions

**Table 9. Resistor test conditions**

| Type number | R1 (kΩ) | R2 (kΩ) | Test conditions | | | |
|---|---|---|---|---|---|---|
| | | | $I_{I1}$ | $I_{I2}$ | $I_{I3}$ | $I_{I4}$ |
| **Per transistor; for the PNP transistor with negative polarity** | | | | | | |
| NHUMD3 | 10 | 10 | 800 µA | 1.1 mA | -350 µA | -450 µA |
| NHUMD2 | 22 | 22 | 550 µA | 750 µA | -150 µA | -230 µA |
| NHUMD12 | 47 | 47 | 250 µA | 350 µA | -55 µA | -105 µA |

## 12. Package outline

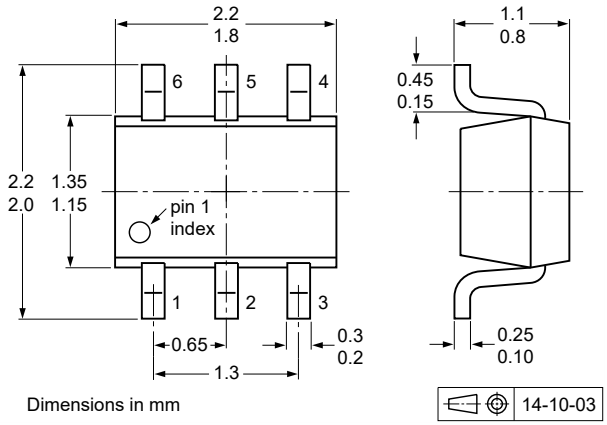



Fig. 43. Package outline SOT363 (SC-88)

## 13. Soldering

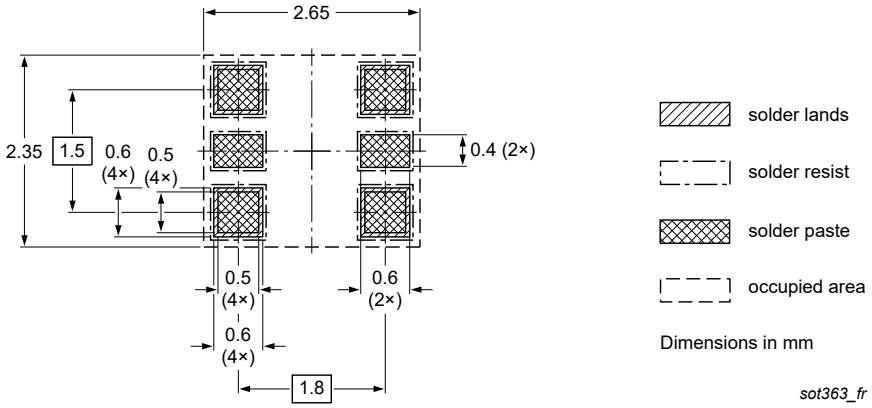



Fig. 44. Reflow soldering footprint for SOT363 (SC-88)

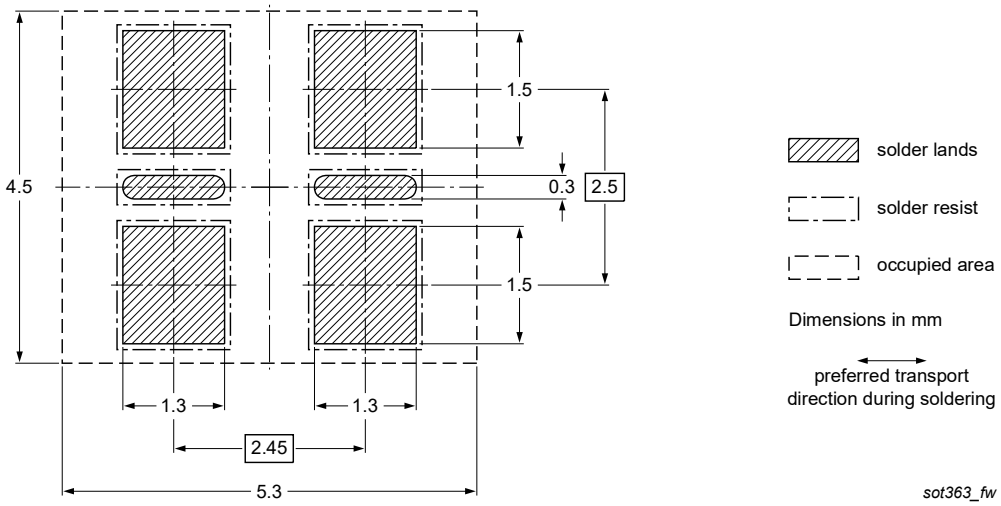



Fig. 45. Wave soldering footprint for SOT363 (SC-88)

# 14. Revision history

**Table 10. Revision history**

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| NHUMD3_2_12_SER v.1 | 20200724 | Product data sheet | - | - |

# 15. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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