



# PESD1V0R1BSF

Extremely low capacitance bidirectional ESD protection diode

22 July 2020

Short data sheet

## 1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS protection family. This device is housed in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

## 2. Features and benefits

- Bidirectional ESD protection of one line
- Extremely low diode capacitance  $C_d = 0.155$  pF at 0 V
- Extremely low insertion loss  $\alpha_{IL} = -0.27$  dB at 10 GHz
- Extremely low return loss  $\alpha_{RL} = -14.3$  dB at 10 GHz
- Extremely low clamping voltage to protect sensitive I/Os
- Extremely low inductance protection path to ground
- Extremely low leakage 1 nA typical at 1 V
- Ultra small SMD package

## 3. Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals
- Thunderbolt and USB4 data lines


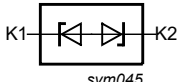
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RWM}$	reverse standoff voltage		-1	-	1	V
$C_d$	diode capacitance	$f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C	-	0.155	0.186	pF

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode	 <p>Transparent top view</p> <p><b>DSN0603-2 (SOD962-2)</b></p>	 <p>sym045</p>
2	K2	cathode		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD1V0R1BSF	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body	SOD962-2

## 7. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

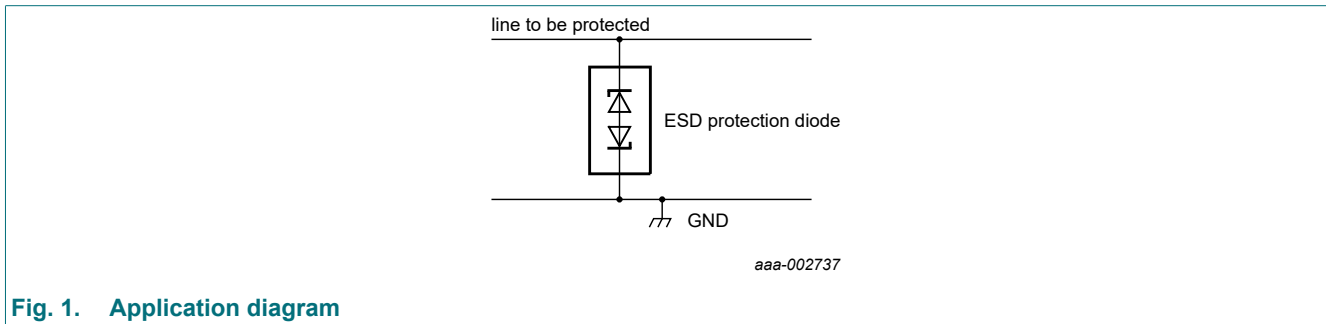


Fig. 1. Application diagram

### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

### 8. Package outline

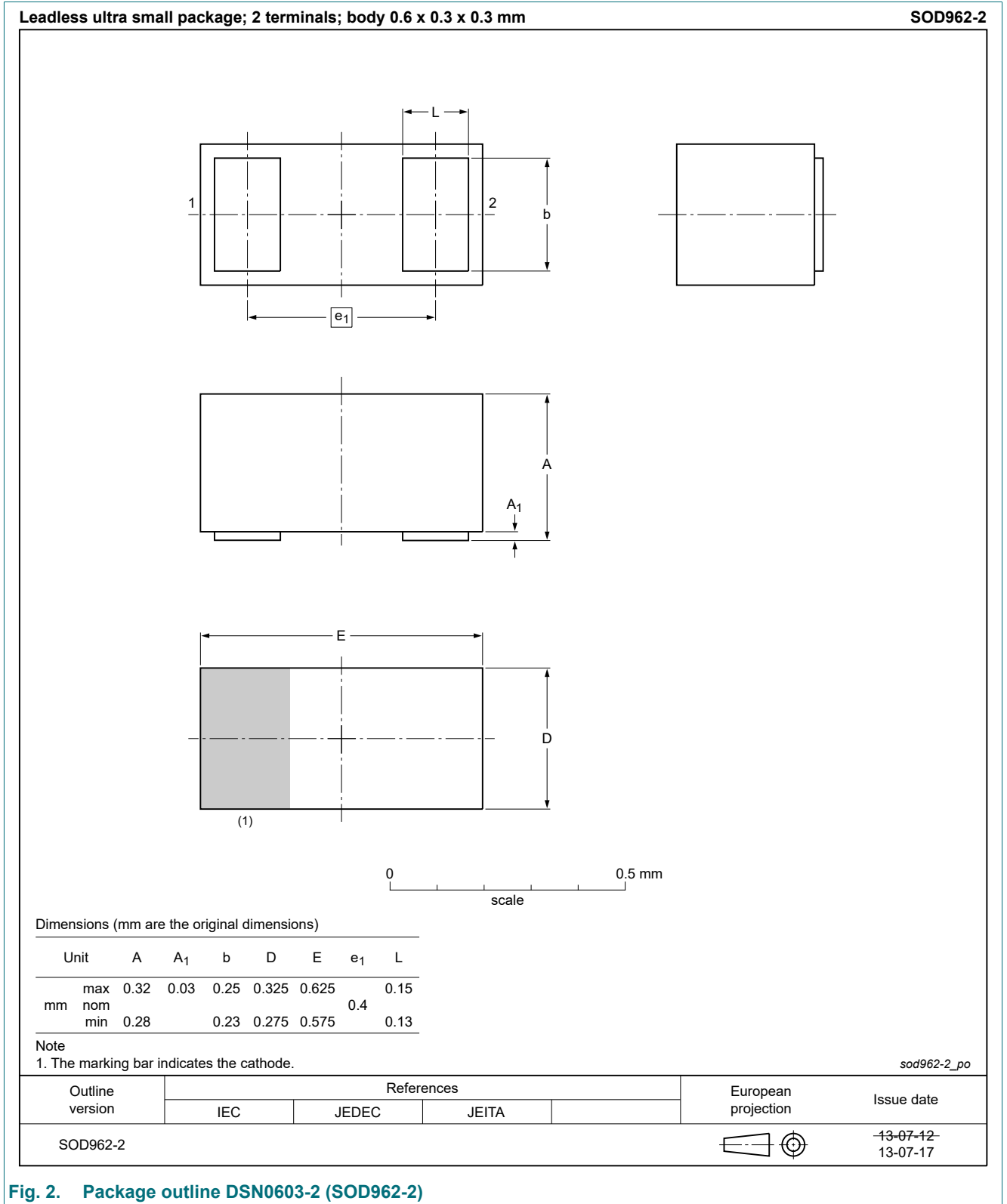
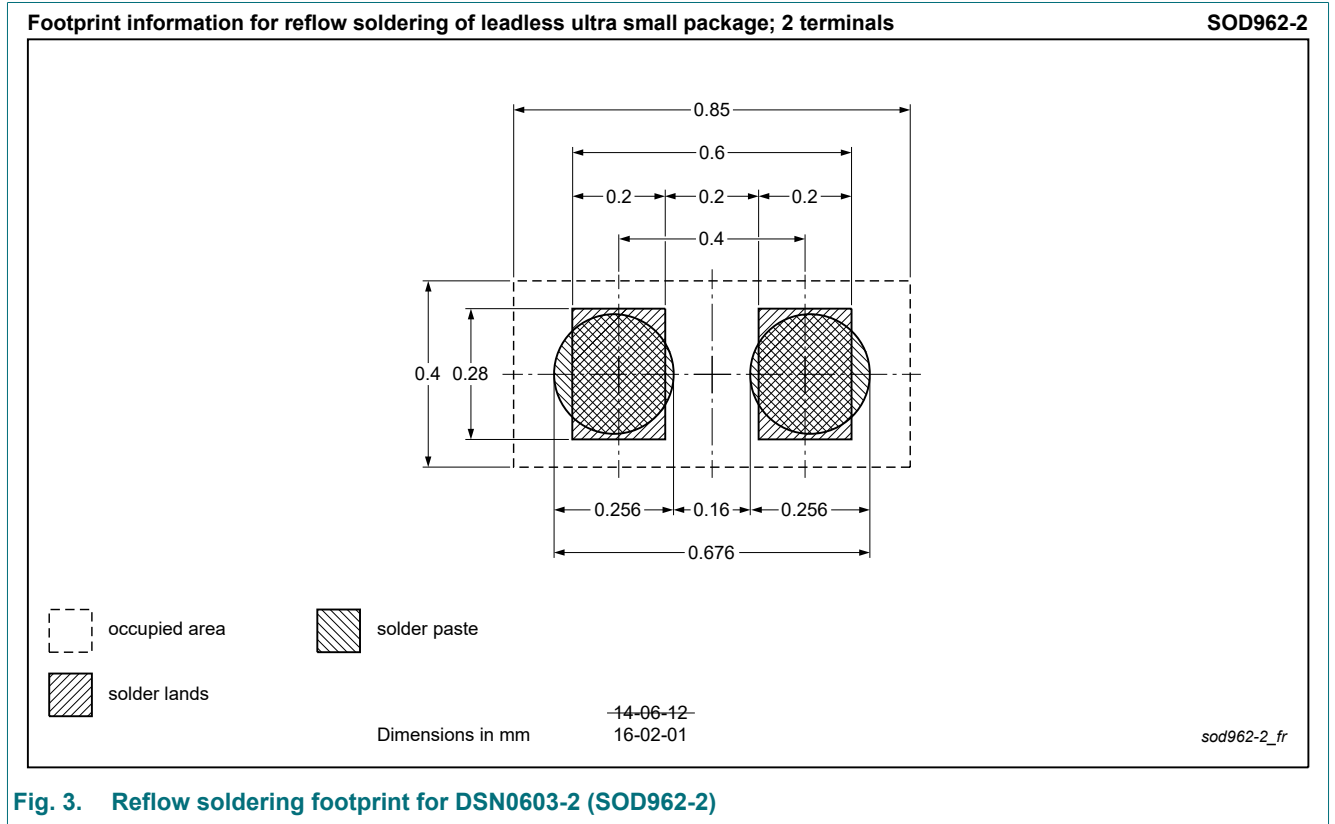


Fig. 2. Package outline DSN0603-2 (SOD962-2)

### 9. Soldering



### 10. Revision history

Table 4. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD1V0R1BSF_SDS v.1	20200722	Short data sheet	-	-

## 11. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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