74HC137

3-to-8 line decoder, demultiplexer with address latches; inverting

Rev. 6 — 11 January 2024 **Product data sheet**

1. General description

The 74HC137 decodes three binary weighted address inputs (A0, A1 and A2) to eight mutually exclusive outputs ($\overline{Y0}$ to $\overline{Y7}$). The device features a latch enable ($\overline{LE}$) and two output enable ($\overline{E}1$, E2) inputs. A LOW on $\overline{LE}$ causes the device to act as an active LOW decoder. A LOW-to HIGH transition on $\overline{LE}$ stores the data that was present before the transition in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH.

The output enable inputs control the state of the outputs independently of the address inputs or latch operation. All outputs will be HIGH unless $\overline{E}1$ is LOW and E2 is HIGH.

Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active LOW mutually exclusive outputs
- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +80 °C and from -40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC137D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC137PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

nexperia

4. Functional diagram

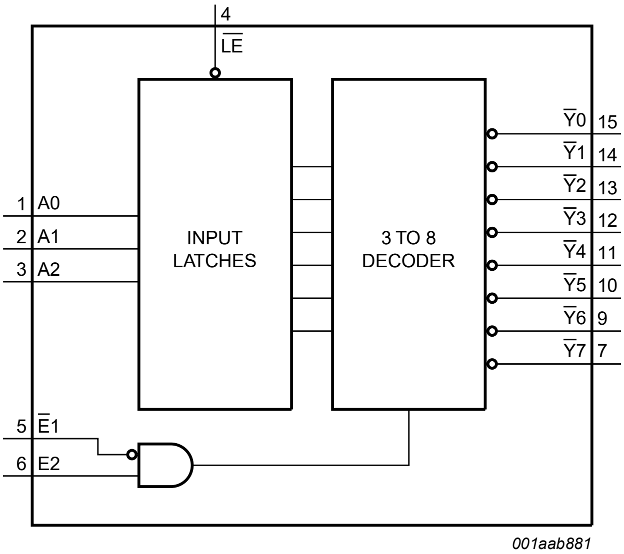


Fig. 1. Functional diagram

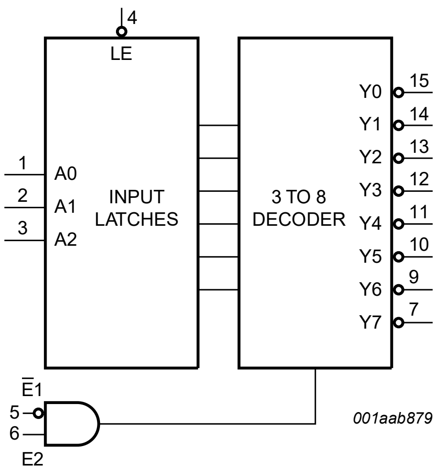


Fig. 2. Logic symbol

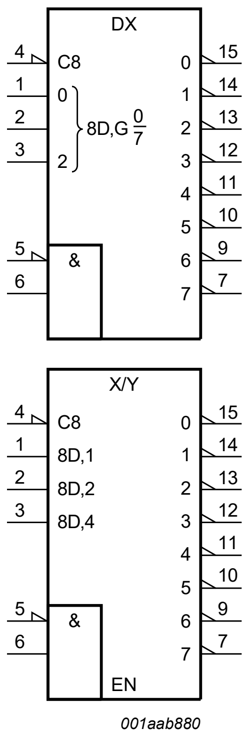


Fig. 3. IEC logic symbol

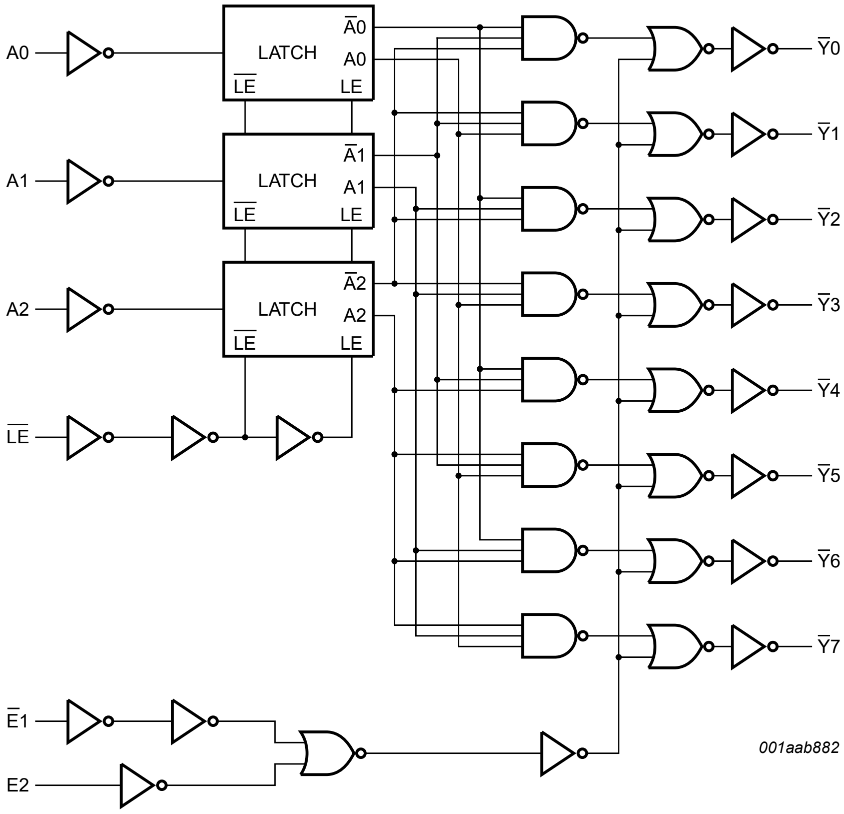
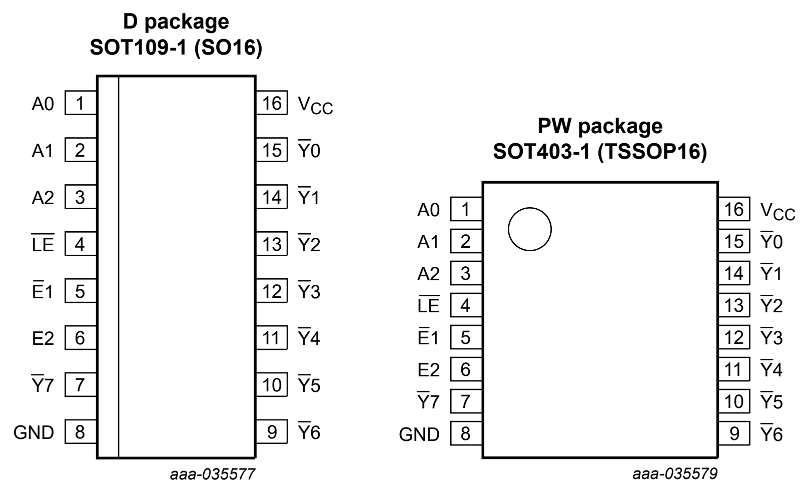


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A0	1	data input 0
A1	2	data input 1
A2	3	data input 2
$\overline{LE}$	4	latch enable input (active LOW)
$\overline{E}1$	5	data enable input 1 (active LOW)
E2	6	data enable input 2 (active HIGH)
$\overline{Y}7$	7	multiplexer output 7
GND	8	ground (0 V)
$\overline{Y}6$	9	multiplexer output 6
$\overline{Y}5$	10	multiplexer output 5
$\overline{Y}4$	11	multiplexer output 4
$\overline{Y}3$	12	multiplexer output 3
$\overline{Y}2$	13	multiplexer output 2
$\overline{Y}1$	14	multiplexer output 1
$\overline{Y}0$	15	multiplexer output 0
V_{CC}	16	positive supply voltage

6. Function table

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Enable			Input			Output							
$\overline{LE}$	$\overline{E}1$	E2	A0	A1	A2	$\overline{Y}0$	$\overline{Y}1$	$\overline{Y}2$	$\overline{Y}3$	$\overline{Y}4$	$\overline{Y}5$	$\overline{Y}6$	$\overline{Y}7$
H	L	H	X	X	X	stable							
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
			H	L	L	H	L	H	H	H	H	H	H
			L	H	L	H	H	L	H	H	H	H	H
			H	H	L	H	H	H	L	H	H	H	H
			L	L	H	H	H	H	H	L	H	H	H
			H	L	H	H	H	H	H	H	L	H	H
			L	H	H	H	H	H	H	H	H	L	H
			H	H	H	H	H	H	H	H	H	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input diode current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-	±20	mA
I_{OK}	output diode current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	-	±20	mA
I_O	output source or sink current	V_O = -0.5 V to V_{CC} + 0.5 V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	power dissipation	[1]	-	500	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V
T_{amb}	ambient temperature		-40	-	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = -40 °C to +85 °C		T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

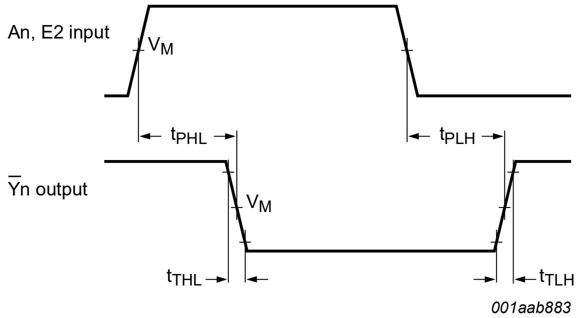
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF; For test circuit see Fig. 8

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = -40 °C to +85 °C		T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	An to $\overline{Y}$n; see Fig. 5 [1]								
		V_{CC} = 2.0 V	-	58	180	-	225	-	270	ns
		V_{CC} = 4.5 V	-	21	36	-	45	-	54	ns
		V_{CC} = 6.0 V	-	17	31	-	38	-	46	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	18	-	-	-	-	-	ns
		$\overline{LE}$ to $\overline{Y}$n; see Fig. 6								
		V_{CC} = 2.0 V	-	55	190	-	240	-	285	ns
		V_{CC} = 4.5 V	-	20	38	-	48	-	57	ns
		V_{CC} = 6.0 V	-	16	32	-	41	-	48	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		$\overline{E}$1 to $\overline{Y}$n; see Fig. 6								
		V_{CC} = 2.0 V	-	50	145	-	180	-	220	ns
		V_{CC} = 4.5 V	-	18	29	-	36	-	44	ns
		V_{CC} = 6.0 V	-	14	25	-	31	-	38	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
		E2 to $\overline{Y}$n; see Fig. 5								
		V_{CC} = 2.0 V	-	50	145	-	180	-	220	ns
		V_{CC} = 4.5 V	-	18	29	-	36	-	44	ns
		V_{CC} = 6.0 V	-	14	25	-	31	-	38	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
t_t	transition time	see Fig. 5 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	$\overline{LE}$ HIGH; see Fig. 7								
		V_{CC} = 2.0 V	50	11	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	4	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	3	-	11	-	13	-	ns
t_{su}	set-up time	An to $\overline{LE}$; see Fig. 7								
		V_{CC} = 2.0 V	50	3	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	1	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	1	-	11	-	13	-	ns
t_h	hold time	An to $\overline{LE}$; see Fig. 7								
		V_{CC} = 2.0 V	30	3	-	40	-	45	-	ns
		V_{CC} = 4.5 V	6	1	-	8	-	9	-	ns
		V_{CC} = 6.0 V	5	1	-	7	-	8	-	ns

Symbol	Parameter	Conditions		T_{amb} = 25 °C			T_{amb} = -40 °C to +85 °C		T_{amb} = -40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[3]	-	57	-	-	-	-	-	pF

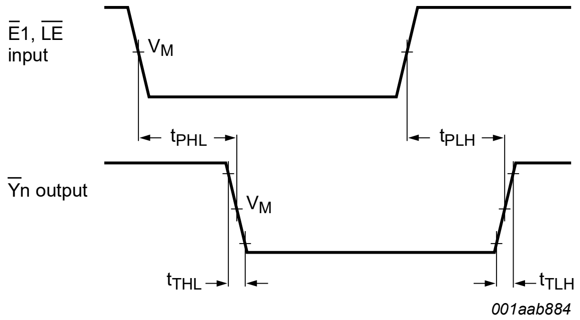
[1] t_{pd} is the same as t_{PHL}, t_{PLH}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \sum(C_L \times V_{CC}{}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}{}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



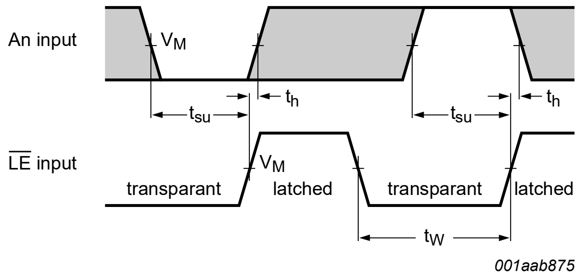
$V_M = 0.5 \times V_I$.

Fig. 5. Waveforms showing the address input (An) and enable input (E2) to output ($\overline{Y}$n) propagation delays and the output transition times



$V_M = 0.5 \times V_I$.

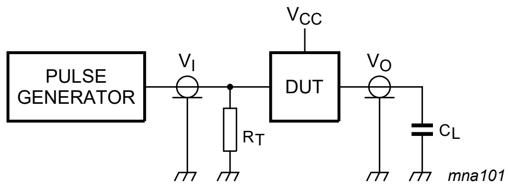
Fig. 6. Waveforms showing the enable input ($\overline{E}$1, $\overline{LE}$) to output ($\overline{Y}$n) propagation delays and the output transition times



The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_M = 0.5 \times V_I$.

Fig. 7. Waveforms showing the data set-up, hold times for An input to $\overline{LE}$ input and the latch enable pulse width



Test data is given in Table 8.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance.

Fig. 8. Test circuit for measuring switching times

Table 8. Test data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V	V_{CC}	6 ns	50 pF
4.5 V	V_{CC}	6 ns	50 pF
6.0 V	V_{CC}	6 ns	50 pF
5.0 V	V_{CC}	6 ns	15 pF

11. Application information

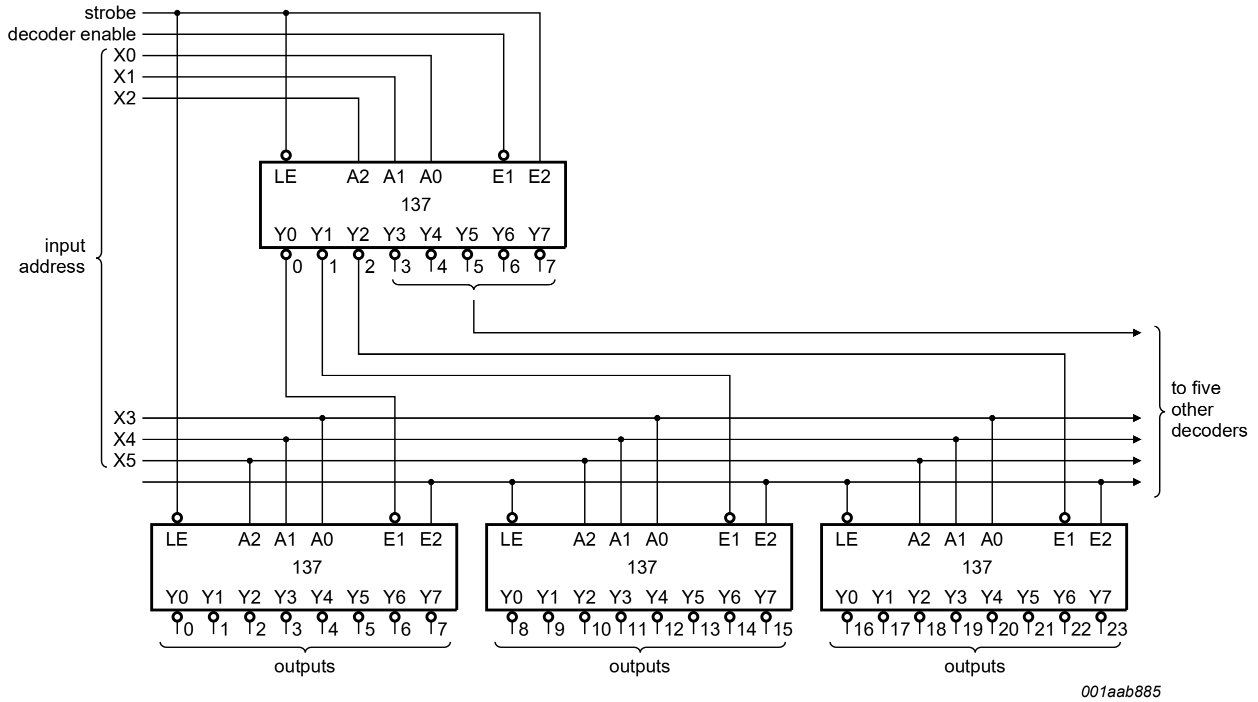
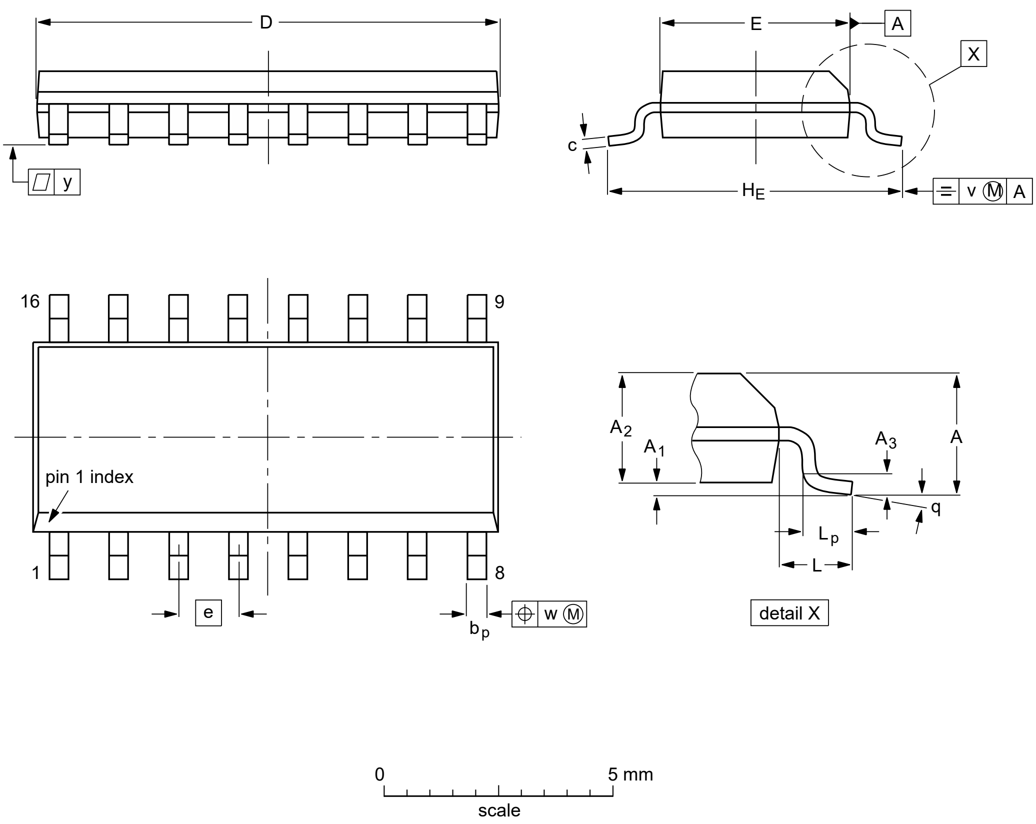


Fig. 9. 6-to-64 line decoder with input address storage

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

Note

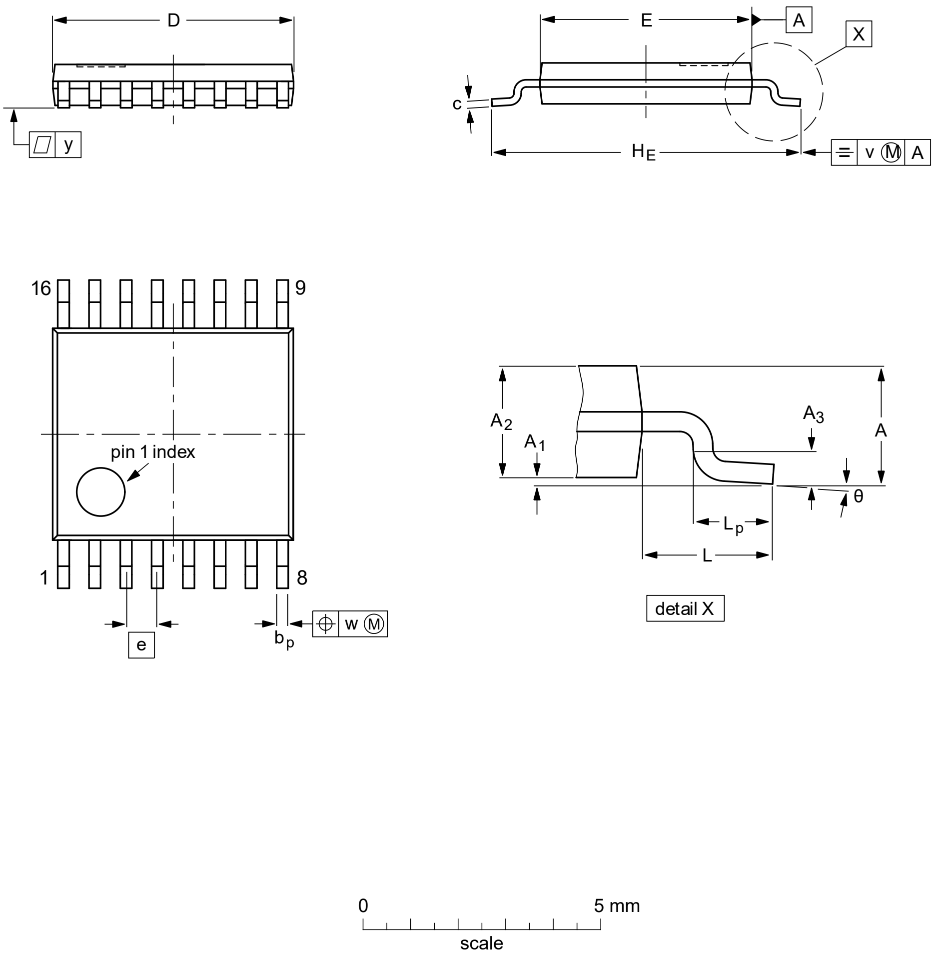
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 10. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

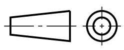
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 11. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 9. Abbreviations

Acronym	Abbreviation
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC137 v.6	20240111	Product data sheet	-	74HC137 v.5
Modifications:	• Type number 74HC137DB (SOT338-1/SSOP16) removed. • Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 10, Fig. 11: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
74HC137 v.5	20210804	Product data sheet	-	74HC137 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74HC137PW (SOT403-1/TSSOP16) added. • Section 1 and Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated.			
74HC137 v.4	20151223	Product data sheet	-	74HC137 v.3
Modifications:	• Type number 74HC137N (SOT38-4) removed.			
74HC137 v.3	20041111	Product data sheet	-	74HC_HCT137_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Removed type number 74HCT137. • Inserted family specification.			
74HC_HCT137_CNV v.2	19970827	Product specification	-	74HC_HCT137 v.1
74HC_HCT137 v.1	19901201	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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