



PSMN5R0-40MLH

N-channel 40 V, 5 mΩ, logic level MOSFET in LPAK33 using NextPower-S3 technology

27 April 2020

Product data sheet

1. General description

85 A, logic level N-channel enhancement mode MOSFET in 175 °C LPAK33 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high efficiency applications at high switching frequencies.

2. Features and benefits

- Avalanche rated, 100% tested
- NextPower-S3 technology delivers 'superfast switching with soft body-diode recovery'
- Low Q_{RR} , Q_G and Q_{GD} for high system efficiency, especially at high switching frequencies
- Low spiking and ringing for low EMI designs
- High reliability clip bonded and solder die attach Mini Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Brushless DC motor drive
- LED lighting

4. Quick reference data

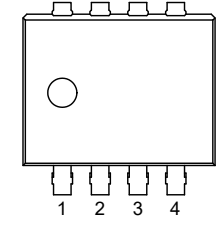
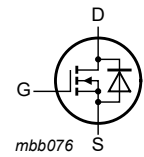
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	85	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	83	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	3.9	5	mΩ
		$V_{GS} = 4.5\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	4.9	6.4	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 20\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 12 ; Fig. 13	0.9	2.9	5.9	nC
$Q_{G(tot)}$	total gate charge		8.5	13	18	nC

[1] 85A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK33 (SOT1210)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN5R0-40MLH	LPAK33	Plastic, single ended surface mounted package (LPAK33); 8 leads; 0.65 mm pitch	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN5R0-40MLH	5H0L40

8. Limiting values

Table 5. Limiting values

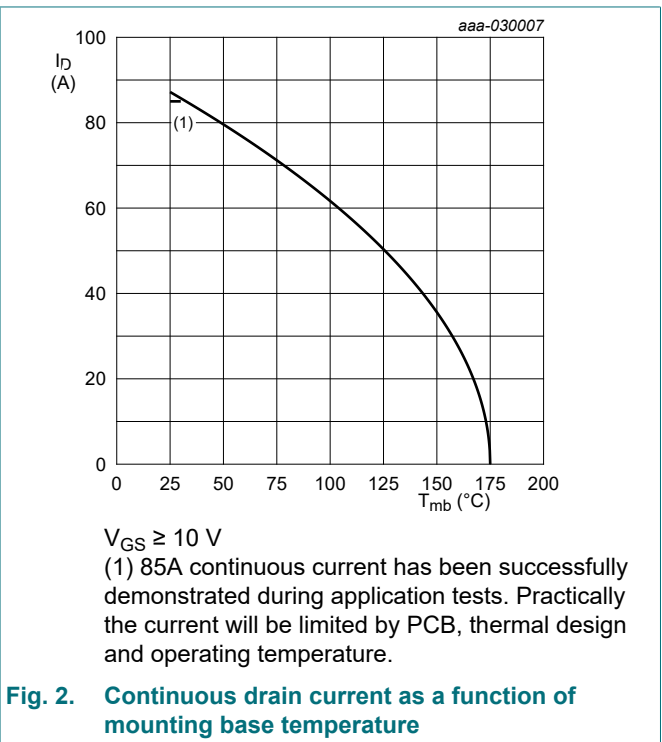
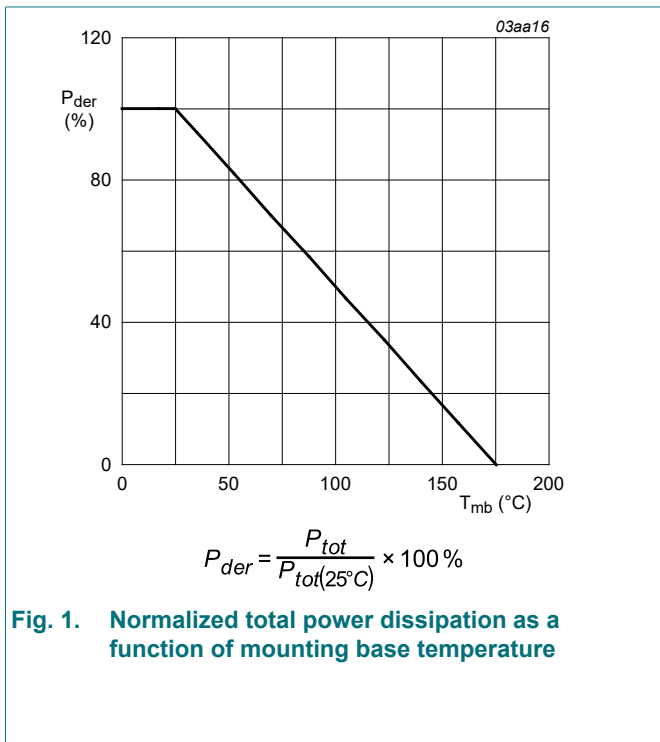
In accordance with the Absolute Maximum Rating System (IEC 60134).

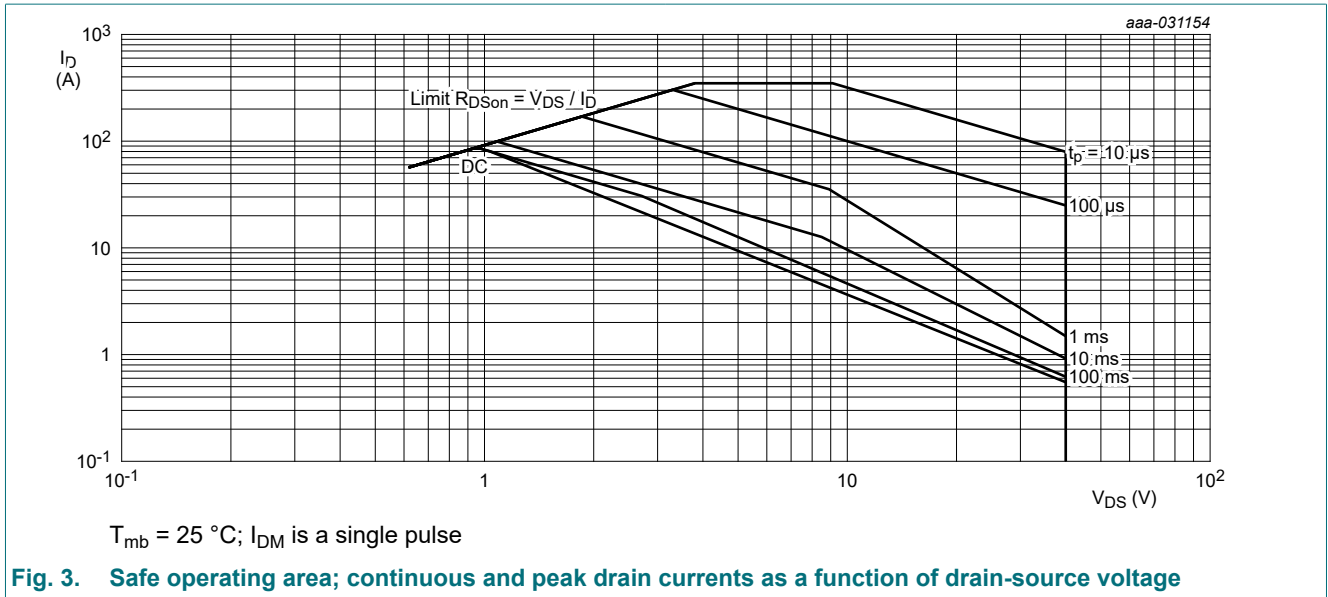
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	40	V
V_{DSM}	peak drain-source voltage	$t_p \leq 20\text{ ns}$; $f \leq 500\text{ kHz}$; $E_{DS(AL)} \leq 200\text{ nJ}$; pulsed		-	45	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$		-	40	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	83	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	85	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	62	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	349	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	85	A

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Symbol	Parameter	Conditions		Min	Max	Unit
I_{SM}	peak source current	pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25 \text{ }^\circ\text{C}$		-	349	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 29.6 \text{ A}$; $V_{sup} \leq 40 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; unclamped; $t_p = 107 \mu s$	[2]	-	82.7	mJ
		$I_D = 20 \text{ A}$; $V_{sup} \leq 40 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; unclamped; $t_p = 245 \mu s$	[2]	-	127.6	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 40 \text{ V}$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; $R_{GS} = 50 \Omega$	[2]	-	70	A

- [1] 85A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test

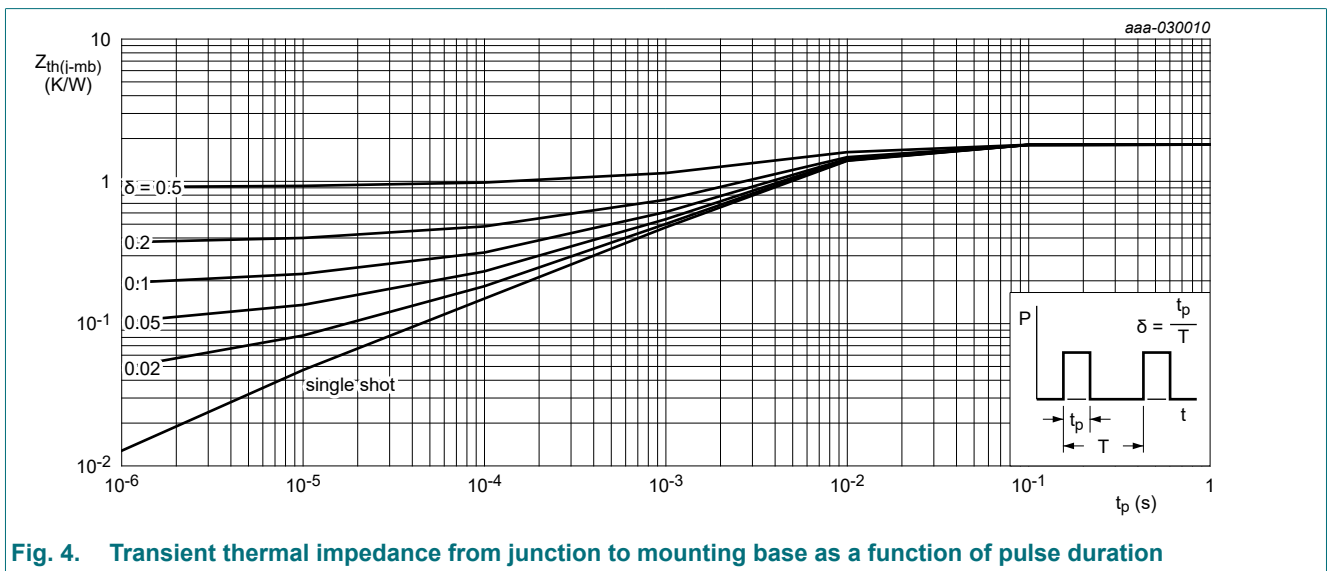


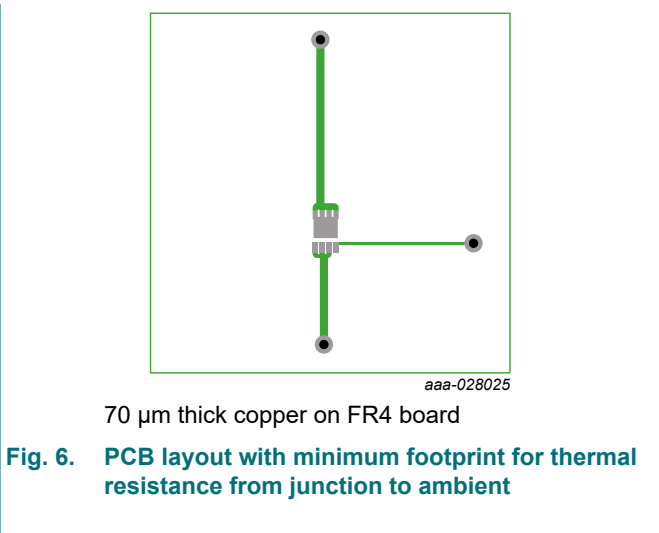
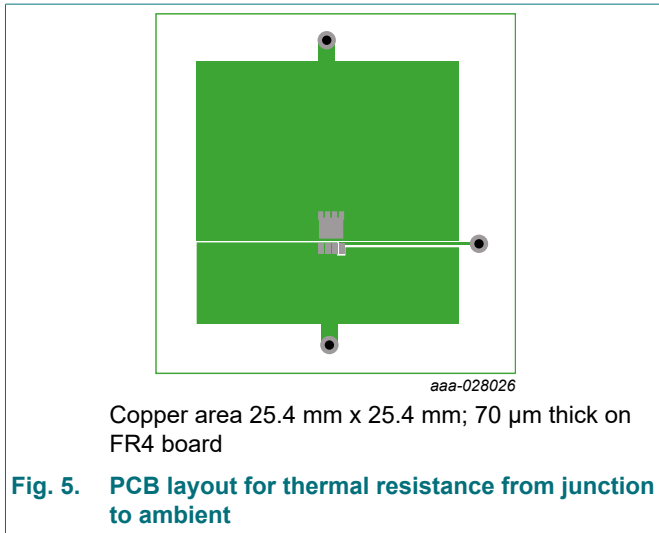


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	1.61	1.81	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	50	-	K/W
		Fig. 6	-	130	-	K/W





10. Characteristics

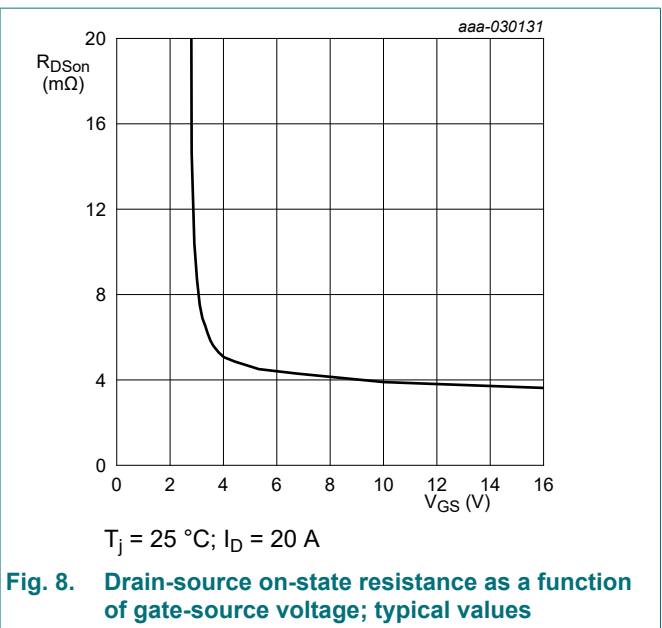
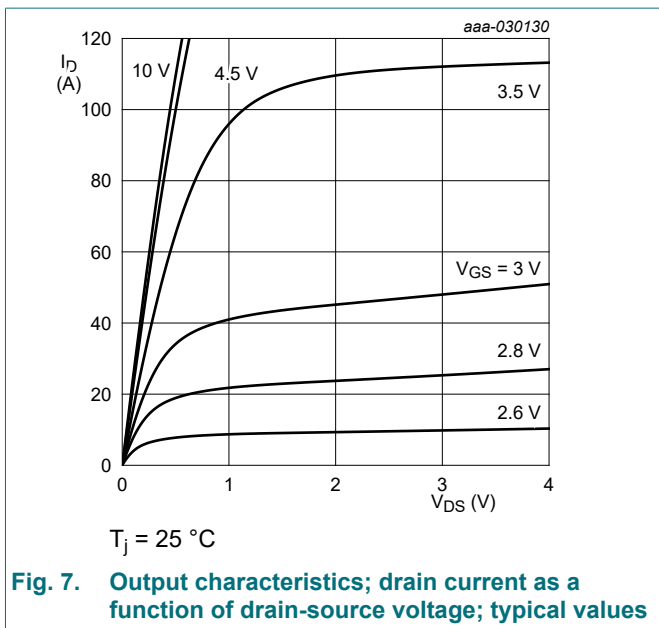
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.45	1.77	2.15	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-4.3	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 32 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.04	1	μA
		$V_{DS} = 32 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	0.9	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 10	-	3.9	5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 11	-	-	10.9	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 10	-	4.9	6.4	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 20 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 11	-	-	14	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.3	0.8	2	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 20 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 12; Fig. 13	8.5	13	18	nC
		$I_D = 20 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 12; Fig. 13	18	28	39	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	15	-	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Q_{GS}	gate-source charge	$I_D = 20\text{ A}; V_{DS} = 20\text{ V}; V_{GS} = 4.5\text{ V};$ Fig. 12 ; Fig. 13	3	4.9	7.4	nC	
$Q_{GS(th)}$	pre-threshold gate-source charge		1.7	2.9	4.3	nC	
$Q_{GS(th-pl)}$	post-threshold gate-source charge		1.2	2	2.8	nC	
Q_{GD}	gate-drain charge		0.9	2.9	5.9	nC	
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 20\text{ A}; V_{DS} = 20\text{ V};$ Fig. 12 ; Fig. 13	-	2.8	-	V	
C_{iss}	input capacitance	$V_{DS} = 20\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14	1230	1892	2649	pF	
C_{oss}	output capacitance		318	490	686	pF	
C_{riss}	reverse transfer capacitance		20	68	150	pF	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}; R_L = 1\text{ }\Omega; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega$	-	18	-	ns	
t_r	rise time		-	22	-	ns	
$t_{d(off)}$	turn-off delay time		-	17	-	ns	
t_f	fall time		-	12	-	ns	
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C}$	-	15	-	nC	
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 20\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 15	-	0.82	1	V	
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 20\text{ V};$ Fig. 16	-	24	-	ns	
Q_r	recovered charge		[1]	-	18	-	nC
t_a	reverse recovery rise time		-	-	15	-	ns
t_b	reverse recovery fall time		-	-	10	-	ns

[1] includes capacitive recovery



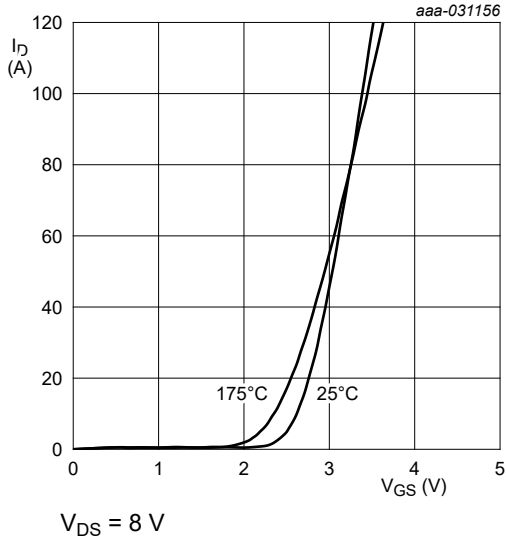


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

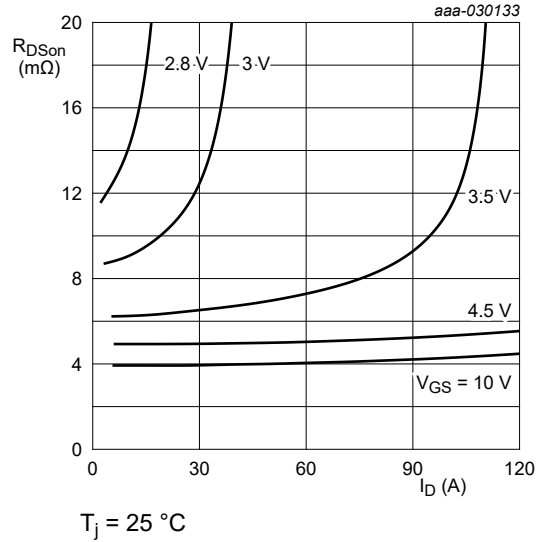


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

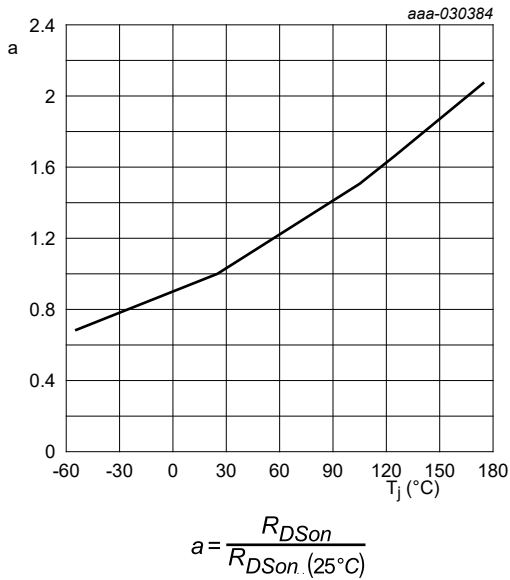


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

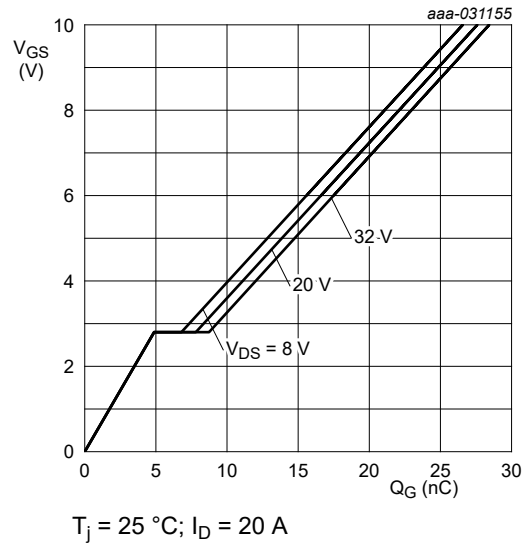


Fig. 12. Gate-source voltage as a function of gate charge; typical values

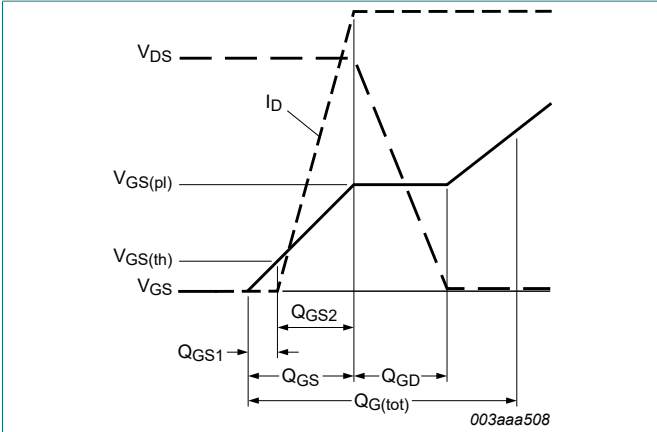
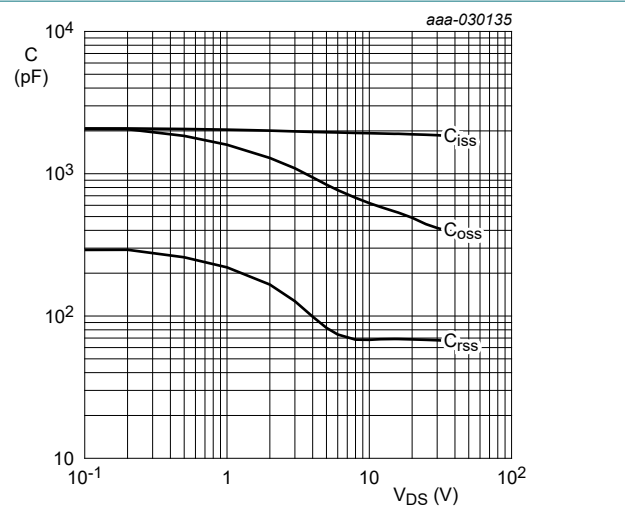
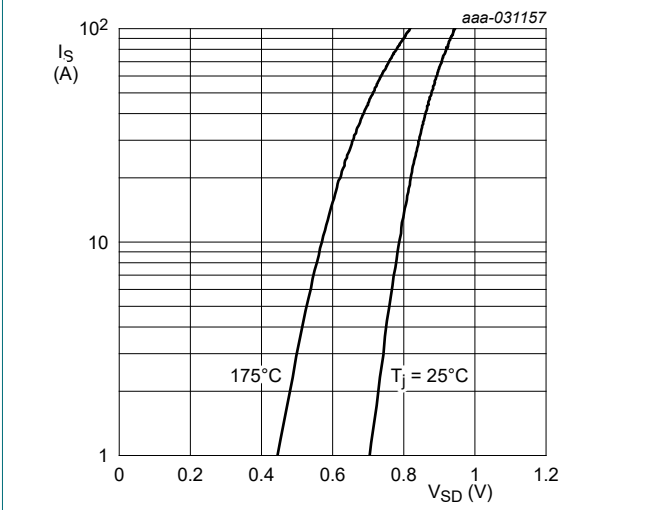


Fig. 13. Gate charge waveform definitions



$V_{GS} = 0$ V; $f = 1$ MHz

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0$ V

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

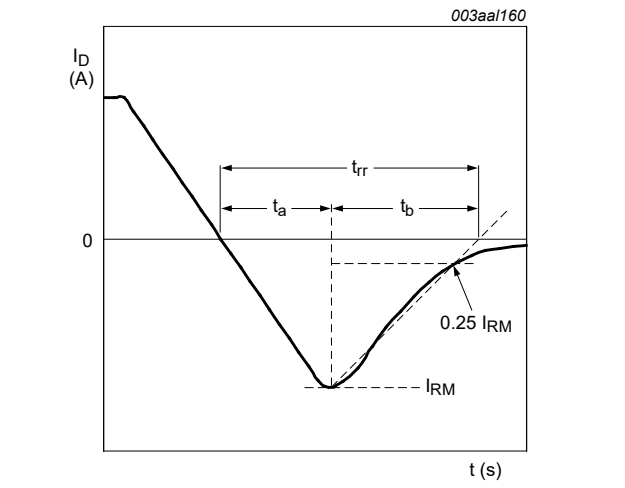


Fig. 16. Reverse recovery timing definition

11. Package outline

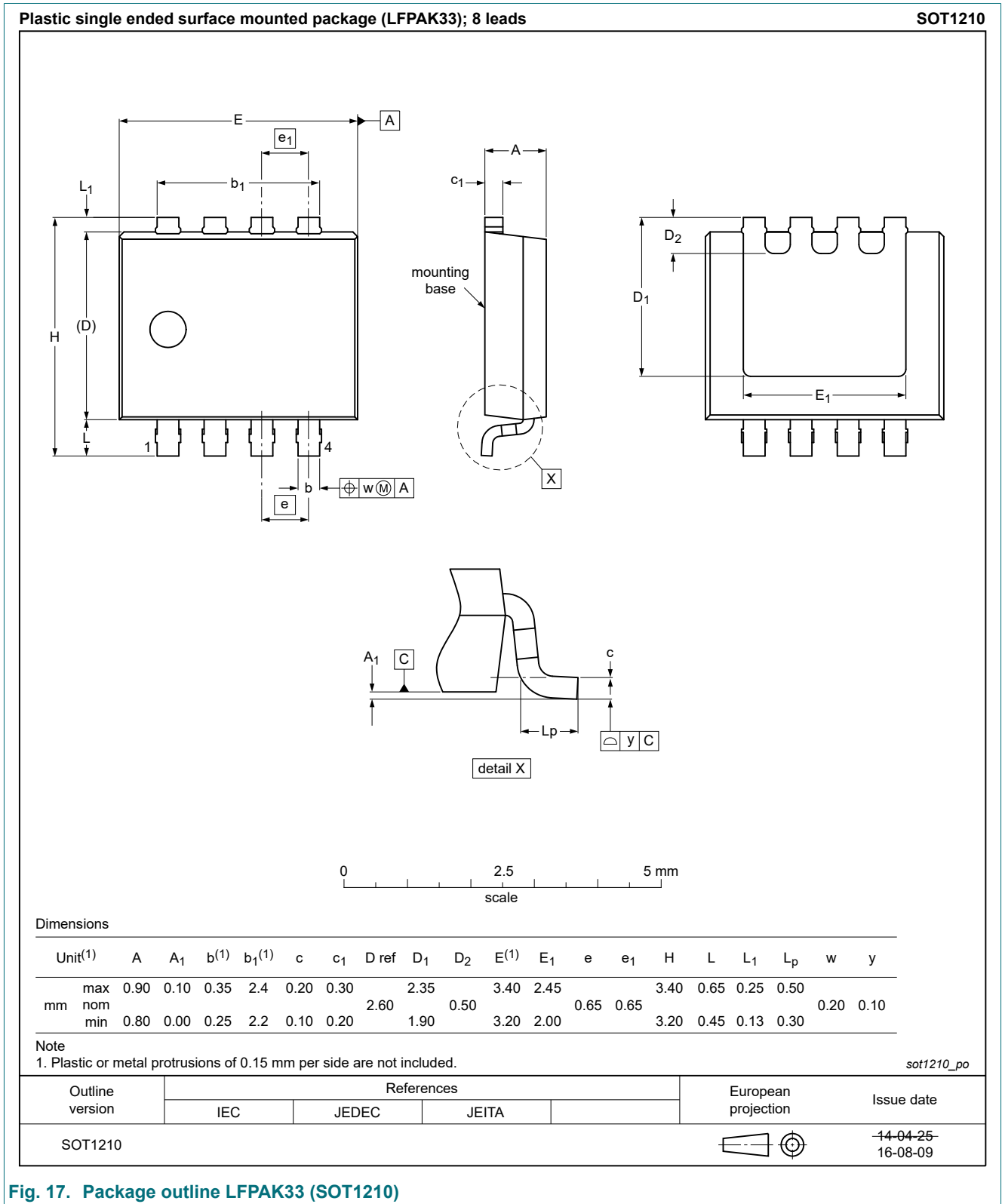


Fig. 17. Package outline LPAK33 (SOT1210)

12. Soldering

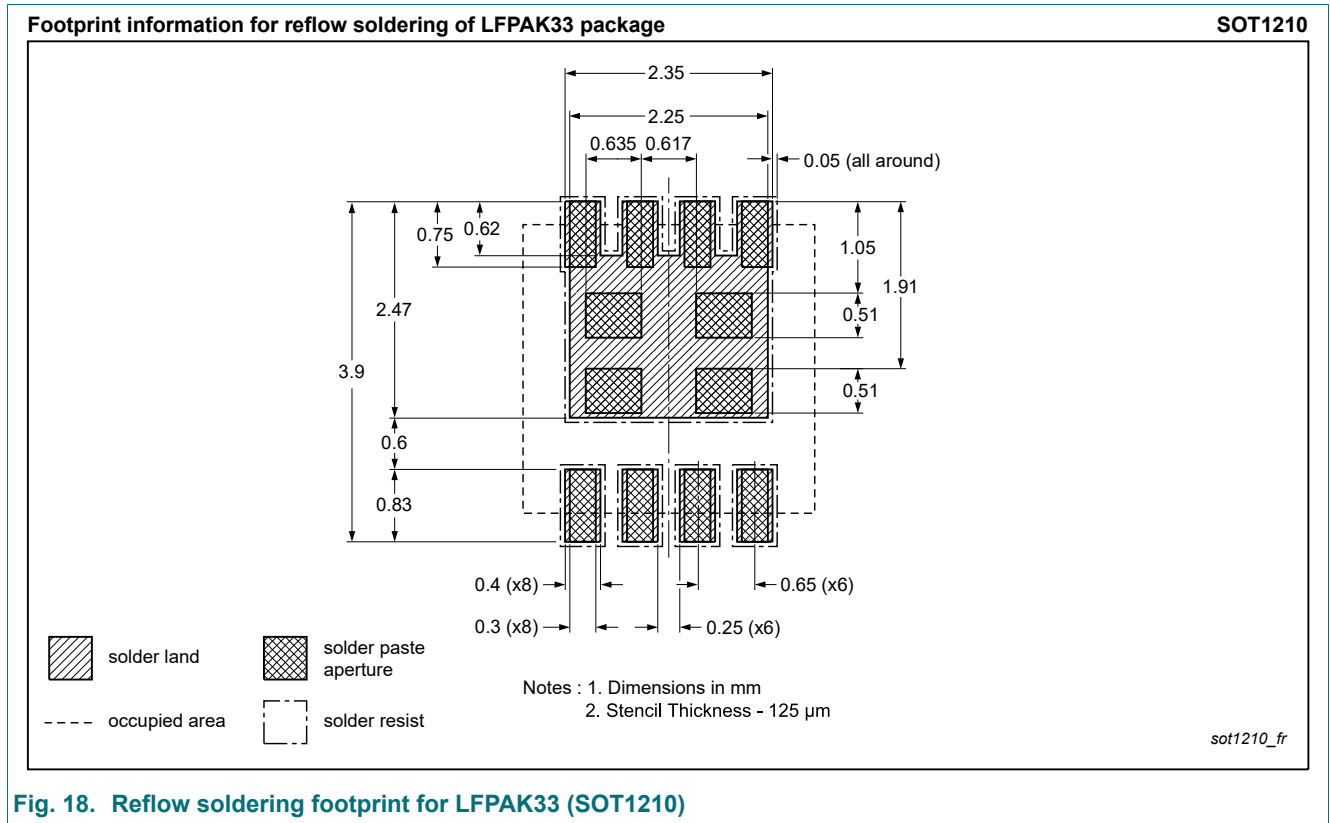


Fig. 18. Reflow soldering footprint for LPAK33 (SOT1210)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 27 April 2020

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