



PXN9R0-30QL

30 V, N-channel Trench MOSFET

31 July 2023

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in an MLPAK33 (SOT8002) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Trench MOSFET technology
- MLPAK33 package (3.3 x 3.3 mm footprint)

3. Applications

- DC-to-DC converters
- Battery management
- Low-side load-switch
- Switching circuits

4. Quick reference data

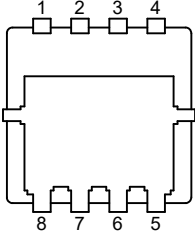
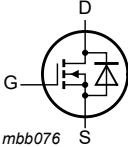
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-	30	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-	17.3	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 11.4\text{ A}; T_j = 25\text{ °C}$		-	7.7	9.1	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 10.1\text{ A}; T_j = 25\text{ °C}$		-	9.3	11.6	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-1)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN9R0-30QL	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PXN9R0-30QL	7AM

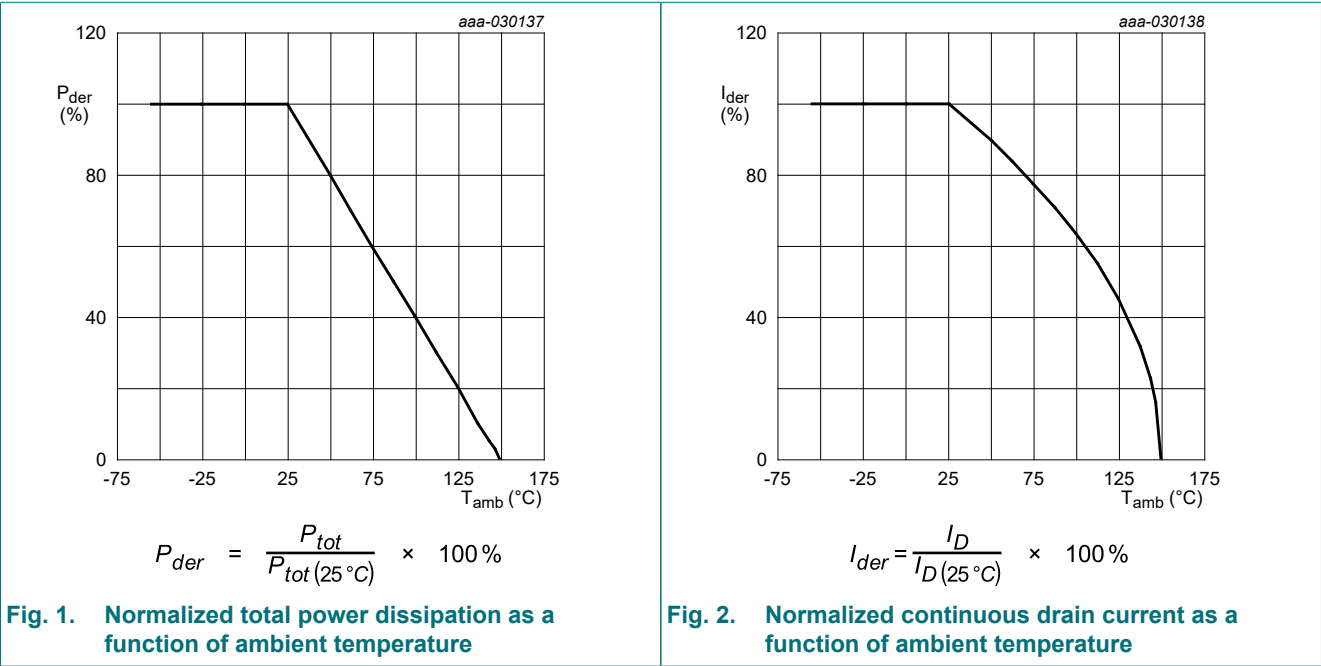
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	30	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	17.3	A
		V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	11.4	A
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	7.2	A
		V _{GS} = 10 V; T _{sp} = 25 °C		-	41.8	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	90	A
P _{tot}	total power dissipation	T _{amb} = 25 °C; t ≤ 5 s	[1]	-	4.5	W
		T _{amb} = 25 °C	[1]	-	1.9	W
		T _{sp} = 25 °C		-	26	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	1.7	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².



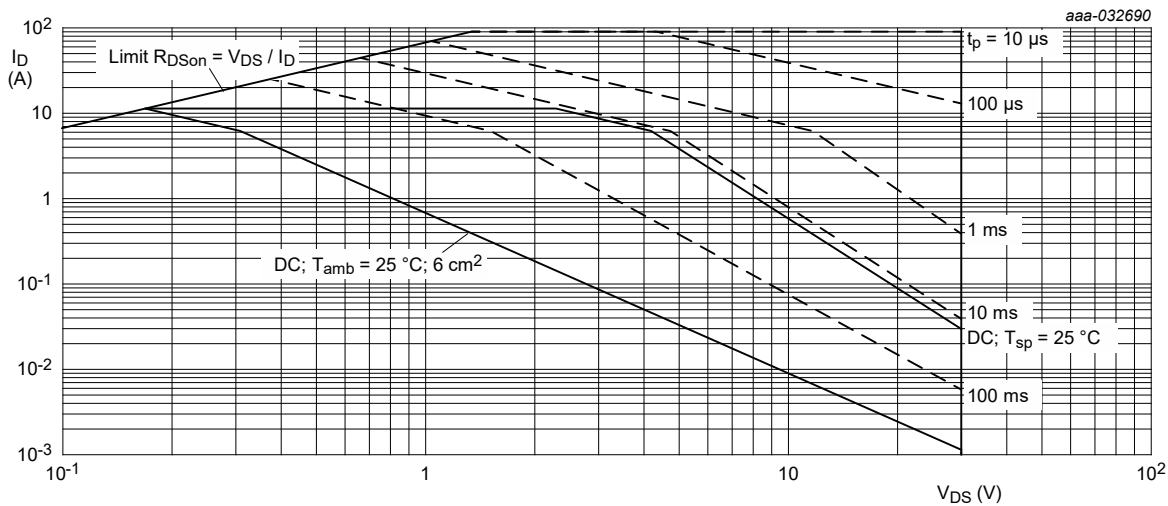


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	150	180	K/W
			[2]	-	55	65	K/W
		in free air; $t \leq 5$ s	[2]	-	24	28	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	4	4.8	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

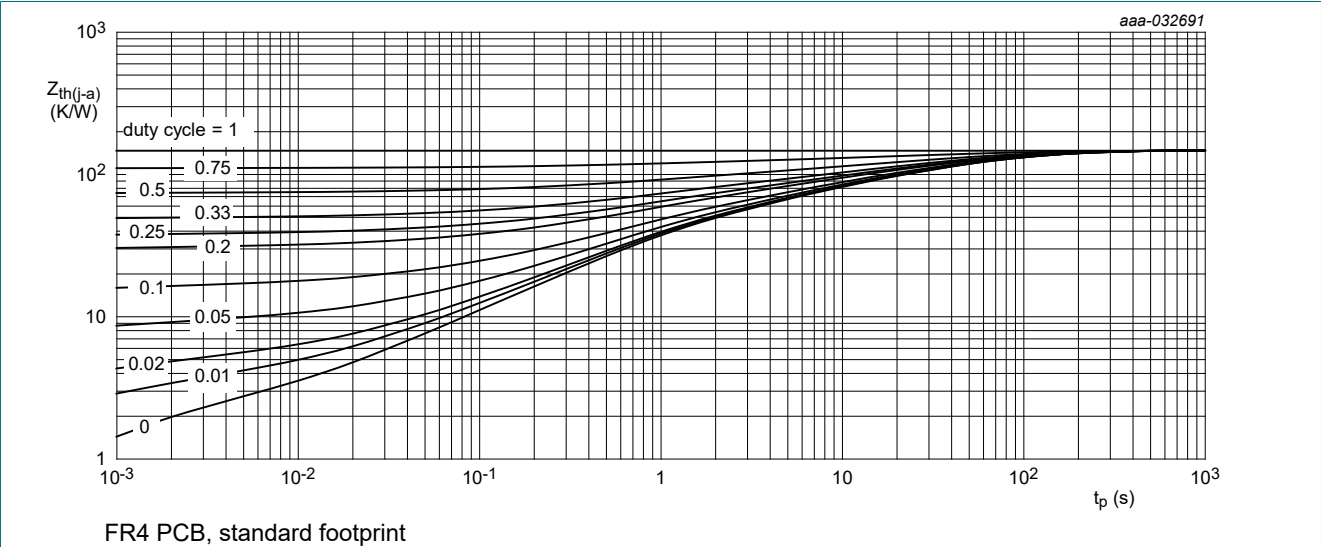


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

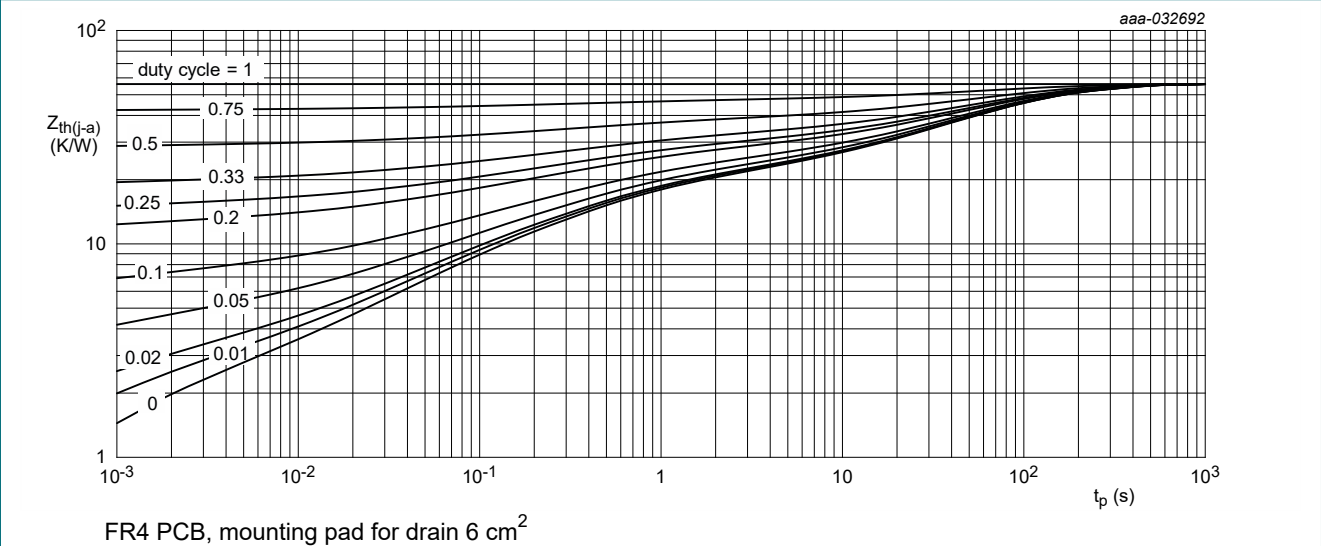


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		30	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		1	1.6	2.5	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 11.4 A; T _j = 25 °C		-	7.7	9.1	mΩ
		V _{GS} = 10 V; I _D = 11.4 A; T _j = 150 °C		-	12.6	14.9	mΩ
		V _{GS} = 4.5 V; I _D = 10.1 A; T _j = 25 °C		-	9.3	11.6	mΩ
R _G	gate resistance	f = 1 MHz		-	1.7	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = 15 V; I _D = 11.4 A; V _{GS} = 10 V; T _j = 25 °C		-	13.8	20.7	nC
		V _{DS} = 15 V; I _D = 10.1 A; V _{GS} = 4.5 V; T _j = 25 °C		-	6.7	10.1	nC
Q _{GS}	gate-source charge			-	2.1	-	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	1.3	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	0.8	-	nC
Q _{GD}	gate-drain charge			-	2	-	nC
V _{GSpl}	gate-source plateau voltage	V _{DS} = 15 V; I _D = 10.1 A; T _j = 25 °C		-	2.5	-	V
C _{iss}	input capacitance	V _{DS} = 15 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	865	-	pF
C _{oss}	output capacitance			-	153	-	pF
C _{rss}	reverse transfer capacitance			-	57	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; I _D = 10.1 A; V _{GS} = 4.5 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	6	-	ns
t _r	rise time			-	9	-	ns
t _{d(off)}	turn-off delay time			-	8	-	ns
t _f	fall time			-	4	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 1.7 A; V _{GS} = 0 V; T _j = 25 °C		-	0.7	1.2	V
t _{rr}	reverse recovery time	I _S = 1.7 A; dI _S /dt = -100 A/μs; V _{GS} = 4.5 V; V _{DS} = 15 V; T _j = 25 °C		-	14	-	ns
Q _r	recovered charge			-	6	-	nC
t _a	reverse recovery rise time			-	9	-	ns
t _b	reverse recovery fall time			-	5	-	ns

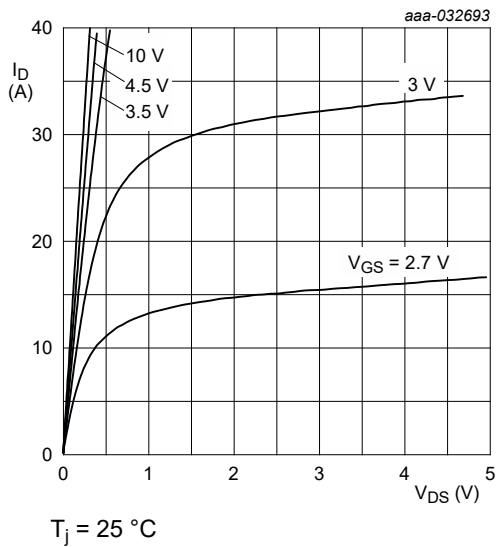


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

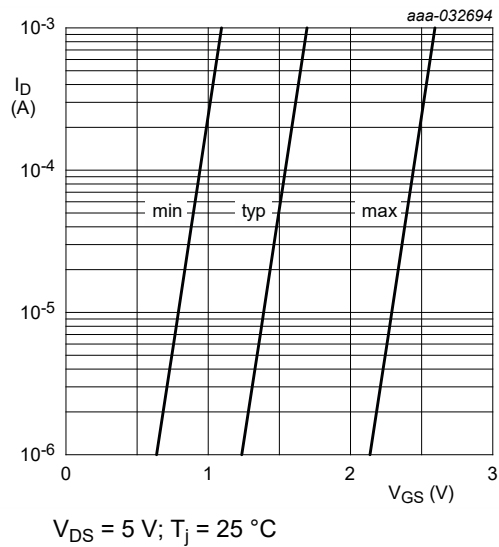


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

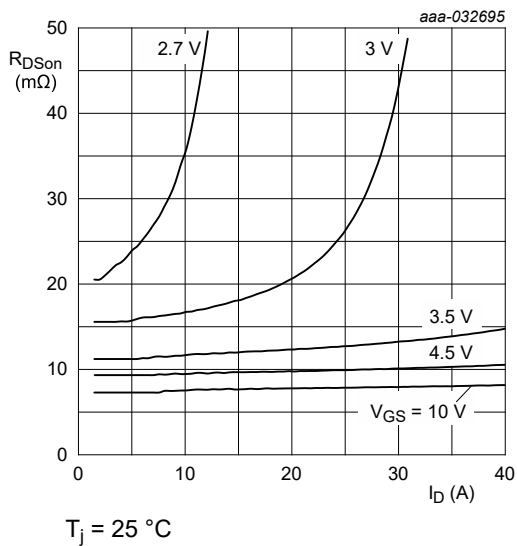


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

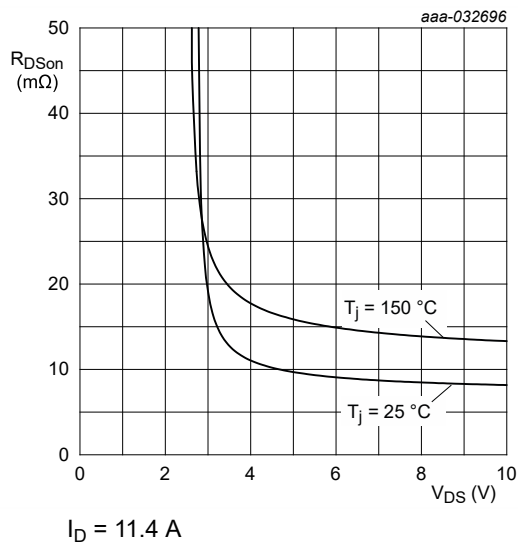


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

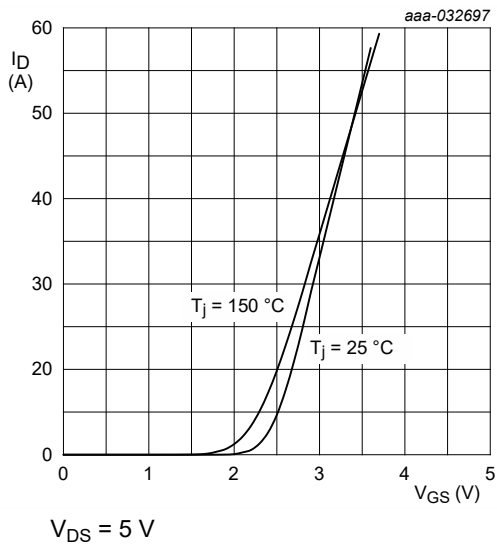


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

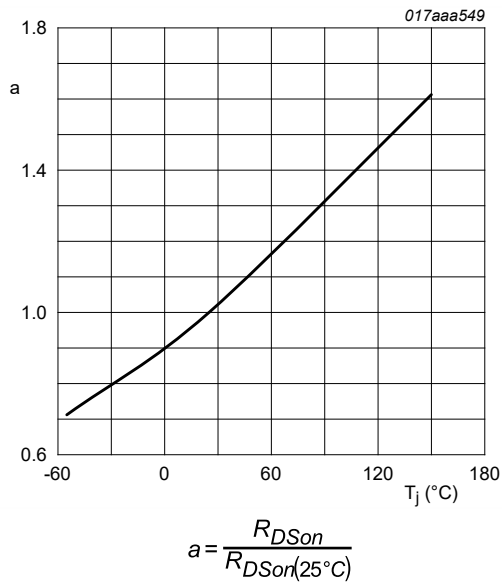


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

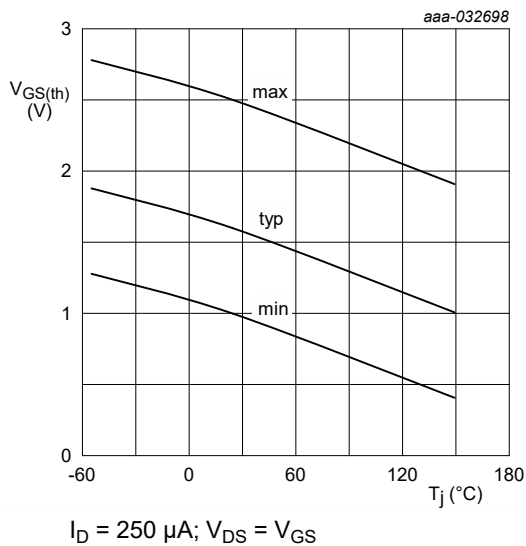


Fig. 12. Gate-source threshold voltage as a function of junction temperature

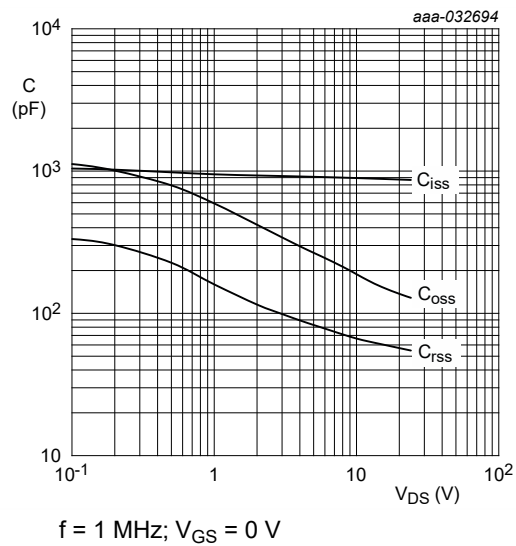


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

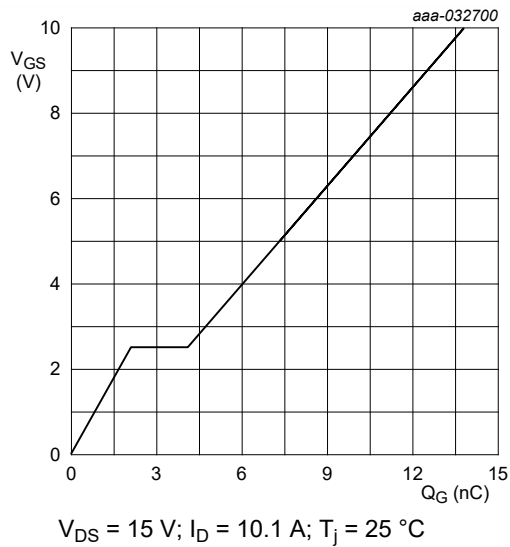


Fig. 14. Gate-source voltage as a function of gate charge; typical values

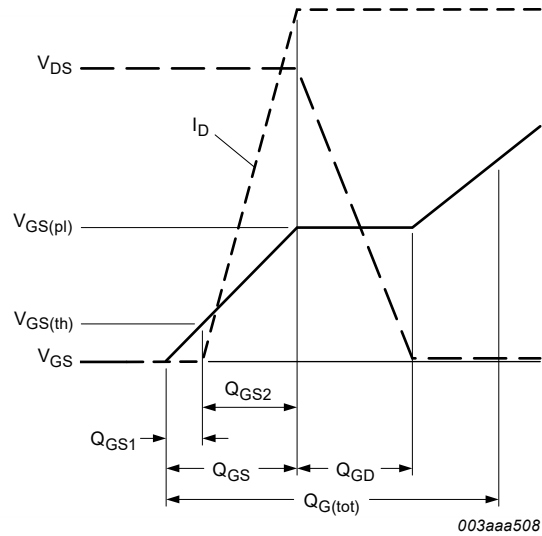


Fig. 15. Gate charge waveform definitions

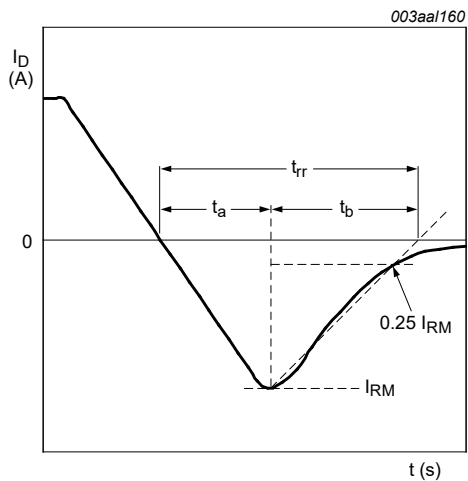


Fig. 16. Reverse recovery timing definition

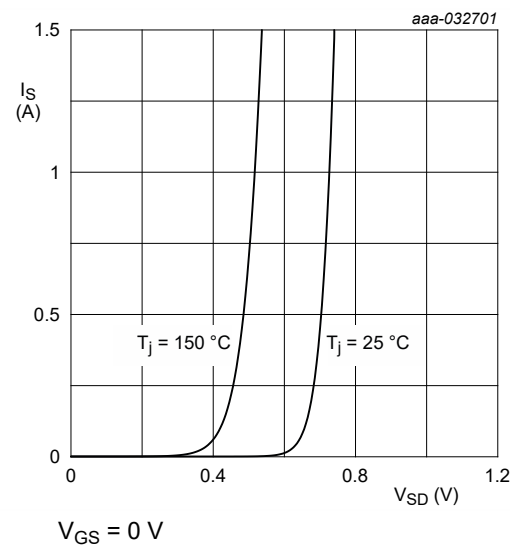


Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

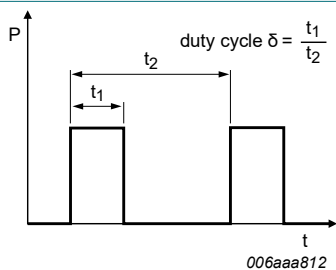


Fig. 18. Duty cycle definition

12. Package outline

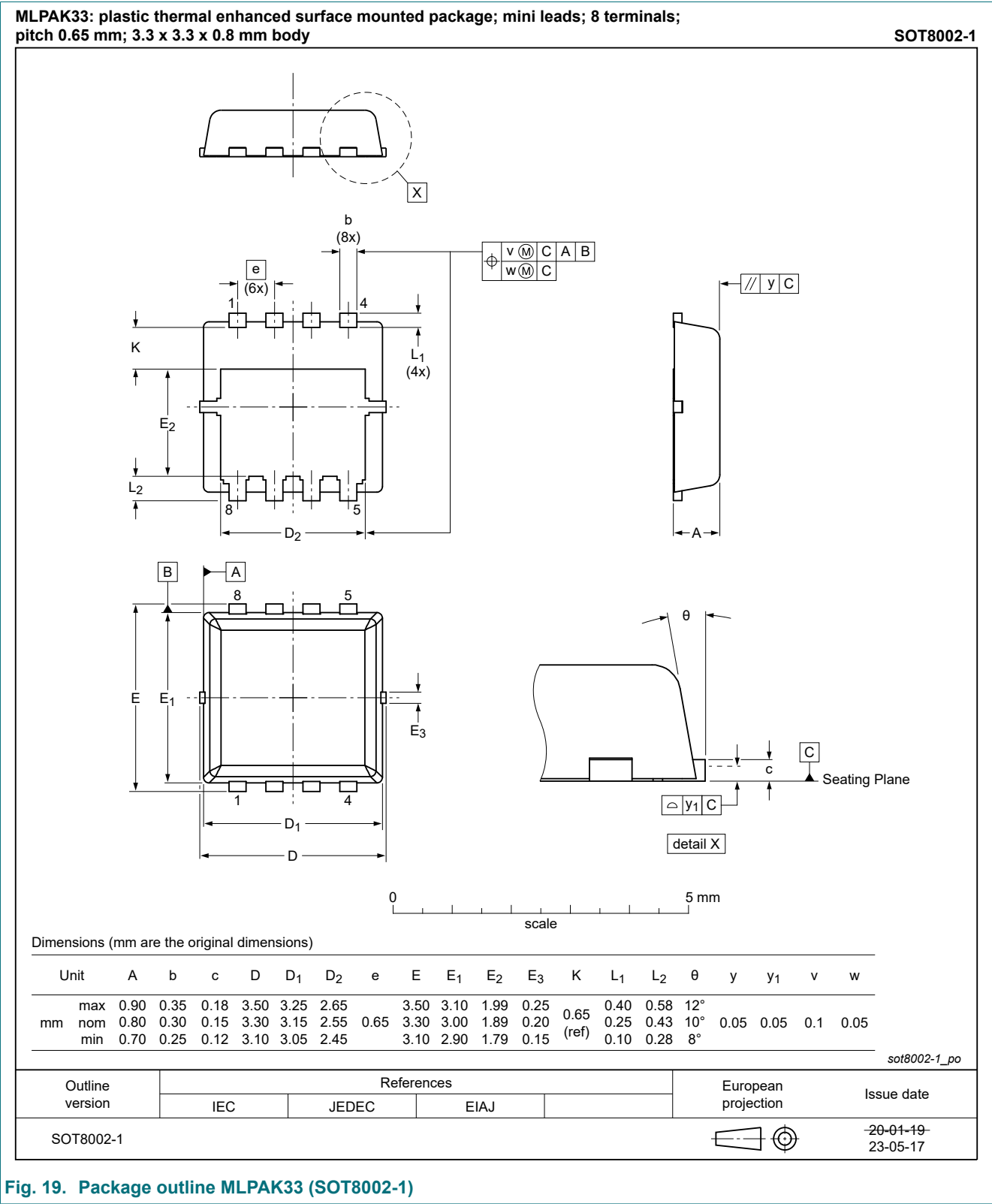


Fig. 19. Package outline MLPAK33 (SOT8002-1)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PXN9R0-30QL v.2	20230731	Product data sheet	-	PXN9R0-30QL v.1
Modifications:	• Chapter "Package outline": drawing update			
PXN9R0-30QL v.1	20210105	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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