HEF4104B-Q100

Quad low-to-high voltage translator with 3-state outputs

Rev. 3 — 25 July 2024 Product data sheet

1. General description

The HEF4104B-Q100 is a quad low-to-high voltage translator with complementary 3-state outputs (Bn and $\overline{Bn}$). A LOW on the output enable input (OE) causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
  - Specified from -40 °C to +85 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4104BT-Q100	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram

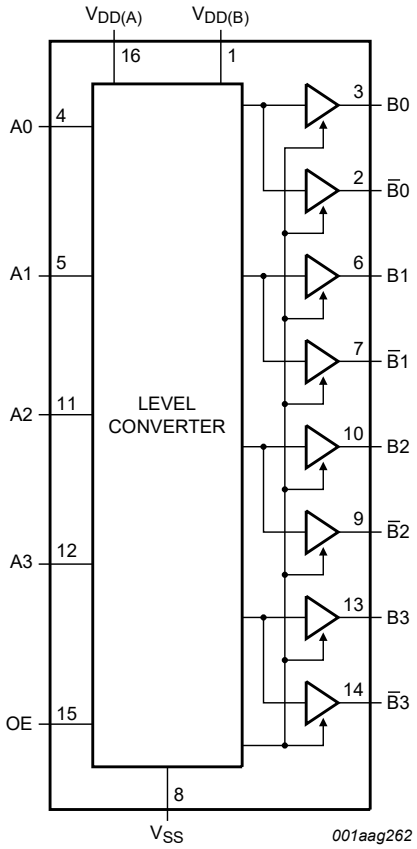


Fig. 1. Logic symbol

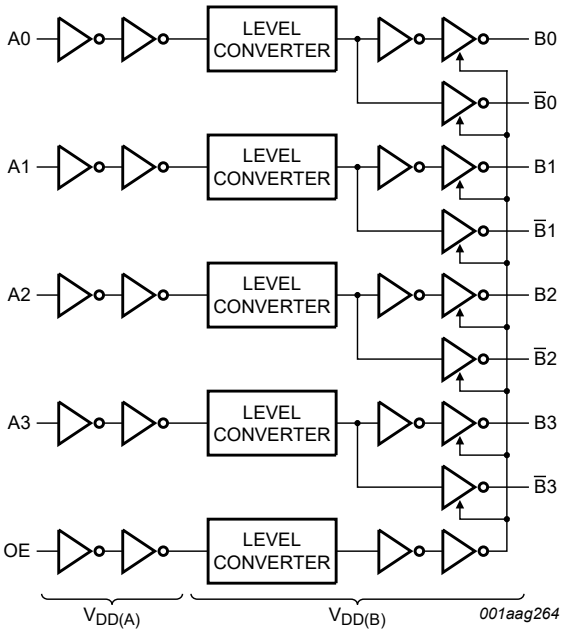


Fig. 2. Logic diagram

5. Pinning information

5.1. Pinning

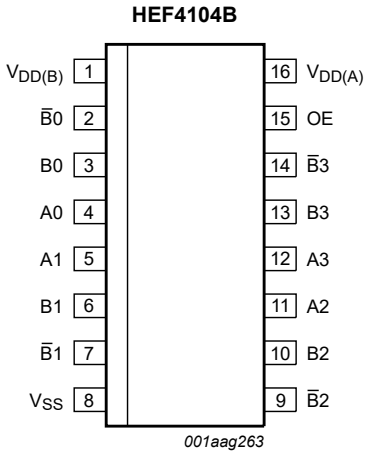


Fig. 3. Pin configuration for SOT109-1 (SO16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{DD(B)}$	1	supply voltage port B
$\overline{B}0$, $\overline{B}1$, $\overline{B}2$, $\overline{B}3$	2, 7, 9, 14	complementary data output
B0, B1, B2, B3	3, 6, 10, 13	data output
A0, A1, A2, A3	4, 5, 11, 12	data input
V_{SS}	8	common negative supply voltage (0 V)
OE	15	output enable input
$V_{DD(A)}$	16	supply voltage port A

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Control	Output	
OE	**Bn**	**$\overline{B}$n**
H	An	$\overline{A}$n
L	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(A)}$	supply voltage A	port A; $V_{DD(A)} \leq V_{DD(B)}$	-0.5	+18	V
$V_{DD(B)}$	supply voltage B	port B; $V_{DD(B)} \geq V_{DD(A)}$	-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD(A)} + 0.5$ V	-	±10	mA
V_I	input voltage		-0.5	$V_{DD(A)} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD(B)} + 0.5$ V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current	[1]	-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

[1] I_{DD} is the combined current of $I_{DD(A)}$ and $I_{DD(B)}$.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(A)}$	supply voltage A		3	-	≤ $V_{DD(B)}$	V
$V_{DD(B)}$	supply voltage B		≥ $V_{DD(A)}$	-	15	V
V_I	input voltage		0	-	$V_{DD(A)}$	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	$V_{DD(A)}$ = 5 V	-	-	3.75	μs/V
		$V_{DD(A)}$ = 10 V	-	-	0.5	μs/V
		$V_{DD(A)}$ = 15 V	-	-	0.08	μs/V

9. Static characteristics

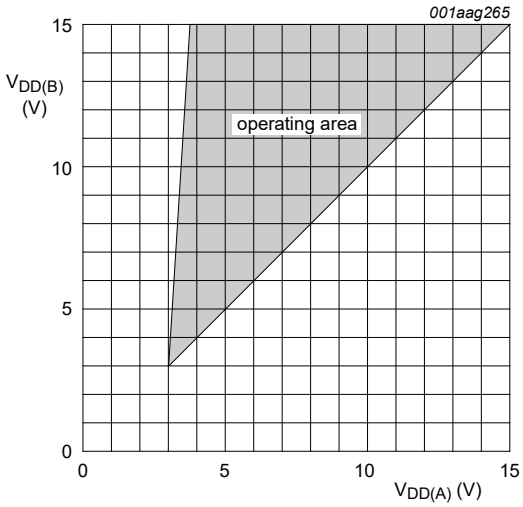
Table 6. Static characteristics

$V_{DD(A)}$ = $V_{DD(B)}$; V_{SS} = 0 V; V_I = V_{SS} or $V_{DD(A)}$; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD} [1]	T_{amb} = -40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V_O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V_O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V_O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I_{DD}	supply current	all valid input combinations; I_O = 0 A	5 V [2]	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
I_{OZ}	OFF-state output current	HIGH; V_O = $V_{DD(B)}$	15 V	-	1.6	-	1.6	-	12.0	μA
		LOW; V_O = V_{SS}	15 V	-	-1.6	-	-1.6	-	-12.0	μA

Symbol	Parameter	Conditions	V_{DD} [1]	T_{amb} = -40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
C_I	input capacitance	digital inputs	-	-	-	-	7.5	-	-	pF

[1] V_{DD} is the same as $V_{DD(A)}$ and $V_{DD(B)}$.
[2] I_{DD} is the combined current of $I_{DD(A)}$ and $I_{DD(B)}$.



The shaded area shows the permissible operating range.

Fig. 4. $V_{DD(B)}$ as a function of $V_{DD(A)}$

10. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = 25 °C unless otherwise specified; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	An to Bn, $\overline{B}$n; see Fig. 5					
		$V_{DD(A)}$ = $V_{DD(B)}$ = 5 V	143 ns + (0.55 ns/pF)C_L	-	170	340	ns
		$V_{DD(A)}$ = $V_{DD(B)}$ = 10 V	69 ns + (0.23 ns/pF)C_L	-	80	160	ns
		$V_{DD(A)}$ = $V_{DD(B)}$ = 15 V	57 ns + (0.16 ns/pF)C_L	-	65	135	ns
t_{PLH}	LOW to HIGH propagation delay	An to Bn, $\overline{B}$n; see Fig. 5					
		$V_{DD(A)}$ = $V_{DD(B)}$ = 5 V	143 ns + (0.55 ns/pF)C_L	-	170	340	ns
		$V_{DD(A)}$ = $V_{DD(B)}$ = 10 V	69 ns + (0.23 ns/pF)C_L	-	80	160	ns
		$V_{DD(A)}$ = $V_{DD(B)}$ = 15 V	62 ns + (0.16 ns/pF)C_L	-	70	140	ns
t_{THL}	HIGH to LOW output transition time	Bn or $\overline{B}$n; see Fig. 6					
		$V_{DD(A)}$ = $V_{DD(B)}$ = 5 V	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
		$V_{DD(A)}$ = $V_{DD(B)}$ = 10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
		$V_{DD(A)}$ = $V_{DD(B)}$ = 15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_{TLH}	LOW to HIGH output transition time	Bn or $\overline{B}$n; see Fig. 6					
		$V_{DD(A)}$ = $V_{DD(B)}$ = 5 V	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
		$V_{DD(A)}$ = $V_{DD(B)}$ = 10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
		$V_{DD(A)}$ = $V_{DD(B)}$ = 15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns

Symbol	Parameter	Conditions	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHZ}	HIGH to OFF-state propagation delay	OE to Bn, $\overline{Bn}$; see Fig. 6					
		$V_{DD(A)} = V_{DD(B)} = 5$ V		-	70	135	ns
		$V_{DD(A)} = V_{DD(B)} = 10$ V		-	55	110	ns
		$V_{DD(A)} = V_{DD(B)} = 15$ V		-	60	120	ns
t_{PLZ}	LOW to OFF-state propagation delay	OE to Bn, $\overline{Bn}$; see Fig. 6					
		$V_{DD(A)} = V_{DD(B)} = 5$ V		-	70	135	ns
		$V_{DD(A)} = V_{DD(B)} = 10$ V		-	55	105	ns
		$V_{DD(A)} = V_{DD(B)} = 15$ V		-	55	110	ns
t_{PZH}	OFF-state to HIGH propagation delay	OE to Bn, $\overline{Bn}$; see Fig. 6					
		$V_{DD(A)} = V_{DD(B)} = 5$ V		-	195	395	ns
		$V_{DD(A)} = V_{DD(B)} = 10$ V		-	95	195	ns
		$V_{DD(A)} = V_{DD(B)} = 15$ V		-	80	165	ns
t_{PZL}	OFF-state to LOW propagation delay	OE to Bn, $\overline{Bn}$; see Fig. 6					
		$V_{DD(A)} = V_{DD(B)} = 5$ V		-	195	395	ns
		$V_{DD(A)} = V_{DD(B)} = 10$ V		-	95	190	ns
		$V_{DD(A)} = V_{DD(B)} = 15$ V		-	80	160	ns

[1] Typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

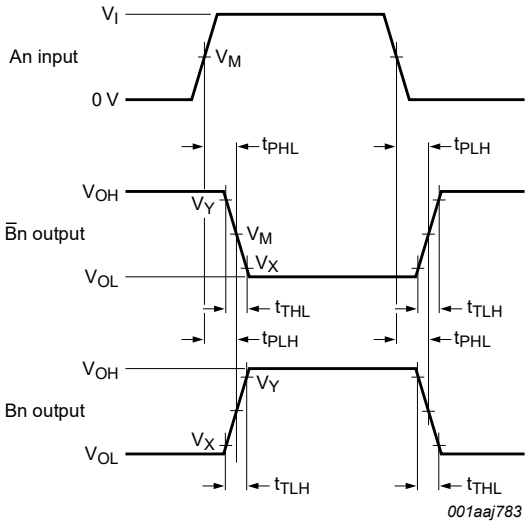
Table 8. Dynamic power dissipation

$V_{DD(A)} = V_{DD(B)}$; $V_{SS} = 0$ V; $t_r = t_f \leq 20$ ns; $T_{amb} = 25$ °C.

Symbol	Parameter	V_{DD} [1]	Typical formula (µW)	where
P_D	dynamic power dissipation	5 V	$P_D = 3000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.
		10 V	$P_D = 12200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 31000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

[1] V_{DD} is the same as $V_{DD(A)}$ and $V_{DD(B)}$.

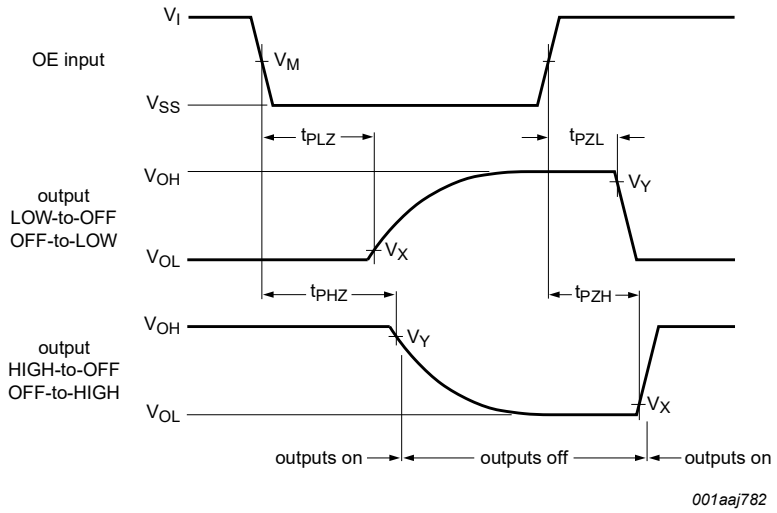
10.1. Waveforms and test circuit



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Data input (An) to data output (Bn, $\overline{B}n$) propagation delays and output transition times



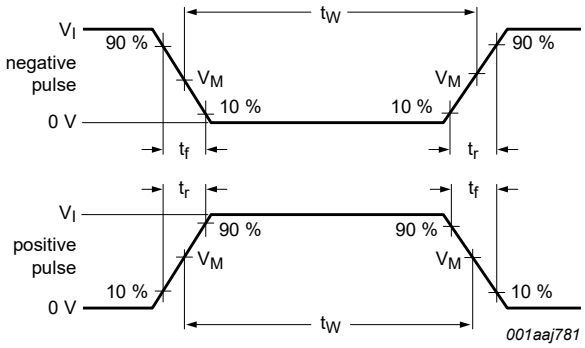
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

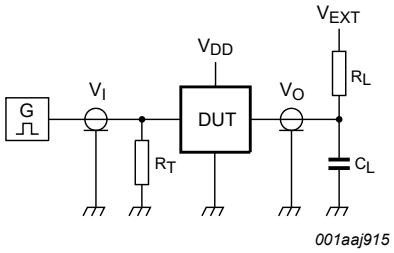
Fig. 6. Enable and disable times

Table 9. Measurement points

Input		Output		
V_I	V_M	V_M	V_X	V_Y
V_{SS} or $V_{DD(A)}$	$0.5V_{DD(A)}$	$0.5V_{DD(B)}$	$0.1V_{DD(B)}$	$0.9V_{DD(B)}$



a. Input waveforms



b. Test circuit

Test data given in Table 10.

Definitions test circuit:

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

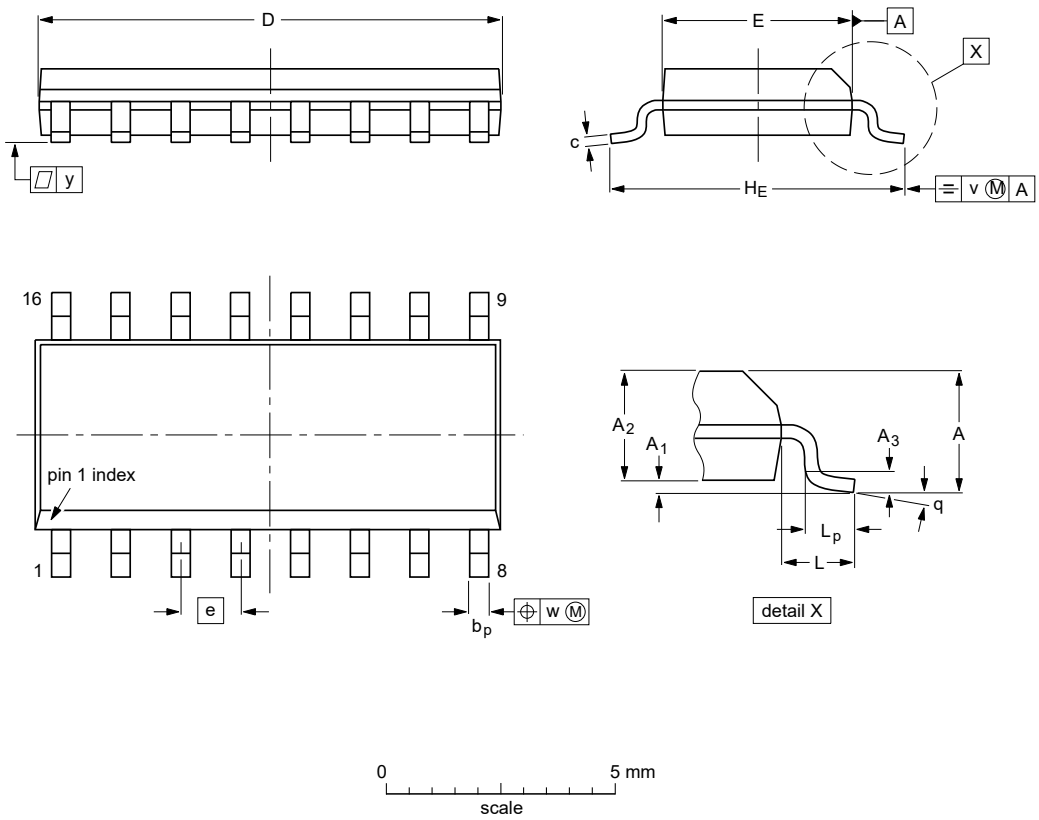
Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Supplies	Input	Load		V_{EXT}		
$V_{DD(A)} = V_{DD(B)}$	t_r, t_f	R_L	C_L	t_{PHL}, t_{PLH}	t_{PZL}, t_{PLZ}	t_{PZH}, t_{PHZ}
5 V to 15 V	≤ 20 ns	1 kΩ	50 pF	open	$V_{DD(B)}$	V_{SS}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 8. Package outline SOT109-1 (SO16)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4104B_Q100 v.3	20240725	Product data sheet	-	HEF4104B_Q100 v.2
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 8: Aligned SO package outline drawing to JEDEC MS-012.			
HEF4104B_Q100 v.2	20211214	Product data sheet	-	HEF4104B_Q100 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Section 12 added.			
HEF4104B_Q100 v.1	20140324	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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