



PSMN8R7-80BS

N-channel 80 V 8.7 mΩ standard level MOSFET in D2PAK

Rev. 2 — 2 March 2012

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

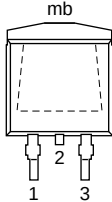
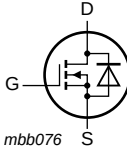
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	80	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1	-	-	90	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	170	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; T _j = 100 °C; see Figure 12	-	-	14	mΩ
		V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C; see Figure 13	-	7.5	8.7	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 40 V; see Figure 14 ; see Figure 15	-	11	-	nC
Q _{G(tot)}	total gate charge		-	52	-	nC
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(initial)} = 25 °C; I _D = 90 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; unclamped	-	-	120	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN8R7-80BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	80	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	80	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	64	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	-	90	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3	-	361	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	170	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	90	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	361	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 90\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	120	mJ

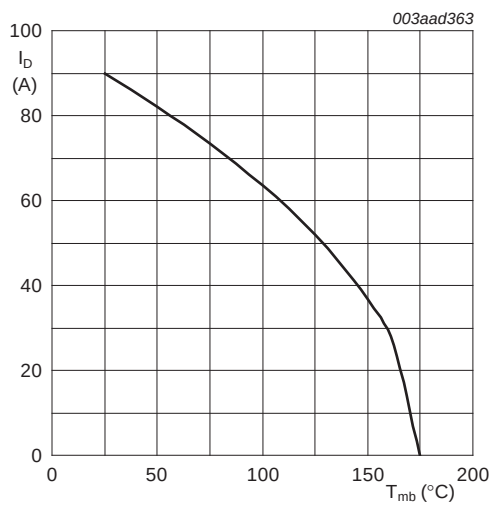
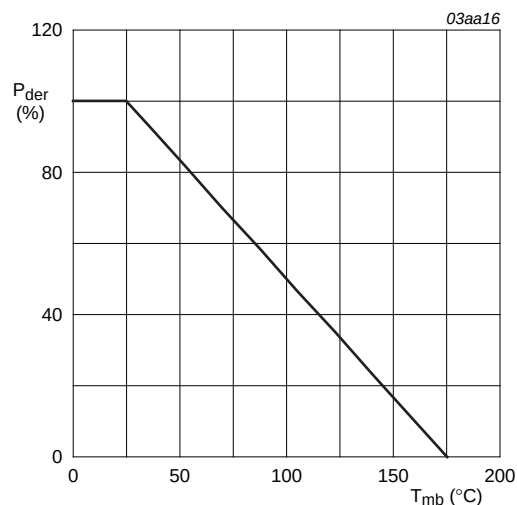


Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

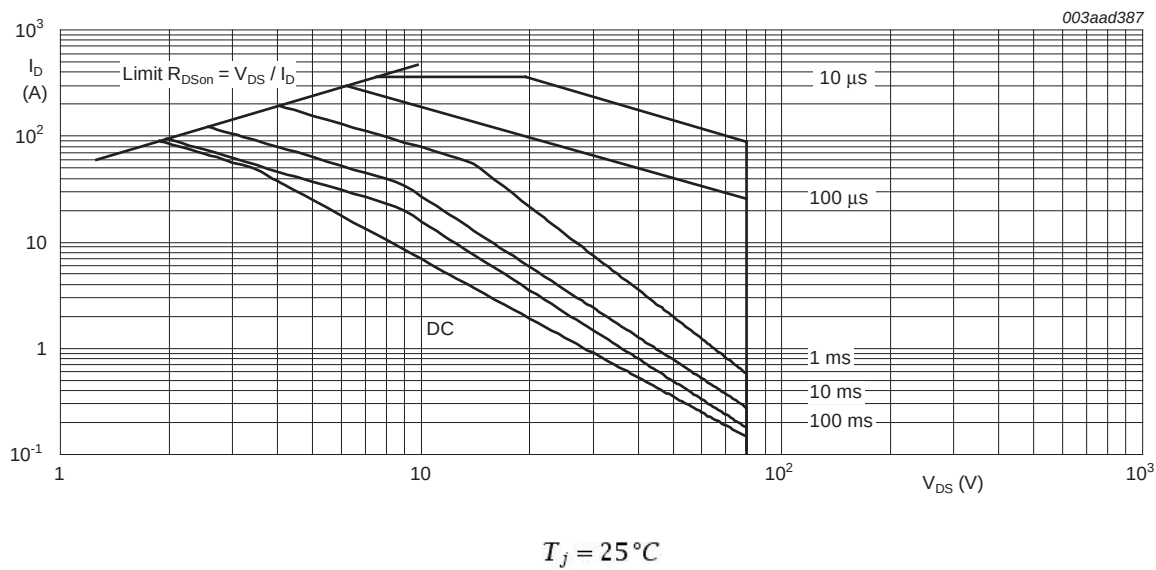
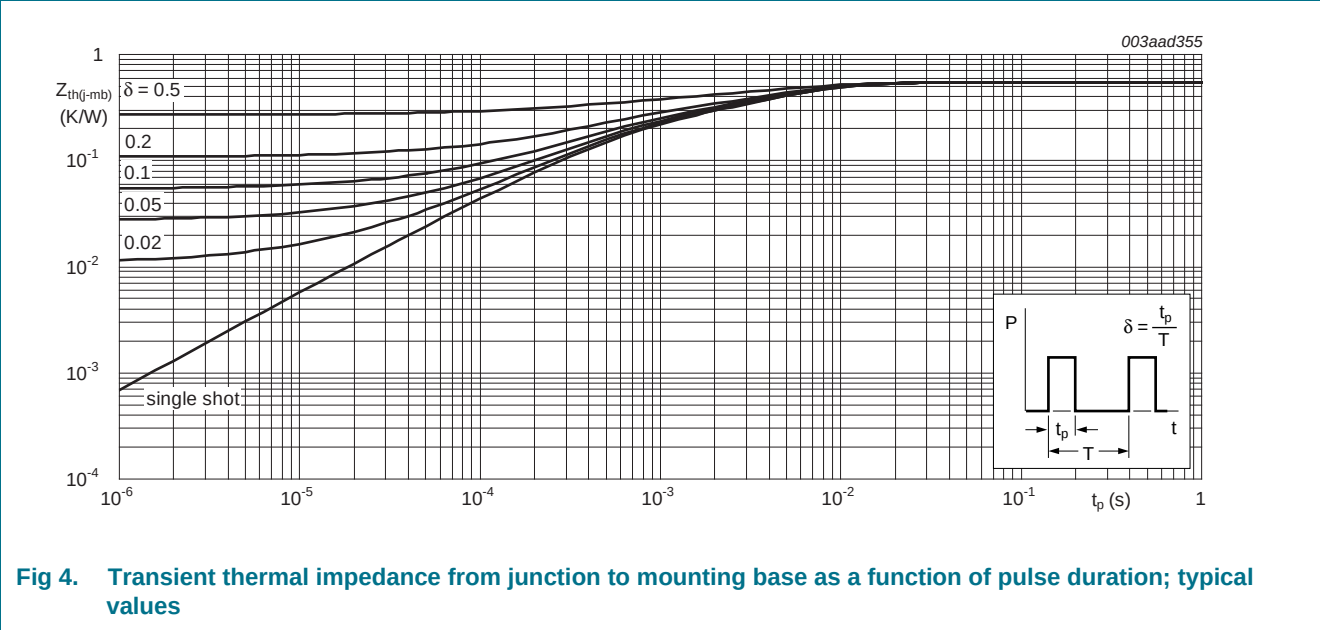


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.54	0.88	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W



6. Characteristics

Table 6. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = -55 ^\circ C$	73	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = 175 ^\circ C$; see Figure 10	1	-	-	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = -55 ^\circ C$; see Figure 10	-	-	4.6	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = 25 ^\circ C$; see Figure 11 ; see Figure 10	2.3	3	4	V
I_{DSS}	drain leakage current	$V_{DS} = 80 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	0.3	5	μA
		$V_{DS} = 80 V$; $V_{GS} = 0 V$; $T_j = 125 ^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	10	100	nA
		$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 10 A$; $T_j = 175 ^\circ C$; see Figure 12	-	-	20.88	mΩ
		$V_{GS} = 10 V$; $I_D = 10 A$; $T_j = 100 ^\circ C$; see Figure 12	-	-	14	mΩ
		$V_{GS} = 10 V$; $I_D = 10 A$; $T_j = 25 ^\circ C$; see Figure 13	-	7.5	8.7	mΩ
R_G	internal gate resistance (AC)	$f = 1 MHz$	-	1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 0 A$; $V_{DS} = 0 V$; $V_{GS} = 10 V$	-	44	-	nC
		$I_D = 25 A$; $V_{DS} = 40 V$; $V_{GS} = 10 V$; see Figure 14 ; see Figure 15	-	52	-	nC
Q_{GS}	gate-source charge		-	15	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 25 A$; $V_{DS} = 40 V$; $V_{GS} = 10 V$; see Figure 14	-	9.2	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	5.8	-	nC
Q_{GD}	gate-drain charge	$I_D = 25 A$; $V_{DS} = 40 V$; $V_{GS} = 10 V$; see Figure 14 ; see Figure 15	-	11	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A$; $V_{DS} = 40 V$; see Figure 15	-	4.6	-	V
C_{iss}	input capacitance	$V_{DS} = 40 V$; $V_{GS} = 0 V$; $f = 1 MHz$; $T_j = 25 ^\circ C$; see Figure 16	-	3346	-	pF
C_{oss}	output capacitance		-	296	-	pF
C_{rss}	reverse transfer capacitance		-	158	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 V$; $R_L = 1.6 \Omega$; $V_{GS} = 10 V$; $R_{G(ext)} = 4.7 \Omega$	-	21	-	ns
t_r	rise time		-	26	-	ns
$t_{d(off)}$	turn-off delay time		-	46	-	ns
t_f	fall time		-	20	-	ns

Table 6. Characteristics ...continued
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ °C}$; see Figure 17	-	0.79	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = 100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	42	-	ns
Q_r	recovered charge	$V_{DS} = 40\text{ V}$	-	66	-	nC

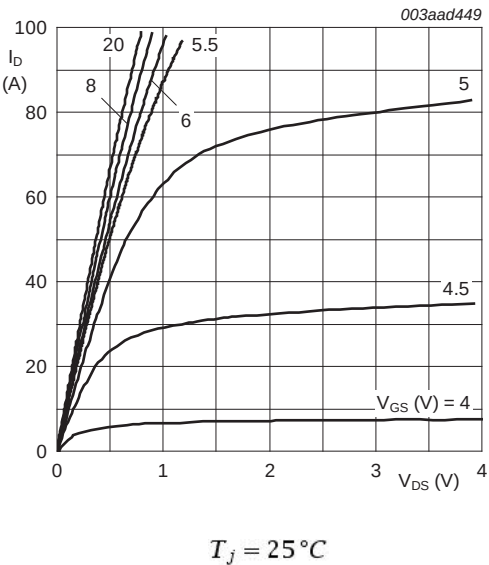


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

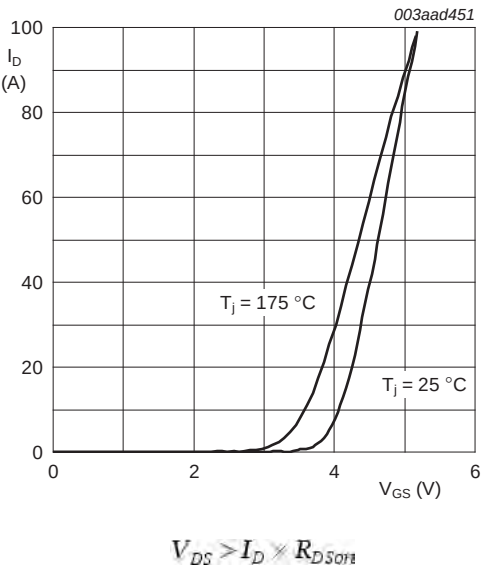


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

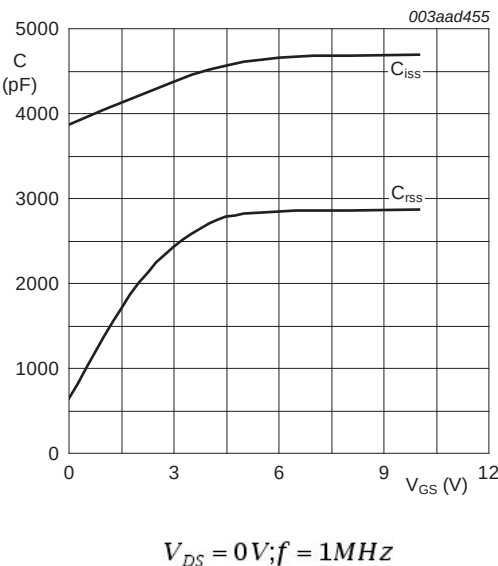


Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

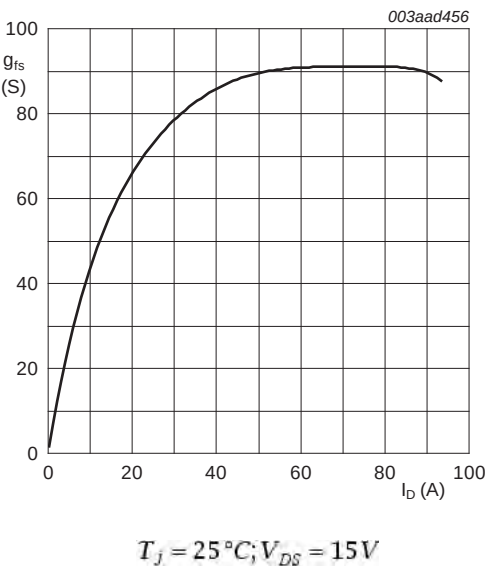
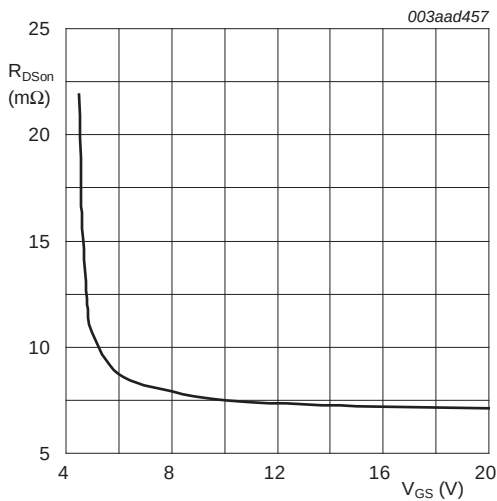
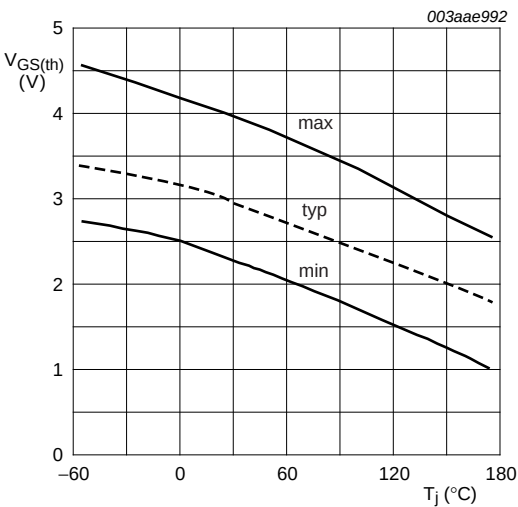


Fig 8. Forward transconductance as a function of drain current; typical values



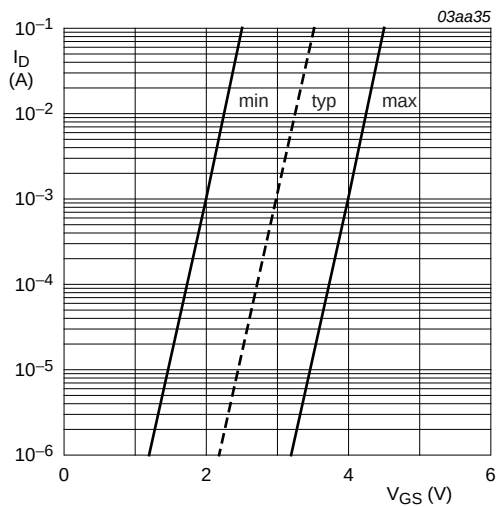
$T_j = 25\text{ }^{\circ}\text{C}; I_D = 25\text{ A}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



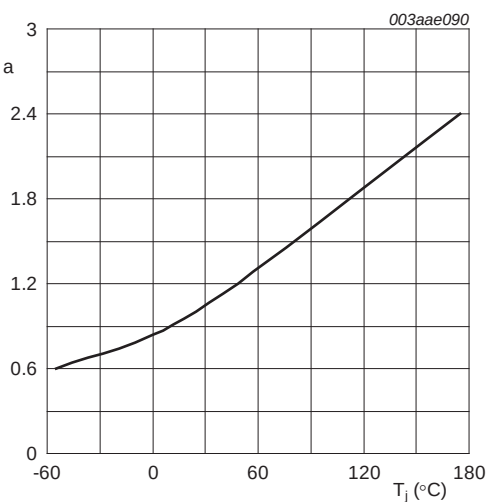
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ }^{\circ}\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

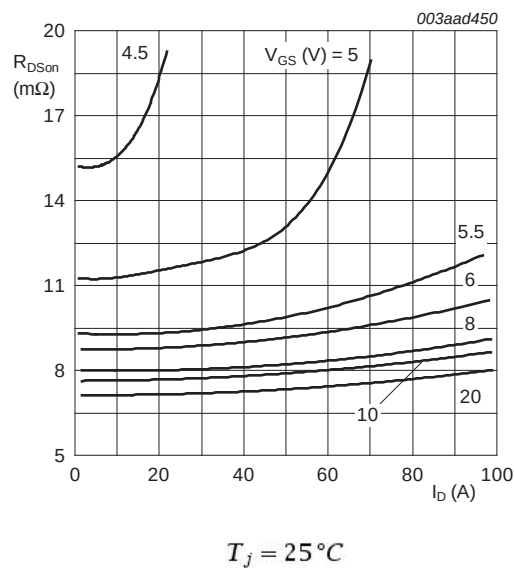


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

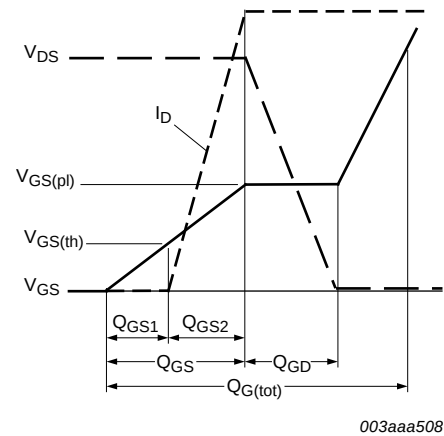


Fig 14. Gate charge waveform definitions

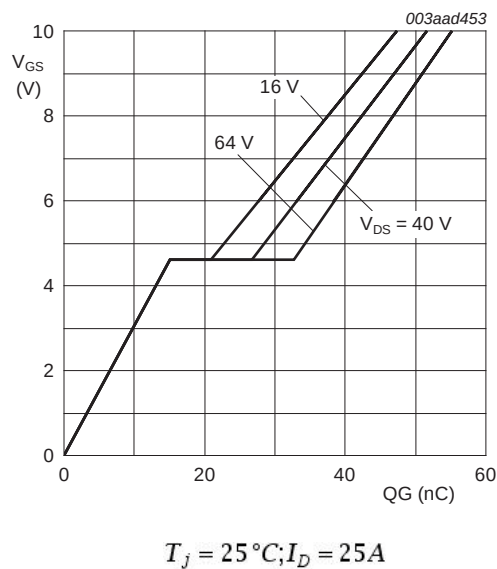


Fig 15. Gate-source voltage as a function of gate charge; typical values

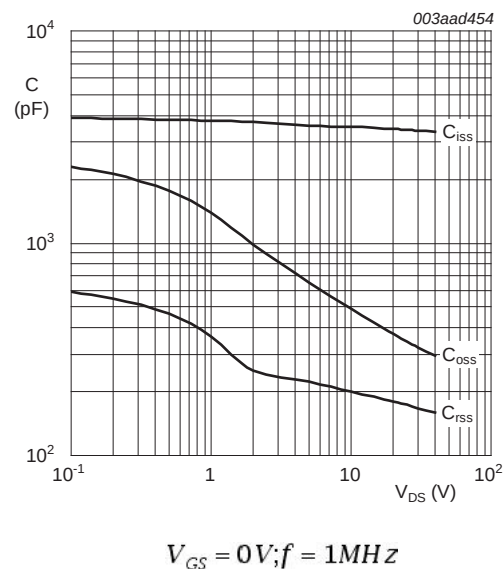


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

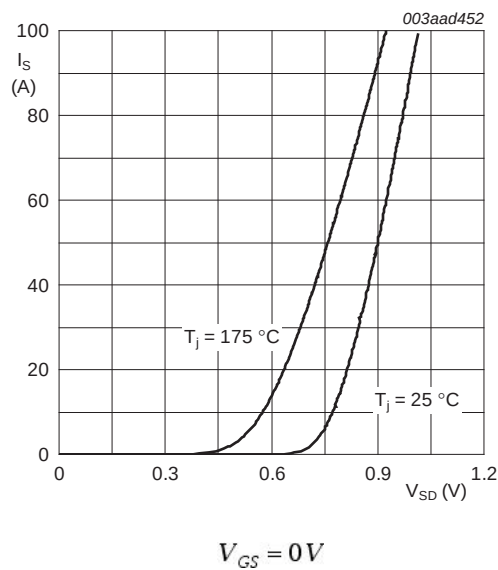
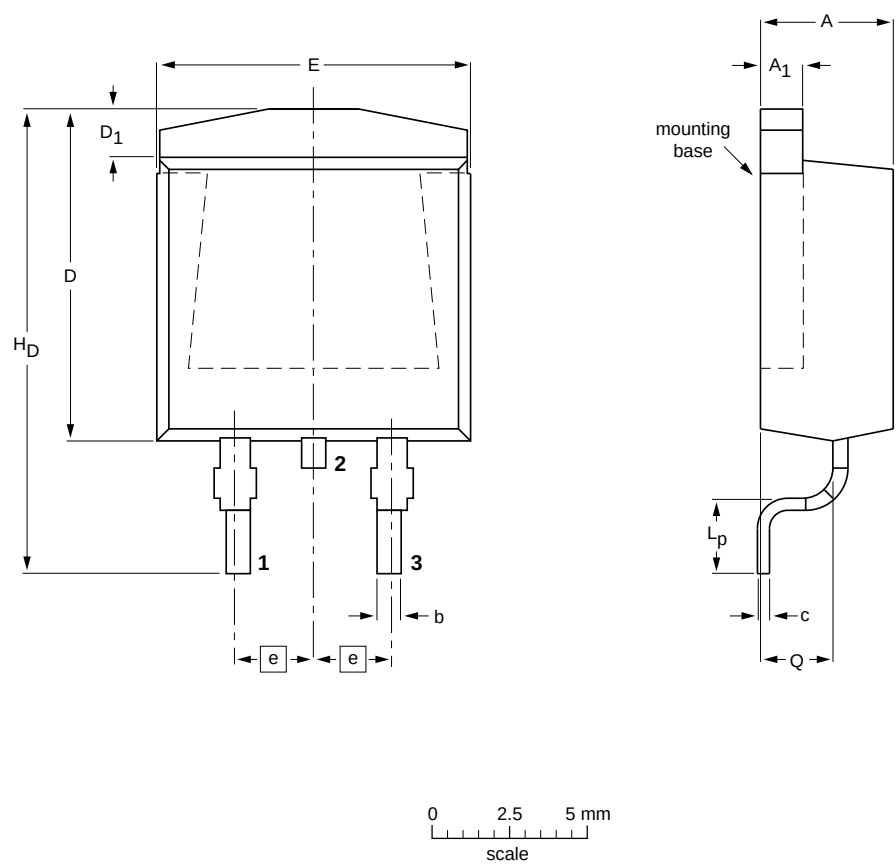


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

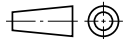
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 18. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN8R7-80BS v.2	20120302	Product data sheet	-	PSMN8R7-80BS v.1
Modifications:	- Status changed from objective to product. - Various changes to content.			
PSMN8R7-80BS v.1	20111024	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
6	Characteristics	5
7	Package outline	10
8	Revision history	11
9	Legal information	12
9.1	Data sheet status	12
9.2	Definitions	12
9.3	Disclaimers	12
9.4	Trademarks	13
10	Contact information	13

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