

# 74AUP1T97-Q100

Low-power configurable gate with voltage-level translator

Rev. 4 — 17 July 2023

Product data sheet

## 1. General description

The 74AUP1T97-Q100 is a configurable multiple function gate with level translating, Schmitt-trigger inputs. The device can be configured as any of the following logic functions MUX, AND, OR, NAND, NOR, inverter and buffer; using the 3-bit input. All inputs can be connected directly to  $V_{CC}$  or GND. Low threshold Schmitt trigger inputs allow these devices to be driven by 1.8 V logic levels in 3.3 V applications. This device ensures very low static and dynamic power consumption across the entire  $V_{CC}$  range from 2.3 V to 3.6 V. This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.3 V to 3.6 V
- CMOS low power dissipation
- High noise immunity
- Overvoltage tolerant inputs to 3.6 V
- Low noise overshoot and undershoot < 10 % of  $V_{CC}$
- $I_{OFF}$  circuitry provides partial power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Low static power consumption;  $I_{CC} = 1.5 \mu\text{A}$  (maximum)
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">74AUP1T97GW-Q100</a>	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	<a href="#">SOT363-2</a>

### 4. Marking

Table 2. Marking

Type number	Marking code[1]
74AUP1T97GW-Q100	59

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram

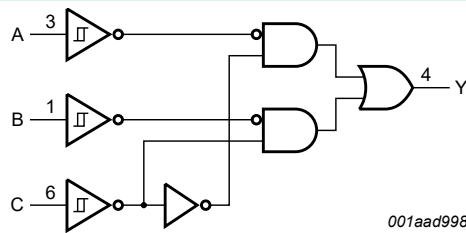


Fig. 1. Logic symbol

## 6. Pinning information

### 6.1. Pinning

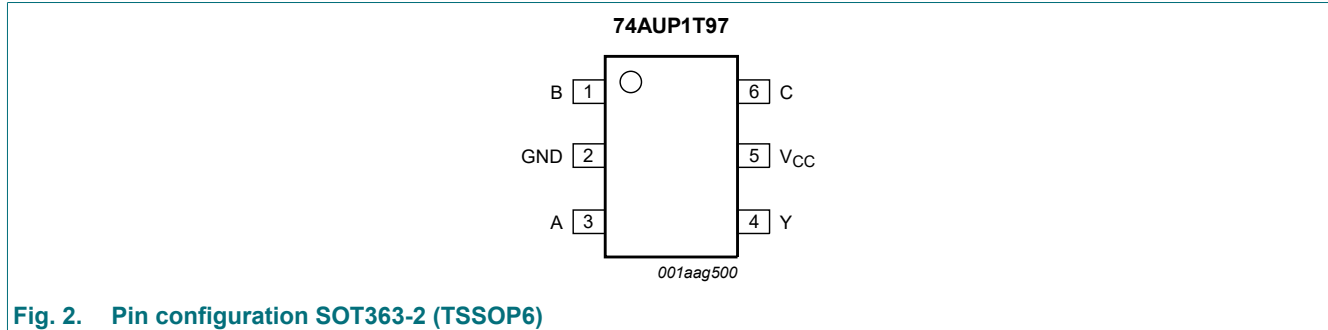


Fig. 2. Pin configuration SOT363-2 (TSSOP6)

### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
GND	2	ground (0 V)
A	3	data input
Y	4	data output
V <sub>CC</sub>	5	supply voltage
C	6	data input

## 7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input			Output
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

7.1. Logic configurations

Table 5. Function selection table

Logic function	Figure
2-input MUX	see Fig. 3
2-input AND	see Fig. 4
2-input OR with one input inverted	see Fig. 5
2-input NAND with one input inverted	see Fig. 5
2-input AND with one input inverted	see Fig. 6
2-input NOR with one input inverted	see Fig. 6
2-input OR	see Fig. 7
Inverter	see Fig. 8
Buffer	see Fig. 9

**Fig. 3. 2-input MUX**

**Fig. 4. 2-input AND gate**

**Fig. 5. 2-input NAND gate with input A inverted or 2-input OR gate with input C inverted**

**Fig. 6. 2-input NOR gate with input B inverted or 2-input AND gate with input C inverted**

**Fig. 7. 2-input OR gate**

**Fig. 8. Inverter**

**Fig. 9. Buffer**

## 8. Limiting values

**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$V_O$	output voltage	Active mode and Power-down mode	[1] -0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±20	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT363-2 (TSSOP6) package:  $P_{tot}$  derates linearly with 3.7 mW/K above 83 °C.

## 9. Recommended operating conditions

**Table 7. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		2.3	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	Active mode	0	$V_{CC}$	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
$T_{amb}$	ambient temperature		-40	+125	°C

## 10. Static characteristics

**Table 8. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = 25 °C</b>						
V <sub>T+</sub>	positive-going threshold voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.60	-	1.10	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.75	-	1.16	V
V <sub>T-</sub>	negative-going threshold voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.35	-	0.60	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.50	-	0.85	V
V <sub>H</sub>	hysteresis voltage	(V <sub>H</sub> = V <sub>T+</sub> - V <sub>T-</sub> )				
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.23	-	0.60	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.25	-	0.56	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.3 V to 3.6 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -2.3 mA; V <sub>CC</sub> = 2.3 V	2.05	-	-	V
		I <sub>O</sub> = -3.1 mA; V <sub>CC</sub> = 2.3 V	1.9	-	-	V
		I <sub>O</sub> = -2.7 mA; V <sub>CC</sub> = 3.0 V	2.72	-	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.6	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.3 V to 3.6 V	-	-	0.10	V
		I <sub>O</sub> = 2.3 mA; V <sub>CC</sub> = 2.3 V	-	-	0.31	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.44	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.31	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.44	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = GND to 3.6 V; V <sub>CC</sub> = 0 V to 3.6 V	-	-	±0.1	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V	-	-	±0.1	μA
ΔI <sub>OFF</sub>	additional power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V to 0.2 V	-	-	±0.2	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.3 V to 3.6 V	-	-	1.2	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	0.8	-	pF
C <sub>O</sub>	output capacitance	V <sub>O</sub> = GND; V <sub>CC</sub> = 0 V	-	1.7	-	pF

## Low-power configurable gate with voltage-level translator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>T+</sub>	positive-going threshold voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.60	-	1.10	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.75	-	1.19	V
V <sub>T-</sub>	negative-going threshold voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.35	-	0.60	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.50	-	0.85	V
V <sub>H</sub>	hysteresis voltage	(V <sub>H</sub> = V <sub>T+</sub> - V <sub>T-</sub> )				
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.10	-	0.60	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.15	-	0.56	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.3 V to 3.6 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -2.3 mA; V <sub>CC</sub> = 2.3 V	1.97	-	-	V
		I <sub>O</sub> = -3.1 mA; V <sub>CC</sub> = 2.3 V	1.85	-	-	V
		I <sub>O</sub> = -2.7 mA; V <sub>CC</sub> = 3.0 V	2.67	-	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.55	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.3 V to 3.6 V	-	-	0.1	V
		I <sub>O</sub> = 2.3 mA; V <sub>CC</sub> = 2.3 V	-	-	0.33	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.45	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.33	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.45	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = GND to 3.6 V; V <sub>CC</sub> = 0 V to 3.6 V	-	-	±0.5	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V	-	-	±0.5	μA
ΔI <sub>OFF</sub>	additional power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V to 0.2 V	-	-	±0.5	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.3 V to 3.6 V	-	-	1.5	μA
ΔI <sub>CC</sub>	additional supply current	V <sub>CC</sub> = 2.3 V to 2.7 V; I <sub>O</sub> = 0 A [1]	-	-	4	μA
		V <sub>CC</sub> = 3.0 V to 3.6 V; I <sub>O</sub> = 0 A [2]	-	-	12	μA

## Low-power configurable gate with voltage-level translator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>T+</sub>	positive-going threshold voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.60	-	1.10	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.75	-	1.19	V
V <sub>T-</sub>	negative-going threshold voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0.33	-	0.64	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.46	-	0.85	V
V <sub>H</sub>	hysteresis voltage	(V <sub>H</sub> = V <sub>T+</sub> - V <sub>T-</sub> )				
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.10	-	0.60	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.15	-	0.56	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.3 V to 3.6 V	V <sub>CC</sub> - 0.11	-	-	V
		I <sub>O</sub> = -2.3 mA; V <sub>CC</sub> = 2.3 V	1.77	-	-	V
		I <sub>O</sub> = -3.1 mA; V <sub>CC</sub> = 2.3 V	1.67	-	-	V
		I <sub>O</sub> = -2.7 mA; V <sub>CC</sub> = 3.0 V	2.40	-	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.30	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>T+</sub> or V <sub>T-</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.3 V to 3.6 V	-	-	0.11	V
		I <sub>O</sub> = 2.3 mA; V <sub>CC</sub> = 2.3 V	-	-	0.36	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.50	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.50	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = GND to 3.6 V; V <sub>CC</sub> = 0 V to 3.6 V	-	-	±0.75	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V	-	-	±0.75	μA
ΔI <sub>OFF</sub>	additional power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V to 0.2 V	-	-	±0.75	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.3 V to 3.6 V	-	-	3.5	μA
ΔI <sub>CC</sub>	additional supply current	V <sub>CC</sub> = 2.3 V to 2.7 V; I <sub>O</sub> = 0 A [1]	-	-	7	μA
		V <sub>CC</sub> = 3.0 V to 3.6 V; I <sub>O</sub> = 0 A [2]	-	-	22	μA

[1] One input at 0.3 V or 1.1 V, other input at V<sub>CC</sub> or GND.

[2] One input at 0.45 V or 1.2 V, other input at V<sub>CC</sub> or GND.



## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
<b>V<sub>CC</sub> = 2.3 V to 2.7 V; V<sub>I</sub> = 1.65 V to 1.95 V</b>										
t <sub>pd</sub>	propagation delay	A, B, C to Y; see Fig. 10 [2]								
		C <sub>L</sub> = 5 pF	2.2	3.5	5.5	0.5	6.8	0.5	7.5	ns
		C <sub>L</sub> = 10 pF	2.6	4.1	6.3	1.0	7.9	1.0	8.7	ns
		C <sub>L</sub> = 15 pF	2.9	4.6	6.9	1.0	8.7	1.0	9.6	ns
		C <sub>L</sub> = 30 pF	3.7	5.8	8.4	1.5	10.8	1.5	11.9	ns
<b>V<sub>CC</sub> = 2.3 V to 2.7 V; V<sub>I</sub> = 2.3 V to 2.7 V</b>										
t <sub>pd</sub>	propagation delay	A, B, C to Y; see Fig. 10 [2]								
		C <sub>L</sub> = 5 pF	1.8	3.4	5.5	0.5	6.0	0.5	6.6	ns
		C <sub>L</sub> = 10 pF	2.2	4.0	6.2	1.0	7.1	1.0	7.9	ns
		C <sub>L</sub> = 15 pF	2.5	4.4	6.8	1.0	7.9	1.0	8.7	ns
		C <sub>L</sub> = 30 pF	3.2	5.6	8.3	1.5	10.0	1.5	11.0	ns
<b>V<sub>CC</sub> = 2.3 V to 2.7 V; V<sub>I</sub> = 3.0 V to 3.6 V</b>										
t <sub>pd</sub>	propagation delay	A, B, C to Y; see Fig. 10 [2]								
		C <sub>L</sub> = 5 pF	1.4	3.1	5.0	0.5	5.5	0.5	6.1	ns
		C <sub>L</sub> = 10 pF	1.8	3.7	5.7	1.0	6.5	1.0	7.2	ns
		C <sub>L</sub> = 15 pF	2.2	4.2	6.3	1.0	7.4	1.0	8.2	ns
		C <sub>L</sub> = 30 pF	2.9	5.3	7.9	1.5	9.5	1.5	10.5	ns
<b>V<sub>CC</sub> = 3.0 V to 3.6 V; V<sub>I</sub> = 1.65 V to 1.95 V</b>										
t <sub>pd</sub>	propagation delay	A, B, C to Y; see Fig. 10 [2]								
		C <sub>L</sub> = 5 pF	2.1	2.9	3.9	0.5	8.0	0.5	8.8	ns
		C <sub>L</sub> = 10 pF	2.5	3.4	4.6	1.0	8.5	1.0	9.4	ns
		C <sub>L</sub> = 15 pF	2.9	3.9	5.2	1.0	9.1	1.0	10.1	ns
		C <sub>L</sub> = 30 pF	3.6	5.0	6.7	1.5	9.8	1.5	10.8	ns
<b>V<sub>CC</sub> = 3.0 V to 3.6 V; V<sub>I</sub> = 2.3 V to 2.7 V</b>										
t <sub>pd</sub>	propagation delay	A, B, C to Y; see Fig. 10 [2]								
		C <sub>L</sub> = 5 pF	1.7	2.8	4.2	0.5	5.3	0.5	5.9	ns
		C <sub>L</sub> = 10 pF	2.1	3.4	5.0	1.0	6.1	1.0	6.8	ns
		C <sub>L</sub> = 15 pF	2.4	3.8	5.6	1.0	6.8	1.0	7.5	ns
		C <sub>L</sub> = 30 pF	3.2	5.0	7.1	1.5	8.5	1.5	9.4	ns
<b>V<sub>CC</sub> = 3.0 V to 3.6 V; V<sub>I</sub> = 3.0 V to 3.6 V</b>										
t <sub>pd</sub>	propagation delay	A, B, C to Y; see Fig. 10 [2]								
		C <sub>L</sub> = 5 pF	1.4	2.7	4.2	0.5	4.7	0.5	5.2	ns
		C <sub>L</sub> = 10 pF	1.8	3.3	5.0	1.0	5.7	1.0	6.3	ns
		C <sub>L</sub> = 15 pF	2.1	3.8	5.6	1.0	6.2	1.0	6.9	ns
		C <sub>L</sub> = 30 pF	2.9	4.9	7.1	1.5	7.8	1.5	8.6	ns

Low-power configurable gate with voltage-level translator

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
<b>T<sub>amb</sub> = 25 °C</b>										
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [3]								
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	3.6	-	-	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	4.3	-	-	-	-	-	pF

- [1] All typical values are measured at nominal V<sub>CC</sub>.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V;  
 N = number of inputs switching;  
 Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

11.1. Waveform and test circuit

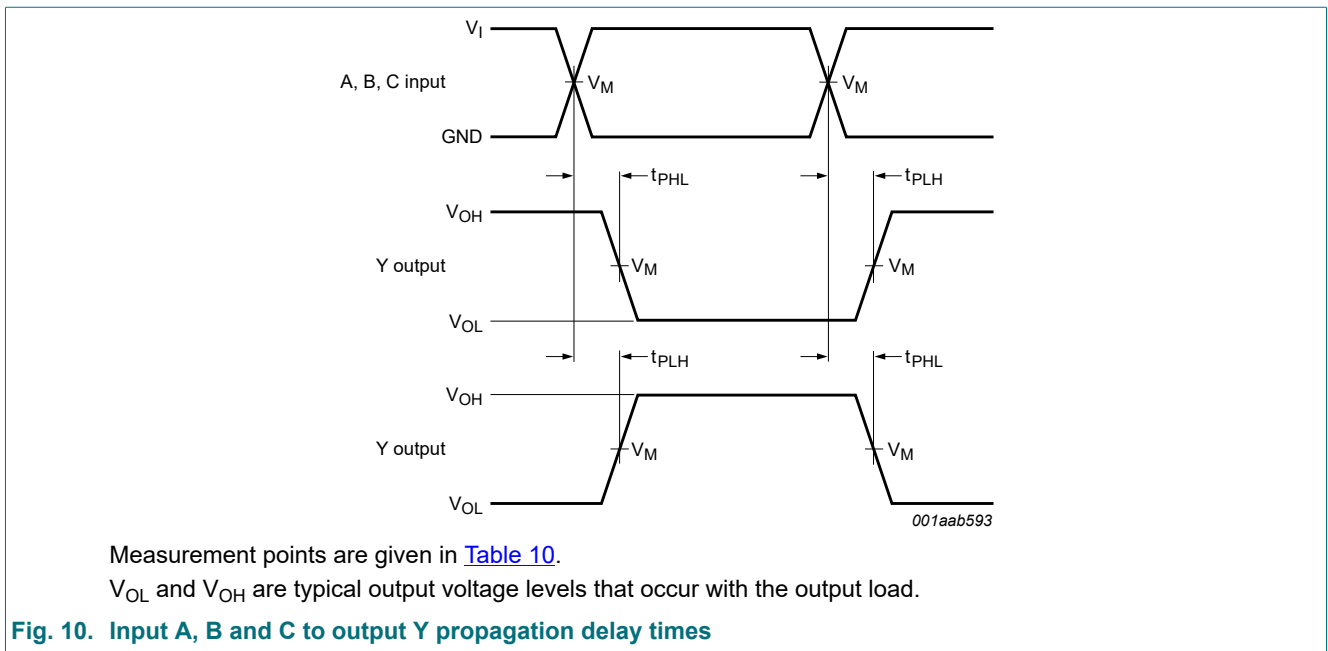
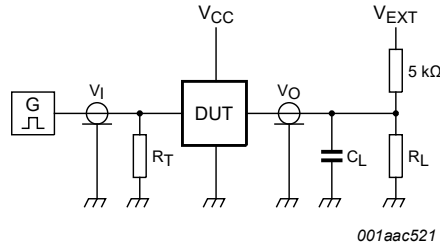


Table 10. Measurement points

Supply voltage	Input			Output
V <sub>CC</sub>	V <sub>M</sub>	V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>	V <sub>M</sub>
2.3 V to 3.6 V	0.5 × V <sub>I</sub>	1.65 V to 3.6 V	≤ 3.0 ns	0.5 × V <sub>CC</sub>



Test data is given in [Table 11](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$C_L$  = load capacitance including jig and probe capacitance;

$R_L$  = load resistance.

**Fig. 11. Test circuit for measuring switching times**

**Table 11. Test data**

Supply voltage	Load		$V_{EXT}$		
$V_{CC}$	$C_L$	$R_L$ [1]	$t_{PLH}$ , $t_{PHL}$	$t_{PZH}$ , $t_{PHZ}$	$t_{PZL}$ , $t_{PLZ}$
2.3 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$

- [1] For measuring enable and disable times  $R_L = 5 \text{ k}\Omega$ .  
 For measuring propagation delays, setup and hold times and pulse width  $R_L = 1 \text{ M}\Omega$ .

## 12. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm

SOT363-2

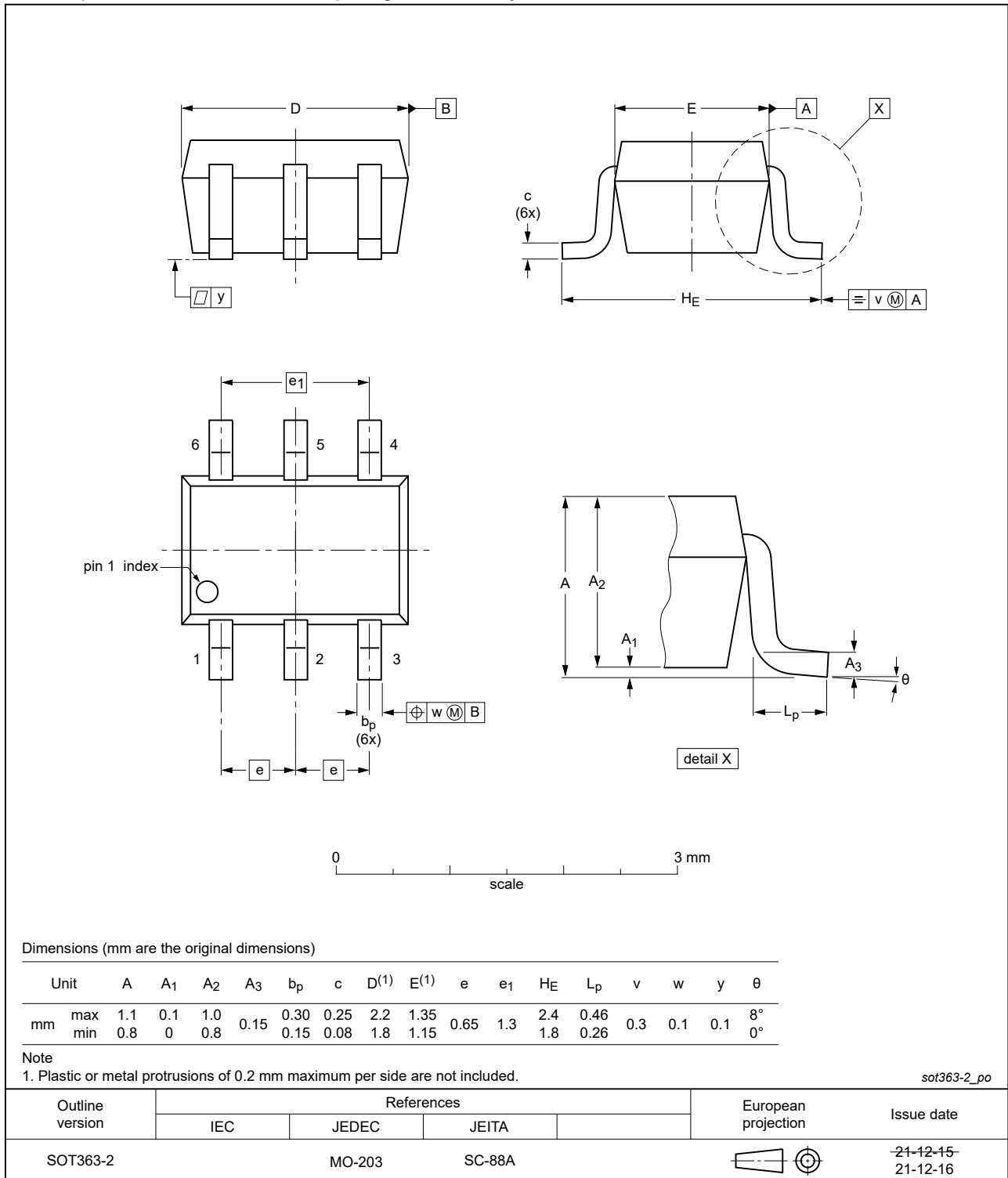


Fig. 12. Package outline SOT363-2 (TSSOP6)

## 13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

## 14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1T97_Q100 v.4	20230717	Product data sheet	-	74AUP1T97_Q100 v.3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74AUP1T97_Q100 v.3	20220127	Product data sheet	-	74AUP1T97_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li>Package SOT363 (SC-88) changed to SOT363-2 (TSSOP6).</li> </ul>			
74AUP1T97_Q100 v.2	20211104	Product data sheet	-	74AUP1T97_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> </ul>			
74AUP1T97_Q100 v.1	20210715	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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