

PESD12VL2BT

Low capacitance double bidirectional ESD protection diode in SOT23 24 July 2023

Product data sheet

1. General description

Low capacitance double bidirectional ElectroStatic Discharge (ESD) protection diode in a small SOT23 Surface-Mounted Device (SMD) plastic package, designed to protect two signal lines from the damage caused by ESD and other transients.

2. Features and benefits

- ESD protection of two lines
- Max. peak pulse power: P_{PPM} = 200 W •
- Low clamping voltage: V_{CL} = 37 V
- Small SMD plastic package
- Ultra low leakage current: I_{RM} = 1 nA
- ESD protection up to 30 kV
- IEC 61000-4-2, level 4 (ESD) •
- IEC 61000-4-5 (surge); I_{PPM} = 5 A
- AEC-Q101 qualified

3. Application information

- Computers and peripherals
- Audio and video equipment •
- Cellular handsets and accessories
- Communication systems
- Portable electronics
- SIM card protection

4. Quick reference data

Table 1. Quick reference data							
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	12	V
C _d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	19	-	pF

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5. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode	3	
2	K2	cathode		
3	CC	double cathode		K2 CC 006aaa155

6. Ordering information

Table 3. Ordering information

Type number	Package	kage				
	Name	Description	Version			
PESD12VL2BT	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23			

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PESD12VL2BT	V5%

[1] % = placeholder for manufacturing site code

8. Limiting values

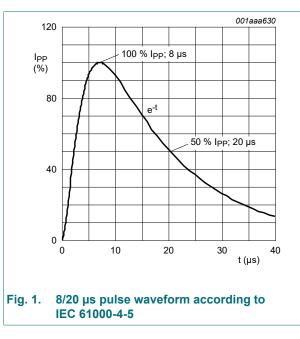
Table 5. Limiting values

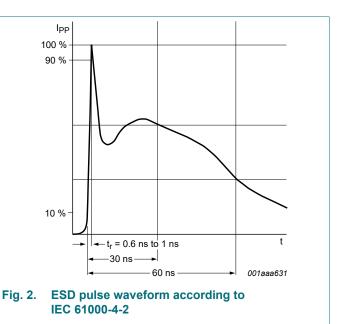
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P _{PPM}	rated peak pulse power	t _p = 8/20 μs	[1] [2]	-	200	W
I _{PPM}	rated peak pulse current		[1] [2]	-	5	А
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximum	ratings					
V _{ESD}	electrostatic discharge	IEC 61000-4-2; contact discharge	[3] [2]	-	30	kV
	voltage	MIL-STD-883; human body model (HBM)	[2]	-	10	kV

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC61000-4-5.

- [2] Measured from pin 1 to 3 or 2 to 3.
- [3] Device stressed with ten non-repetitive ESD pulses.



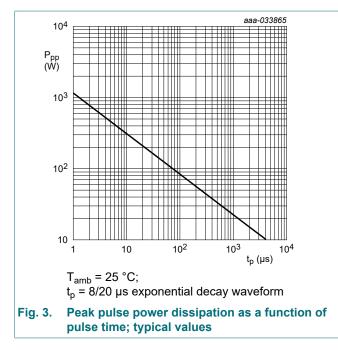


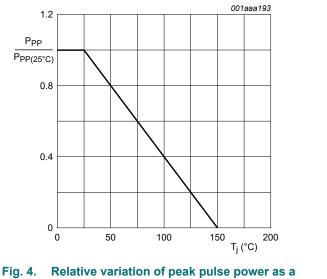
9. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	12	V
V _{BR}	breakdown voltage	I _R = 5 mA; T _{amb} = 25 °C		14.2	15.8	16.7	V
I _{RM}	reverse leakage current	V _{RWM} = 12 V; T _{amb} = 25 °C		-	1	50	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	19	-	pF
V _{CL}	clamping voltage	I _{PP} = 1 A; T _{amb} = 25 °C	[1] [2]	-	-	20	V
		I _{PPM} = 5 A; T _{amb} = 25 °C	[1] [2]	-	-	37	V
R _{diff}	differential resistance	I _R = 1 mA; T _{amb} = 25 °C		-	-	200	Ω

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC61000-4-5.

[2] Measured from pin 1 to 3 or 2 to 3.

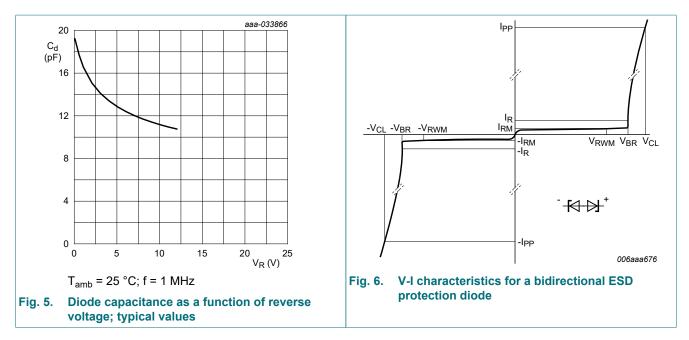




g. 4. Relative variation of peak pulse power as a function of junction temperature; typical values

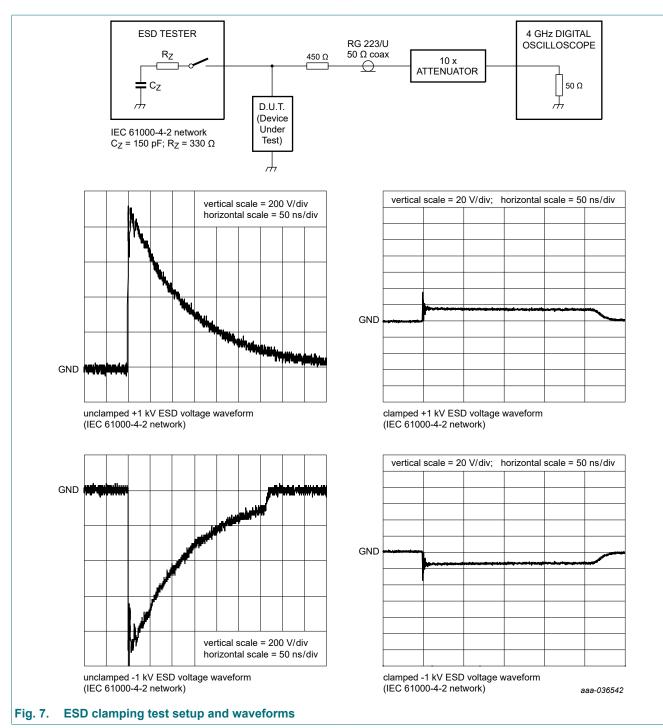
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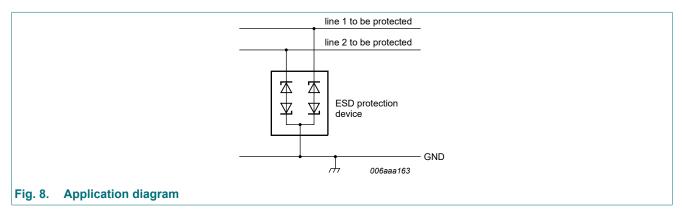
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10. Application information

The device is designed for the protection of two bidirectional signal lines from the damage caused by ESD and surge pulses. The device may be used on lines where the signal polarities are above and below ground.

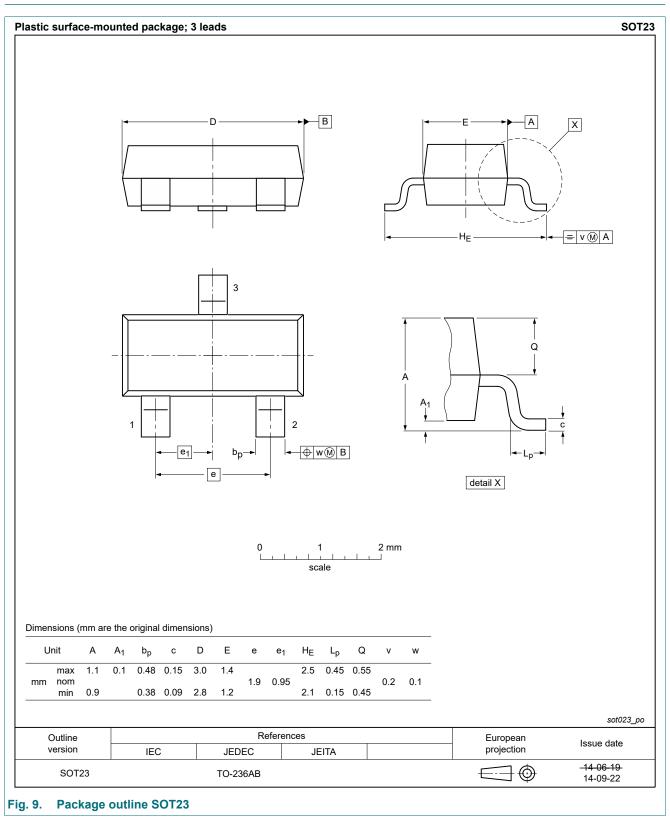


Circuit board layout and protection device placement

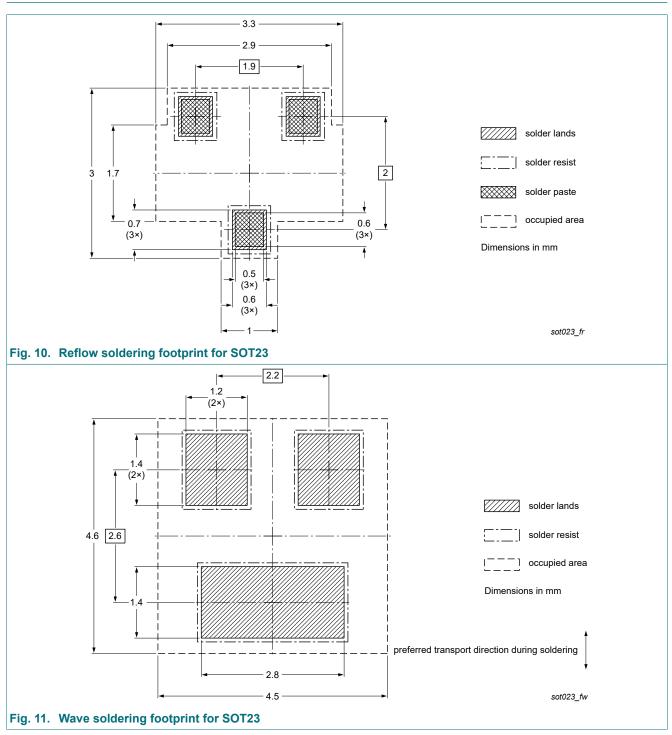
Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- **3.** Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline



12. Soldering



13. Revision history

Table 7. Revision histo	ry				
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes	
PESD12VL2BT v.3	20230724	Product data sheet	-	PESDXL2BT_SER_2	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia Family data sheet reduced to single type data sheet 				
PESDXL2BT_SER_2	20090825	Product data sheet	-	PESDXL2BT_SER_1	
PESDXL2BT_SER_1	20051101	Product data sheet	-	-	

Product data sheet

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <u>https://www.nexperia.com</u>.

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