74LVC4245A

Octal dual supply translating transceiver; 3-state

Rev. 15 — 29 November 2024 Product data sheet

1. General description

The 74LVC4245A is an octal dual supply translating transceiver featuring 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V and 5 V bus in a mixed 3 V and 5 V supply environment. The device features an output enable input ($\overline{OE}$) and a send/receive input (DIR) for direction control. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state, effectively isolating the buses. In suspend mode, when either supply is zero, there is no current path between supplies. $V_{CCA} \geq V_{CCB}$, except in suspend mode. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

2. Features and benefits

- 5 V tolerant inputs/outputs, for interfacing with 5 V logic
- Wide supply voltage range:
  - 3 V bus ($V_{CC(B)}$): 1.5 V to 3.6 V
  - 5 V bus ($V_{CC(A)}$): 1.5 V to 5.5 V
- CMOS low-power consumption
- TTL interface capability at 3.3 V
- Overvoltage tolerant control inputs to 5.5 V
- High-impedance when $V_{CC(A)}$ = 0 V
- Complies with JEDEC standard no. JESD8B/JESD36
- Latch-up performance meets requirements of JESD78 Class 1
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC4245AD	-40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC4245APW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74LVC4245ABQ	-40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

4. Functional diagram

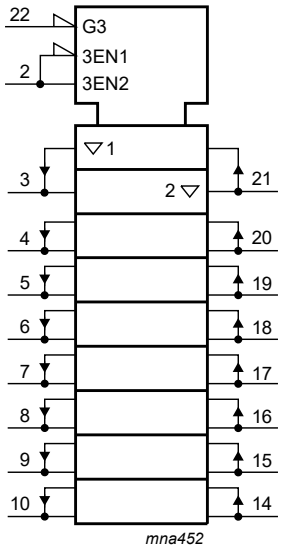


Fig. 1. IEC Logic symbol

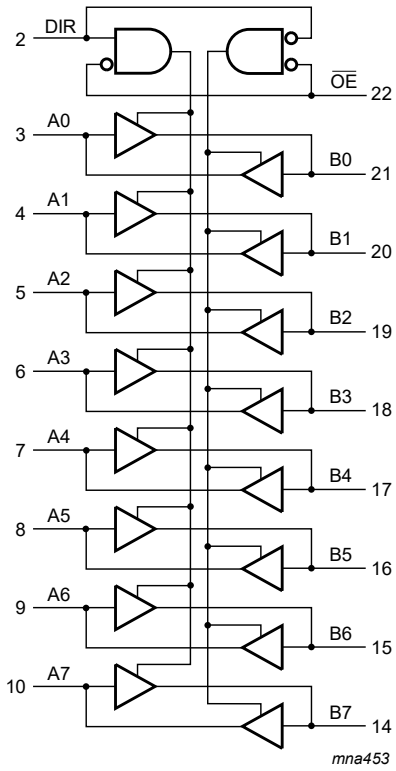
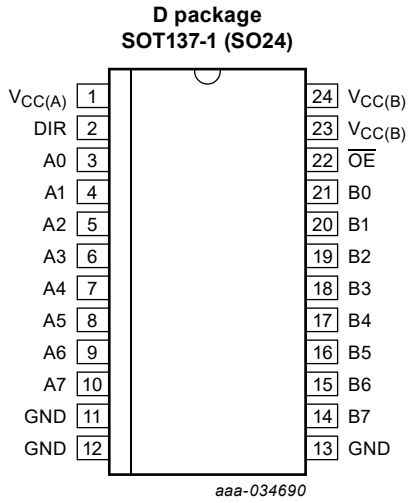
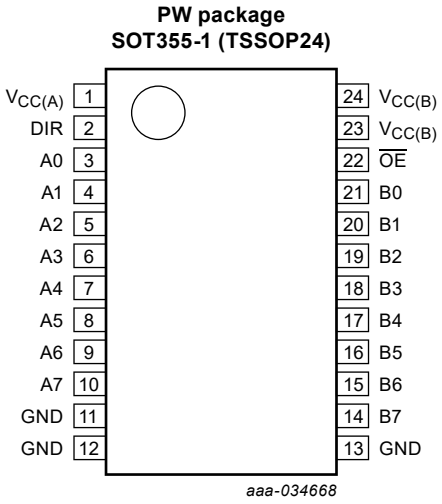


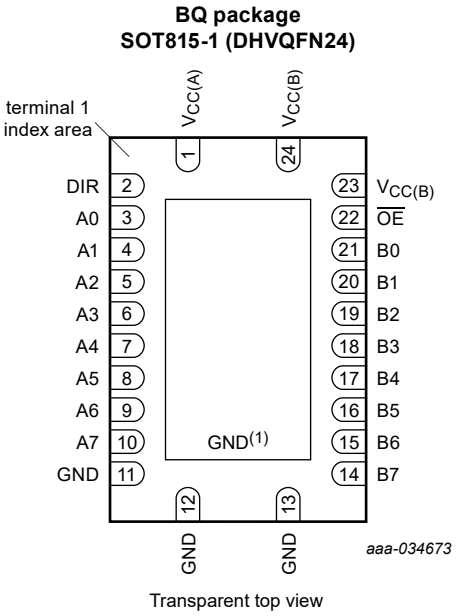
Fig. 2. Logic diagram

5. Pinning information

5.1. Pinning







(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage (5 V bus)
$V_{CC(B)}$	23, 24	supply voltage (3 V bus)
GND	11, 12, 13	ground (0 V)
DIR	2	direction control
A0, A1, A2, A3, A4, A5, A6, A7	3, 4, 5, 6, 7, 8, 9, 10	data input or output
B0, B1, B2, B3, B4, B5, B6, B7	21, 20, 19, 18, 17, 16, 15, 14	data input or output
$\overline{OE}$	22	output enable input (active LOW)

6. Functional description

Table 3. Functional table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Input/output	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B			-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CCO}$ or $V_O < 0$ V	[2]	-	±50	mA
V_O	output voltage	output HIGH or LOW state	[1]	-0.5	V_{CC} + 0.5	V
		output 3-state	[1]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CCO}	[2]	-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output.
[3] For SOT137-1 (SO24) package: P_{tot} derates linearly with 16.2 mW/K above 119 °C.
For SOT355-1 (TSSOP24) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT815-1 (DHVQFN24) package: P_{tot} derates linearly with 15.0 mW/K above 117 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(A)}$	supply voltage A	$V_{CC(A)} \geq V_{CC(B)}$; see Fig. 3 for maximum speed performance	1.5	-	5.5	V
$V_{CC(B)}$	supply voltage B	$V_{CC(A)} \geq V_{CC(B)}$; see Fig. 3 for low-voltage applications	1.5	-	3.6	V
V_I	input voltage	for control inputs	0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC(B)}$ = 2.7 V to 3.0 V	-	-	20	ns/V
		$V_{CC(B)}$ = 3.0 V to 3.6 V	-	-	10	ns/V
		$V_{CC(A)}$ = 3.0 V to 4.5 V	-	-	20	ns/V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	-	-	10	ns/V

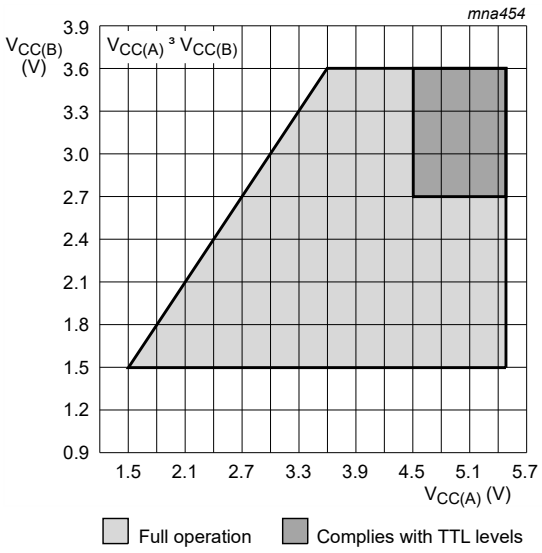


Fig. 3. Supply operation area

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	$V_{CC(B)}$ = 2.7 V to 3.6 V	2.0	-	-	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC(B)}$ = 2.7 V to 3.6 V	-	-	0.8	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		$V_{CC(B)}$ = 2.7 V to 3.6 V; I_O = -100 µA	$V_{CC(B)}$ - 0.2	$V_{CC(B)}$	-	V
		$V_{CC(B)}$ = 2.7 V; I_O = -12 mA	$V_{CC(B)}$ - 0.5	-	-	V
		$V_{CC(B)}$ = 3.0 V; I_O = -24 mA	$V_{CC(B)}$ - 0.8	-	-	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V; I_O = -100 µA	$V_{CC(A)}$ - 0.2	$V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 4.5 V; I_O = -12 mA	$V_{CC(A)}$ - 0.5	-	-	V
		$V_{CC(A)}$ = 4.5 V; I_O = -24 mA	$V_{CC(A)}$ - 0.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		$V_{CC(B)}$ = 2.7 V to 3.6 V; I_O = 100 µA	-	-	0.20	V
		$V_{CC(B)}$ = 2.7 V; I_O = 12 mA	-	-	0.40	V
		$V_{CC(B)}$ = 3.0 V; I_O = 24 mA	-	-	0.55	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V; I_O = 100 µA	-	-	0.20	V
		$V_{CC(A)}$ = 4.5 V; I_O = 12 mA	-	-	0.40	V
		$V_{CC(A)}$ = 4.5 V; I_O = 24 mA	-	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND	-	±0.1	±5	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL} [2]				
		$V_{CC(B)}$ = 3.6 V; V_O = $V_{CC(B)}$ or GND	-	±0.1	±5	µA
		$V_{CC(A)}$ = 5.5 V; V_O = $V_{CC(A)}$ or GND	-	±0.1	±5	µA
I_{CC}	supply current	I_O = 0 A				
		$V_{CC(B)}$ = 3.6 V; other inputs at $V_{CC(B)}$ or GND	-	0.1	10	µA
		$V_{CC(A)}$ = 5.5 V; other inputs at $V_{CC(A)}$ or GND	-	0.1	10	µA
ΔI_{CC}	additional supply current	per pin; I_O = 0 A				
		$V_{CC(B)}$ = 2.7 V to 3.6 V; V_I = $V_{CC(B)}$ - 0.6 V; other inputs at $V_{CC(B)}$ or GND	-	5	500	µA
		$V_{CC(A)}$ = 4.5 V to 5.5 V; V_I = $V_{CC(A)}$ - 0.6 V; other inputs at $V_{CC(A)}$ or GND	-	5	500	µA
C_I	input capacitance		-	4.0	-	pF
$C_{I/O}$	input/output capacitance	An and Bn	-	5.0	-	pF

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC(B)}$ = 2.7 V to 3.6 V	2.0	-	-	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC(B)}$ = 2.7 V to 3.6 V	-	-	0.8	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		$V_{CC(B)}$ = 2.7 V to 3.6 V; I_O = -100 µA	$V_{CC(B)}$ - 0.3	-	-	V
		$V_{CC(B)}$ = 2.7 V; I_O = -12 mA	$V_{CC(B)}$ - 0.65	-	-	V
		$V_{CC(B)}$ = 3.0 V; I_O = -24 mA	$V_{CC(B)}$ - 1.0	-	-	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V; I_O = -100 µA	$V_{CC(A)}$ - 0.3	-	-	V
		$V_{CC(A)}$ = 4.5 V; I_O = -12 mA	$V_{CC(A)}$ - 0.65	-	-	V
		$V_{CC(A)}$ = 4.5 V; I_O = -24 mA	$V_{CC(A)}$ - 1.0	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		$V_{CC(B)}$ = 2.7 V to 3.6 V; I_O = 100 µA	-	-	0.30	V
		$V_{CC(B)}$ = 2.7 V; I_O = 12 mA	-	-	0.60	V
		$V_{CC(B)}$ = 3.0 V; I_O = 24 mA	-	-	0.80	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V; I_O = 100 µA	-	-	0.30	V
		$V_{CC(A)}$ = 4.5 V; I_O = 12 mA	-	-	0.60	V
		$V_{CC(A)}$ = 4.5 V; I_O = 24 mA	-	-	0.80	V
I_I	input leakage current	V_I = 5.5 V or GND	-	-	±20	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL} [2]				
		$V_{CC(B)}$ = 3.6 V; V_O = $V_{CC(B)}$ or GND	-	-	±20	µA
		$V_{CC(A)}$ = 5.5 V; V_O = $V_{CC(A)}$ or GND	-	-	±20	µA
I_{CC}	supply current	I_O = 0 A				
		$V_{CC(B)}$ = 3.6 V; other inputs at $V_{CC(B)}$ or GND	-	-	40	µA
		$V_{CC(A)}$ = 5.5 V; other inputs at $V_{CC(A)}$ or GND	-	-	40	µA
ΔI_{CC}	additional supply current	per pin; I_O = 0 A				
		$V_{CC(B)}$ = 2.7 V to 3.6 V; V_I = $V_{CC(B)}$ - 0.6 V; other inputs at $V_{CC(B)}$ or GND	-	-	5000	µA
		$V_{CC(A)}$ = 4.5 V to 5.5 V; V_I = $V_{CC(A)}$ - 0.6 V; other inputs at $V_{CC(A)}$ or GND	-	-	5000	µA

[1] All typical values are measured at $V_{CC(A)}$ = 5.0 V, $V_{CC(B)}$ = 3.3 V and T_{amb} = 25 °C.
[2] For transceivers, the parameter I_{OZ} includes the input leakage current.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). $V_{CC(A)}$ = 4.5 V to 5.5 V; $t_r = t_f \leq 2.5$ ns. For test circuit see Fig. 6.

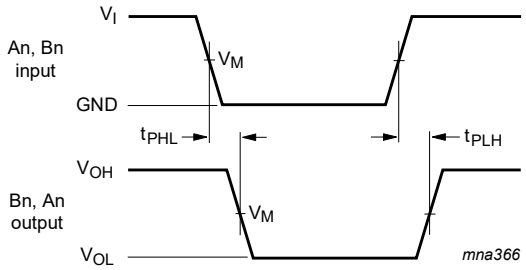
Symbol	Parameter	Conditions	$V_{CC(B)}$	-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	
t_{PHL}	HIGH to LOW propagation delay	An to Bn; see Fig. 4	2.7 V	1.0	3.6	6.3	1.0	8.0	ns
			3.0 V to 3.6 V	1.0	3.3	6.3	1.0	8.0	ns
		Bn to An; see Fig. 4	2.7 V	1.0	3.4	6.1	1.0	8.0	ns
			3.0 V to 3.6 V	1.0	3.4	6.1	1.0	8.0	ns
t_{PLH}	LOW to HIGH propagation delay	An to Bn; see Fig. 4	2.7 V	1.0	3.3	6.7	1.0	8.5	ns
			3.0 V to 3.6 V	1.0	2.8	6.5	1.0	8.5	ns
		Bn to An; see Fig. 4	2.7 V	1.0	3.0	5.0	1.0	6.5	ns
			3.0 V to 3.6 V	1.0	3.0	5.0	1.0	6.5	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to An; see Fig. 5	2.7 V	1.0	4.5	9.0	1.0	11.5	ns
			3.0 V to 3.6 V	1.0	4.5	9.0	1.0	11.5	ns
		$\overline{OE}$ to Bn; see Fig. 5	2.7 V	1.0	4.4	8.7	1.0	11.0	ns
			3.0 V to 3.6 V	1.0	3.8	8.1	1.0	10.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$ to An; see Fig. 5	2.7 V	1.0	4.5	8.1	1.0	10.5	ns
			3.0 V to 3.6 V	1.0	4.5	8.1	1.0	10.5	ns
		$\overline{OE}$ to Bn; see Fig. 5	2.7 V	1.0	4.3	8.7	1.0	11.0	ns
			3.0 V to 3.6 V	1.0	3.2	8.1	1.0	10.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to An; see Fig. 5	2.7 V	1.0	2.9	7.0	1.0	9.0	ns
			3.0 V to 3.6 V	1.0	2.9	7.0	1.0	9.0	ns
		$\overline{OE}$ to Bn; see Fig. 5	2.7 V	1.0	3.9	7.7	1.0	10.0	ns
			3.0 V to 3.6 V	1.0	3.5	7.7	1.0	10.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to An; see Fig. 5	2.7 V	1.0	2.8	5.8	1.0	7.5	ns
			3.0 V to 3.6 V	1.0	2.8	5.8	1.0	7.5	ns
		$\overline{OE}$ to Bn; see Fig. 5	2.7 V	1.0	3.3	7.8	1.0	10.0	ns
			3.0 V to 3.6 V	1.0	2.9	7.8	1.0	10.0	ns
$t_{sk(o)}$	output skew time		[2]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	5 V bus: Bn to An; V_I = GND to $V_{CC(A)}$; $V_{CC(A)}$ = 5.0 V	[3]						
		outputs enabled	-	-	17	-	-	-	pF
		outputs disabled	-	-	5	-	-	-	pF
		3 V bus: An to Bn; V_I = GND to $V_{CC(B)}$; $V_{CC(B)}$ = 3.3 V	[3]						
		outputs enabled	-	-	17	-	-	-	pF
		outputs disabled	-	-	5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C, $V_{CC(A)}$ = 5.0 V, and $V_{CC(B)}$ = 2.7 V and 3.3 V respectively.

[2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW). $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz;
C_L = output load capacitance in pF; V_{CC} = supply voltage in Volts;
N = number of inputs switching; $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs

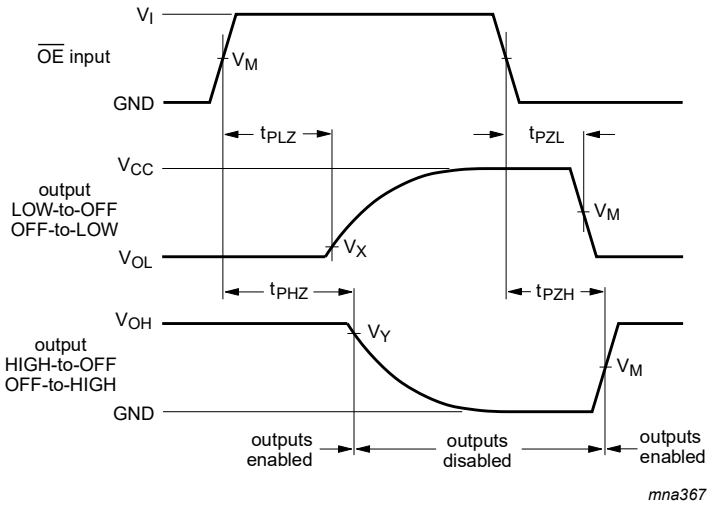
10.1. Waveforms and test circuit



Measurement point are given in Table 8.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig. 4. Input (An, Bn) to output (Bn, An) propagation delays



Measurement point are given in Table 8.

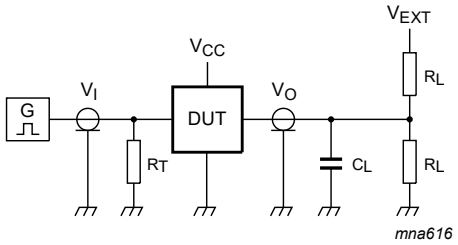
V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig. 5. 3-state enable and disable times

Table 8. Measurement points

Supply voltage		Input		Output		
$V_{CC(A)}$	$V_{CC(B)}$	V_M [1]	V_I [1]	V_M [2]	V_X	V_Y
≤ 2.7 V	≤ 2.7 V	0.5 V_{CCI}	V_{CCI}	0.5 V_{CCO}	-	-
-	2.7 V to 3.6 V	1.5 V	2.7 V	1.5 V	-	-
≥ 4.5 V	-	0.5 V_{CCI}	3.0 V	0.5 V_{CCO}	-	-
-	≥ 2.7 V	-	V_{CCI}	-	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the data input port.
[2] V_{CCO} is the supply voltage associated with the data output port.



Test data is given in Table 9. Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 6. Test circuit for measuring switching times

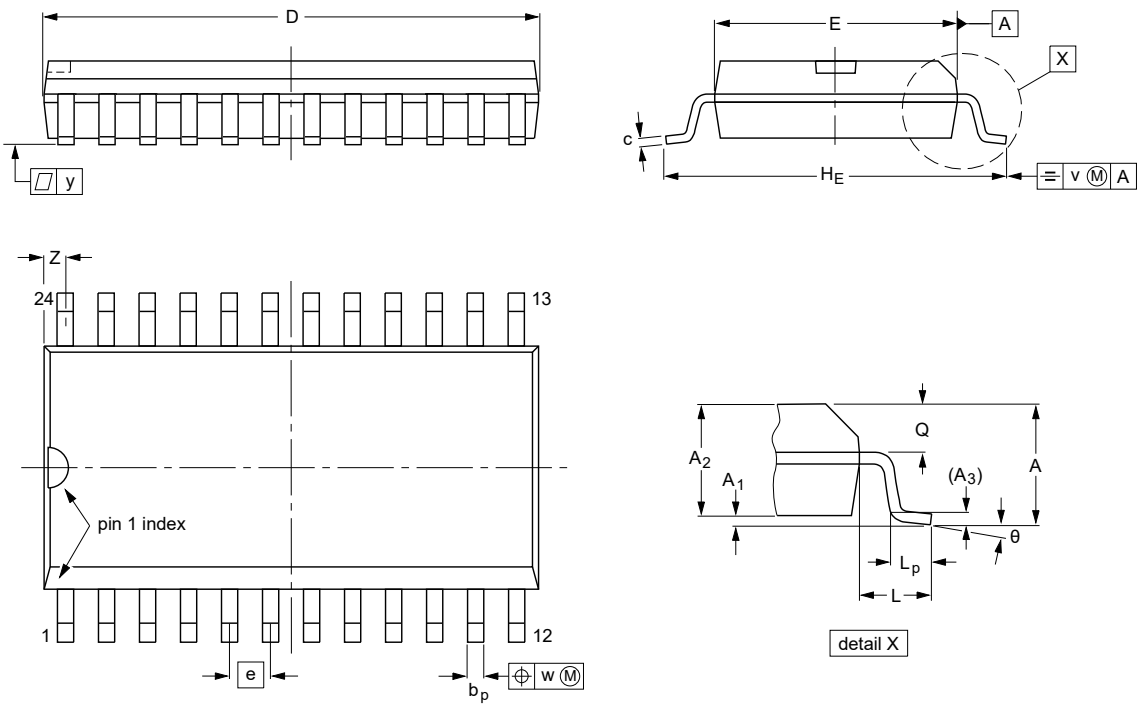
Table 9. Test data

Supply voltage		Input	Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I [1]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [2]
< 2.7 V	< 2.7 V	V_{CCI}	50 pF	500 Ω	open	GND	2 × V_{CCO}
-	2.7 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	2 × V_{CCO}
4.5 V to 5.5 V	-	3.0 V	50 pF	500 Ω	open	GND	2 × V_{CCO}

[1] V_{CCI} is the supply voltage associated with the data input port.
[2] V_{CCO} is the supply voltage associated with the output port.

11. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

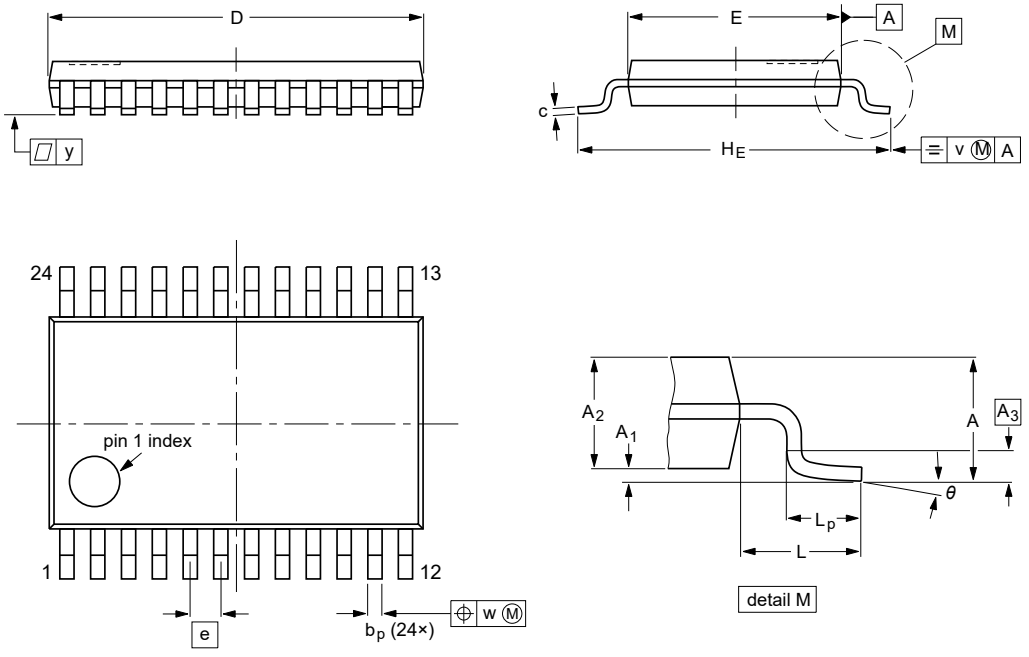
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig. 7. Package outline SOT137-1 (SO24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05	0.25 BSC	0.30	0.20	7.90	4.50	0.65 BSC	6.60	1.00 REF	0.75	0.2	0.1	0.1	8°
	nom																
	min		0.05	0.80		0.19	0.09	7.70	4.30		6.20		0.45				0°

Notes

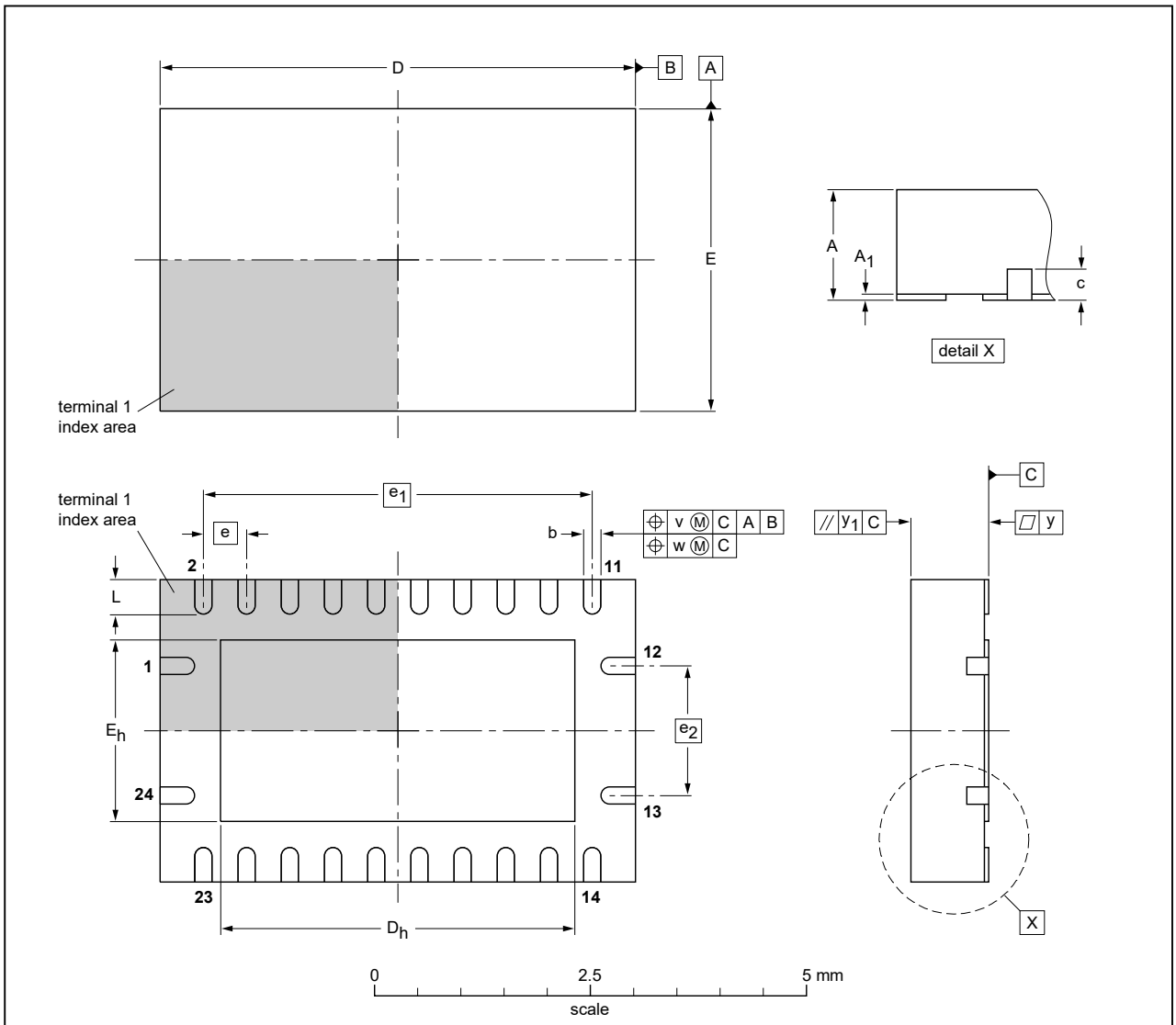
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot355-1_po

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153				~~03-02-19~~ 24-11-07

Fig. 8. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Fig. 9. Package outline SOT815-1 (DHVQFN24)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC4245A v.15	20241129	Product data sheet	-	74LVC4245A v.14
Modifications:	• Fig. 8: Aligned TSSOP package outline drawing to JEDEC MO-153.			
74LVC4245A v.14	20230901	Product data sheet	-	74LVC4245A v.13
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC4245A v.13	20210827	Product data sheet	-	74LVC4245A v.12
Modifications:	• Type number 74LVC4245ADB (SOT340-1/SSOP24) removed.			
74LVC4245A v.12	20210412	Product data sheet	-	74LVC4245A v.11
Modifications:	• Section 9: ΔI_{CC} conditions have changed.			
74LVC4245A v.11	20200922	Product data sheet	-	74LVC4245A v.10
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 updated. • Table 4: Derating values for P_{tot} total power dissipation updated. • Measurement points related to Fig. 4 and Fig. 5 are given in Table 8.			
74LVC4245A v.10	20121218	Product data sheet	-	74LVC4245A v.9
Modifications:	• $V_{CC(A)}$ and $V_{CC(B)}$ changed into $V_{CC(A)}$ and $V_{CC(B)}$ (errata)			
74LVC4245A v.9	20121120	Product data sheet	-	74LVC4245A v.8
Modifications:	• Section 5.1: Pin configuration drawing corrected for DHVQFN24 package			
74LVC4245A v.8	20111122	Product data sheet	-	74LVC4245A v.7
74LVC4245A v.7	20110812	Product data sheet	-	74LVC4245A v.6
74LVC4245A v.6	20080118	Product data sheet	-	74LVC4245A v.5
74LVC4245A v.5	20040330	Product specification	-	74LVC4245A v.4
74LVC4245A v.4	20040211	Product specification	-	74LVC4245A v.3
74LVC4245A v.3	19990615	Product specification	-	74LVC4245A v.2
74LVC4245A v.2	19980729	Product specification	-	74LVC4245A v.1
74LVC4245A v.1	19980729	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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