



74LVT16240A

3.3 V 16-bit inverting buffer/driver; 3-state

Rev. 6 — 8 July 2024

Product data sheet

1. General description

The 74LVT16240A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four output enable inputs (1OE, 2OE, 3OE, 4OE), each controlling four of the 3-state outputs.

2. Features and benefits

- 16-bit bus interface
- 3-state buffers
- Output capability: +64 mA/-32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
 - JESD78B Class II exceeds 500 mA
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT16240ADGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

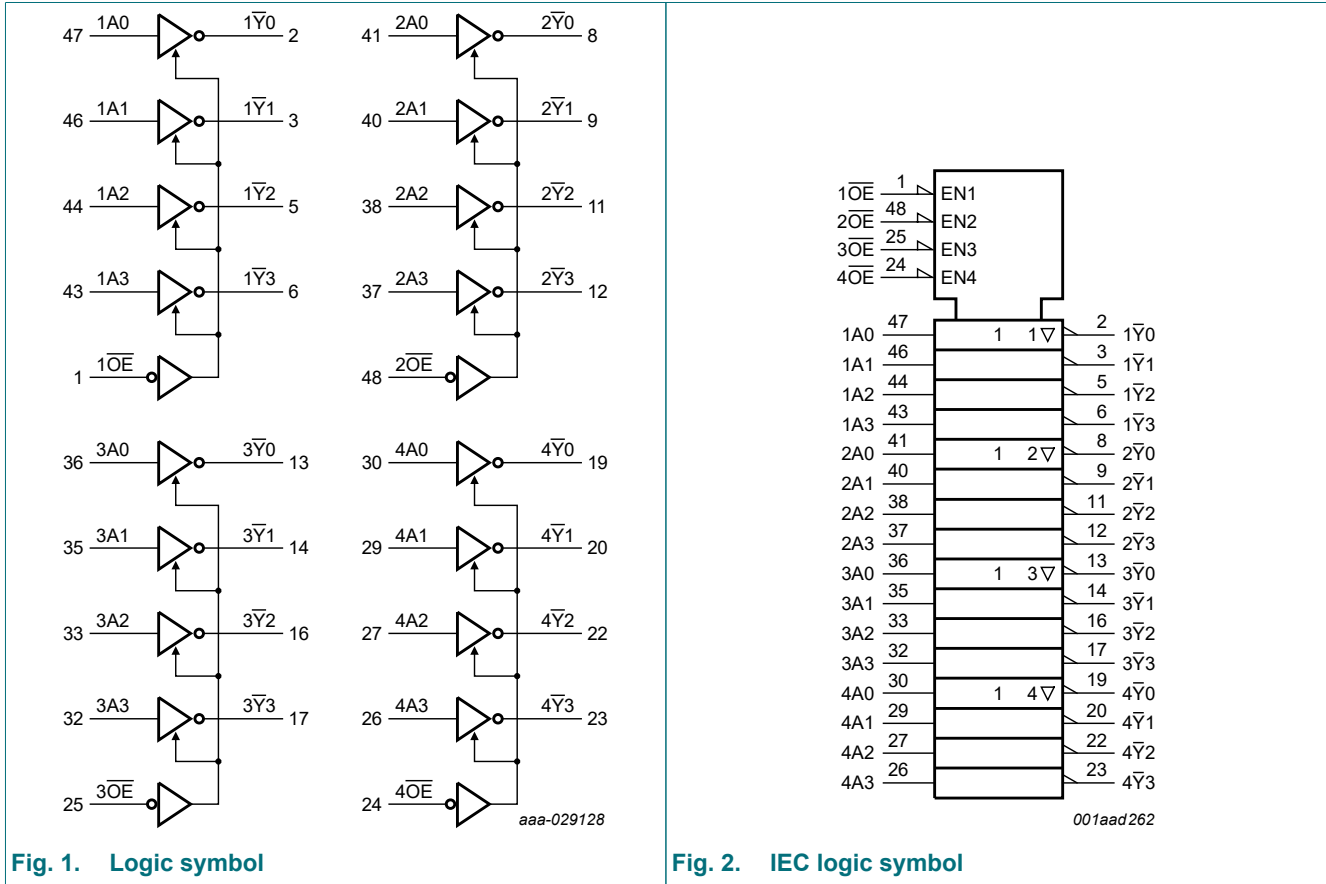
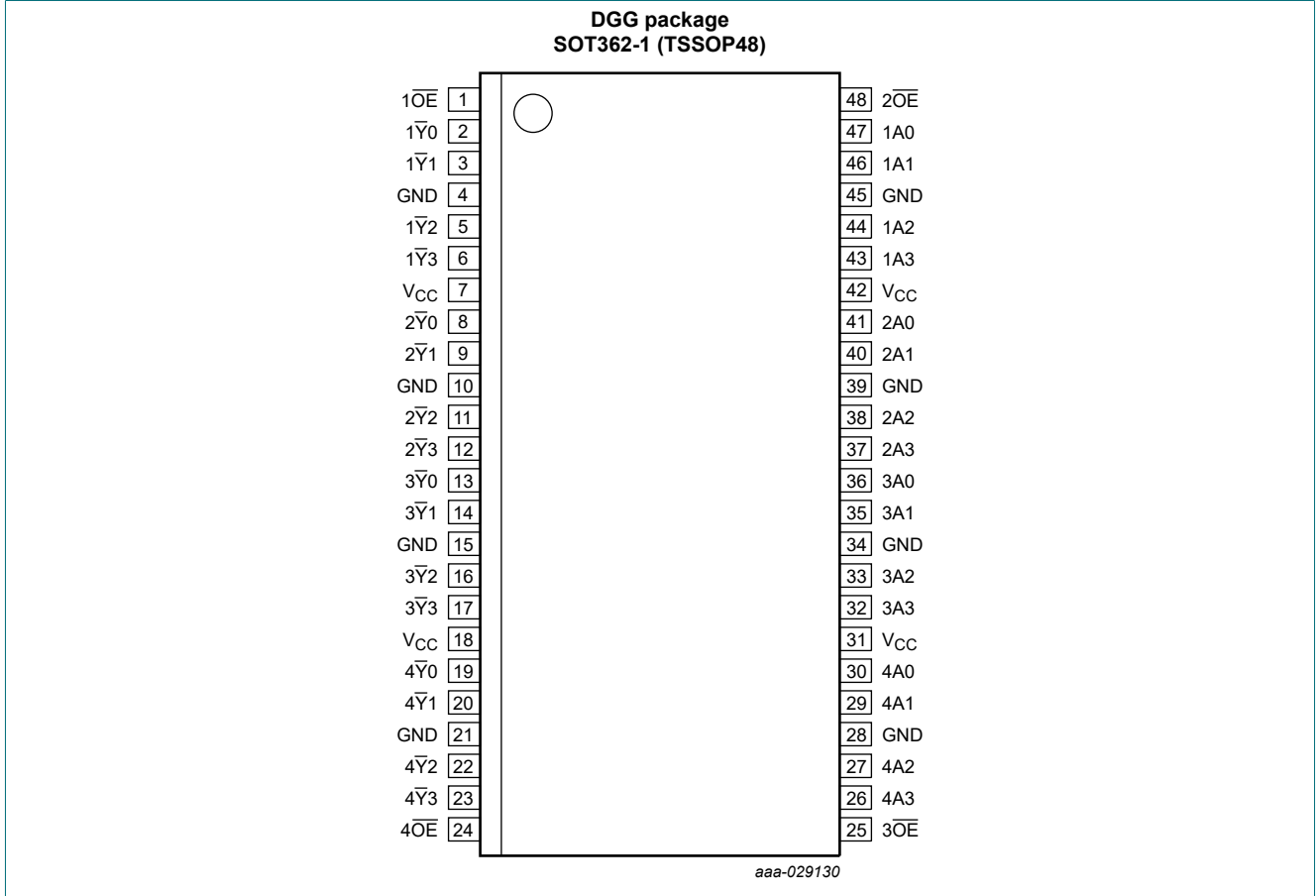


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE, 3OE, 4OE	1, 48, 25, 24	output enable inputs (active LOW)
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	data inputs
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	data inputs
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	data inputs
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	data inputs
1Y0, 1Y1, 1Y2, 1Y3	2, 3, 5, 6	data outputs
2Y0, 2Y1, 2Y2, 2Y3	8, 9, 11, 12	data outputs
3Y0, 3Y1, 3Y2, 3Y3	13, 14, 16, 17	data outputs
4Y0, 4Y1, 4Y2, 4Y3	19, 20, 22, 23	data outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
VCC	7, 18, 31, 42	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
nOE	nAn	nYn
L	L	H
L	H	L
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		[1] -0.5	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		[2] -	+150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.7	-	3.6	V
V _I	input voltage		0	-	5.5	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	$V_{CC} = 2.7\text{ V}$; $I_{IK} = -18\text{ mA}$	-	-0.85	-1.2	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	V_{CC}	-	V
		$V_{CC} = 2.7\text{ V}$; $I_{OH} = -8\text{ mA}$	2.4	2.5	-	V
		$V_{CC} = 3.0\text{ V}$; $I_{OH} = -32\text{ mA}$	2.0	2.3	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 2.7\text{ V}$; $I_{OL} = 100\text{ }\mu\text{A}$	-	0.07	0.2	V
		$V_{CC} = 2.7\text{ V}$; $I_{OL} = 24\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}$; $I_{OL} = 16\text{ mA}$	-	0.25	0.4	V
		$V_{CC} = 3.0\text{ V}$; $I_{OL} = 32\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}$; $I_{OL} = 64\text{ mA}$	-	0.4	0.55	V
I_{OH}	HIGH-level output current		-	-	-32	mA
I_{OL}	LOW-level output current		-	-	32	mA
		current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$	-	-	64	mA
I_I	input leakage current	all input pins				
		$V_{CC} = 0\text{ V or }3.6\text{ V}$; $V_I = 5.5\text{ V}$	-	0.4	10	μA
		control pins				
		$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}\text{ or GND}$	-	± 0.1	± 1	μA
		data pins				
		$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ [2]	-	0.1	1	μA
	$V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$ [2]	-	-0.4	-5	μA	
I_{OFF}	power-off leakage current	$V_{CC} = 0\text{ V}$; $V_I\text{ or }V_O = 0\text{ V to }4.5\text{ V}$	-	0.1	± 100	μA
I_{BHL}	bus hold LOW current	nAn input; $V_{CC} = 3\text{ V}$; $V_I = 0.8\text{ V}$	75	135	-	μA
I_{BHH}	bus hold HIGH current	nAn input; $V_{CC} = 3\text{ V}$; $V_I = 2.0\text{ V}$	-75	-135	-	μA
I_{BHLO}	bus hold LOW overdrive current	nAn input; $V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V to }3.6\text{ V}$ [3]	500	-	-	μA
I_{BHHO}	bus hold HIGH overdrive current	nAn input; $V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V to }3.6\text{ V}$ [3]	-	-	-500	μA
I_{CEX}	output high leakage current	output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5\text{ V}$; $V_{CC} = 3.0\text{ V}$	-	50	125	μA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V to }V_{CC}$; $V_I = \text{GND or }V_{CC}$; $n\overline{\text{OE}} = \text{don't care}$ [4]	-	1	± 100	μA
I_{OZ}	OFF-state output current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{IL}\text{ or }V_{IH}$				
		output HIGH: $V_O = 3.0\text{ V}$	-	0.5	5	μA
		output LOW: $V_O = 0.5\text{ V}$	-	0.5	-5	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = \text{GND or }V_{CC}$; $I_O = 0\text{ A}$				
		outputs HIGH	-	0.07	0.12	mA
		outputs LOW	-	4.0	6	mA
		outputs disabled [5]	-	0.07	0.12	mA

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3\text{ V}$ to 3.6 V ; one input at $V_{CC} - 0.6\text{ V}$ and other inputs at V_{CC} or GND [6]	-	0.1	0.2	mA
C_I	input capacitance	$n\overline{OE}$; $V_I = 0\text{ V}$ or 3 V	-	3	-	pF
C_O	output capacitance	Outputs disabled; $V_O = 0\text{ V}$ or 3.0 V	-	9	-	pF

[1] All typical values are at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^\circ\text{C}$.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms . From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ a transition time of $100\text{ }\mu\text{s}$ is permitted. This parameter is valid for $T_{amb} = 25\text{ }^\circ\text{C}$ only.

[5] Measured with outputs pulled up to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{PLH}	LOW to HIGH propagation delay	nAn to $n\overline{Yn}$; see Fig. 3				
		$V_{CC} = 2.7\text{ V}$	-	-	4.0	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	0.5	1.8	3.2	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to $n\overline{Yn}$; see Fig. 3				
		$V_{CC} = 2.7\text{ V}$	-	-	4.0	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	0.5	2.0	3.2	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to $n\overline{Yn}$; see Fig. 4				
		$V_{CC} = 2.7\text{ V}$	-	-	5.0	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	2.3	4.0	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to $n\overline{Yn}$; see Fig. 4				
		$V_{CC} = 2.7\text{ V}$	-	-	4.8	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	2.1	4.4	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to $n\overline{Yn}$; see Fig. 4				
		$V_{CC} = 2.7\text{ V}$	-	-	5.0	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	3.2	4.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to $n\overline{Yn}$; see Fig. 4				
		$V_{CC} = 2.7\text{ V}$	-	-	4.8	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	3.0	4.4	ns

[1] Typical values are at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^\circ\text{C}$.

10.1. Waveforms and test circuit

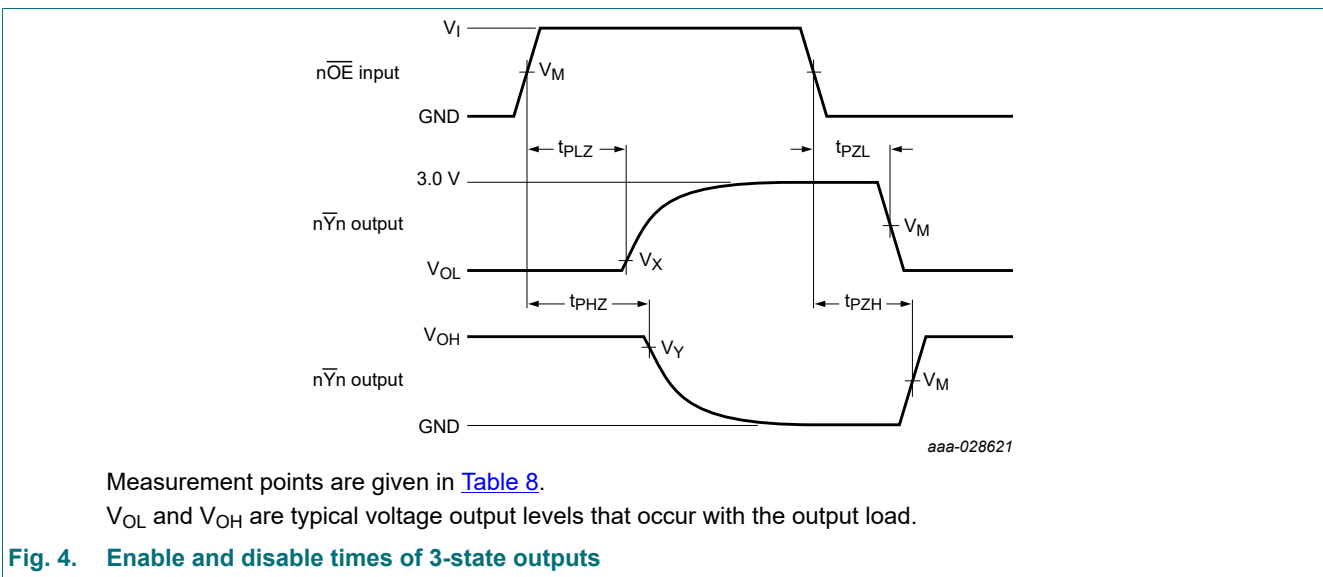
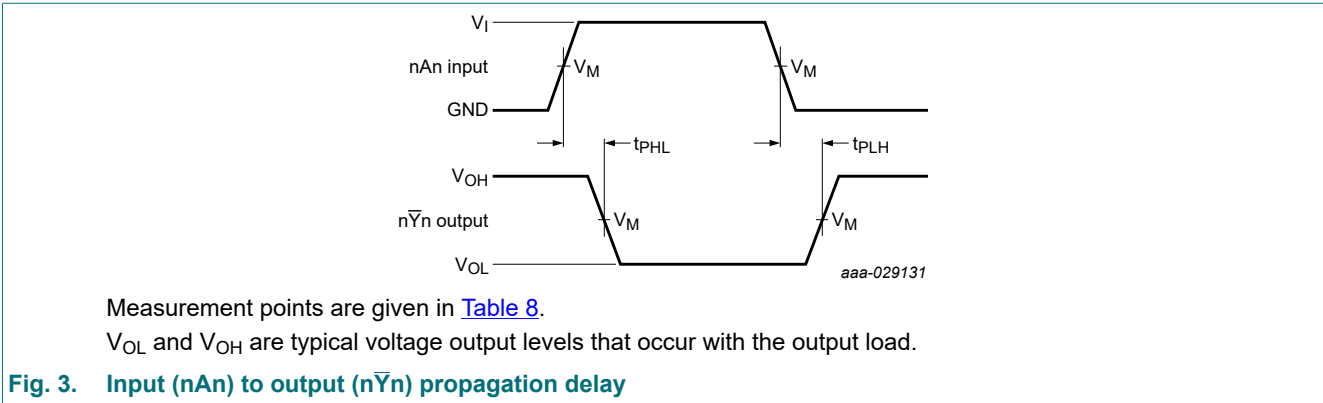
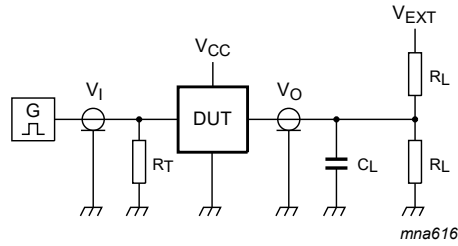


Table 8. Measurement points

Input		Output		
V_{CC}	V_M	V_M	V_X	V_Y
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = Test voltage for switching times.

Fig. 5. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_w	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

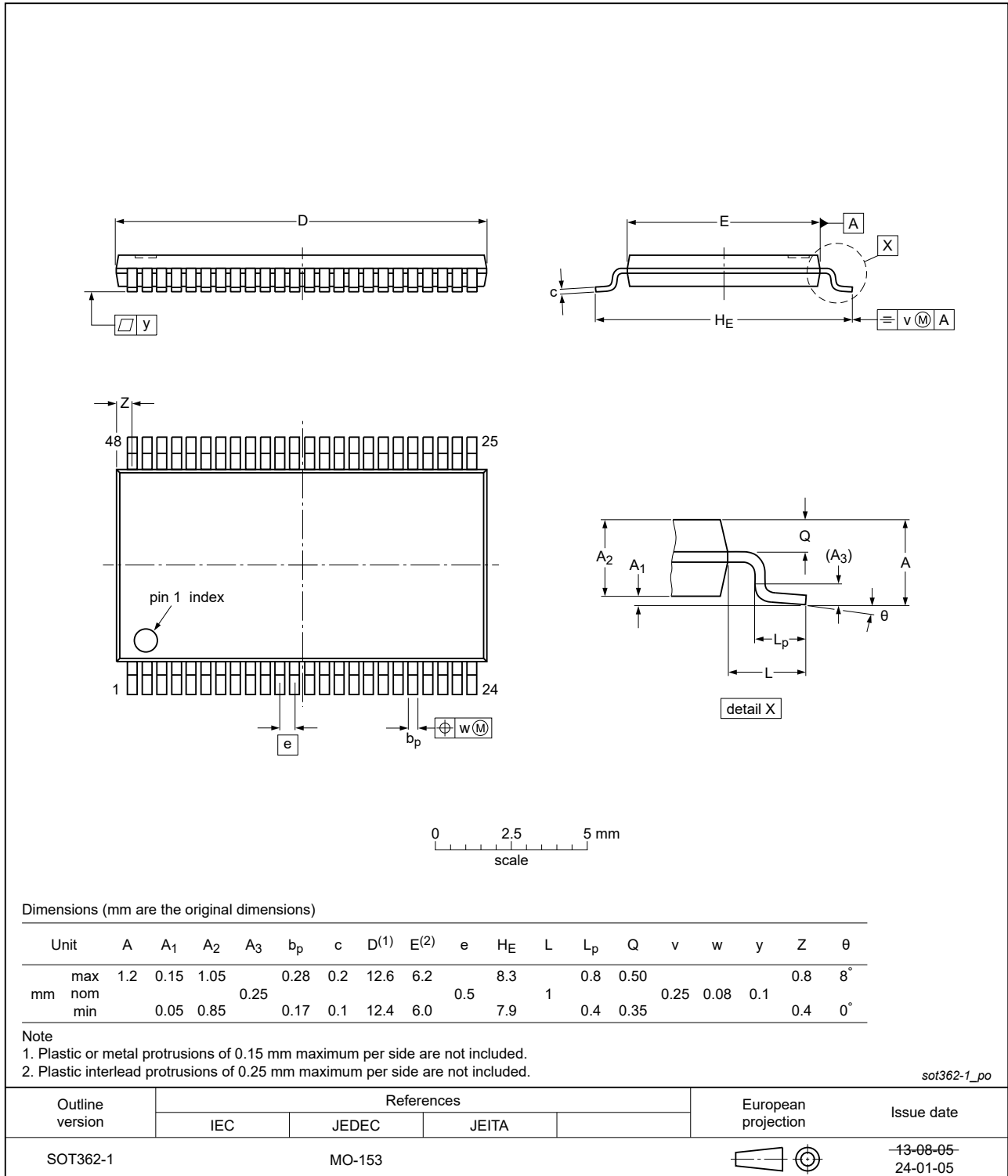


Fig. 6. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT16240A v.6	20240708	Product data sheet	-	74LVT16240A v.5
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74LVT16240A v.5	20240208	Product data sheet	-	74LVT16240A v.4
Modifications:	<ul style="list-style-type: none"> Fig. 6: Updated package outline drawing SOT362-1 (TSSOP48). Fig. 5 waveform definition removed (errata). 			
74LVT16240A v.4	20181001	Product data sheet	-	74LVT16240A v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74LVT16240ADL (SOT370-1) removed. 			
74LVT16240A v.3	20030221	Product data sheet	-	74LVT16240A v.2
Modifications:	<ul style="list-style-type: none"> Table 1 corrected: removed 'North America' column. Fig. 2 modified to correct pin names 			
74LVT16240A v.2	19980219	Product specification	-	74LVT16240A v.1
74LVT16240A v.1	19941215	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Functional diagram	2
5. Pinning information	3
5.1. Pinning.....	3
5.2. Pin description.....	3
6. Functional description	4
7. Limiting values	4
8. Recommended operating conditions	4
9. Static characteristics	5
10. Dynamic characteristics	6
10.1. Waveforms and test circuit.....	7
11. Package outline	9
12. Abbreviations	10
13. Revision history	10
14. Legal information	11

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