## 1. General description

PNP/PNP Resistor-Equipped double Transistor (RET) in a medium power SOT1118 (DFN2020-6) leadless Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PIMN31PA NPN/PNP complement: PIMC31PA

## 2. Features and benefits

500 mA output current capability

- Built-in resistors
- Simplifies circuit design
- · Reduces component count
- · Reduces pick and place costs

## 3. Applications

- Digital applications
- Cost-saving alternative to BC807 series in digital applications
- · Control of IC inputs
- Switching loads

### 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transistor							
V <sub>CEO</sub>	collector-emitter voltage	open base		-	-	-50	V
Io	output current			-	-	-500	mA
R1	bias resistor 1 (input)	T <sub>amb</sub> = 25 °C	[1]	0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		[1]	9	10	11	

[1] See section "Test information" for resistor calculation and test conditions.



50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

# 5. Pinning information

**Table 2. Pinning information** 

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1		O1 I2 GND2
2	I1	input (base) TR1	6 5 4	
3	O2	output (collector) TR2		R1 R2
4	GND2	GND (emitter) TR2		TR2
5	12	input (base) TR2		TR1 R2 R1
6	01	output (collector) TR1	1 2 3	
7	01	output (collector) TR1	Transparent top view	
8	O2	output (collector) TR2	DFN2020-6 (SOT1118)	GND1 I1 O2 aaa-019790

# 6. Ordering information

**Table 3. Ordering information** 

Type number	Package		
	Name	Description	Version
PIMP31PA		plastic, leadless thermal enhanced ultra thin small outline package; no leads; 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	<u>SOT1118</u>

## 7. Marking

### Table 4. Marking codes

Type number	Marking code
PIMP31PA	8G

50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

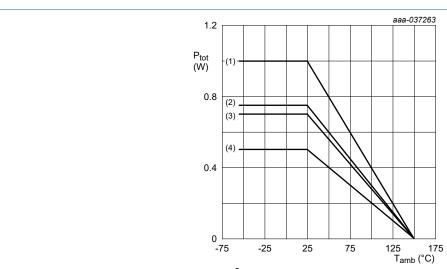
## 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transiste	or					
V <sub>CBO</sub>	collector-base voltage	open emitter		-	-50	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	-50	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	-5	V
VI	input voltage			-10	5	V
Io	output current			-	-500	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	360	mW
			[2]	-	550	mW
			[3]	-	510	mW
			[4]	-	730	mW
Per device		1		<u> </u>		
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	500	mW
			[2]	-	750	mW
			[3]	-	700	mW
			[4]	-	1	W
Tj	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided, 35µm copper, tin-plated; mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated; mounting pad for collector 1 cm<sup>2</sup>.



- (1) FR4 PCB, 4-layer copper, 1 cm<sup>2</sup>
- (2) FR4 PCB, single-sided, 35µm copper, 1 cm<sup>2</sup>
- (3) FR4 PCB, 4-layer copper, standard footprint
- (4) FR4 PCB, single-sided, 35µm copper, standard footprint
- Fig. 1. Per device: Power derating curves for DFN2020-6 (SOT1118)

PIMP31PA

50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

## 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transist	tor						
ιι ( <u>)</u> -α)	thermal resistance from	in free air	[1]	-	-	348	K/W
	junction to ambient	[3	[2]	-	-	228	K/W
			[3]	-	-	246	K/W
			[4]	-	-	172	K/W
Per device	'		,				
$R_{th(j-a)}$			[1]	-	-	250	K/W
	junction to ambient		[2]	-	-	167	K/W
			[3]	-	-	179	K/W
			[4]	-	-	125	K/W

- Device mounted on an FR4 PCB, single-sided, 35  $\mu m$  copper, tin-plated and standard footprint.
- [2] [3] Device mounted on an FR4 PCB, single-sided, 35μm copper, tin-plated; mounting pad for collector 1 cm<sup>2</sup>.
- Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- Device mounted on an FR4 PCB, 4-layer copper, tin-plated; mounting pad for collector 1 cm<sup>2</sup>.

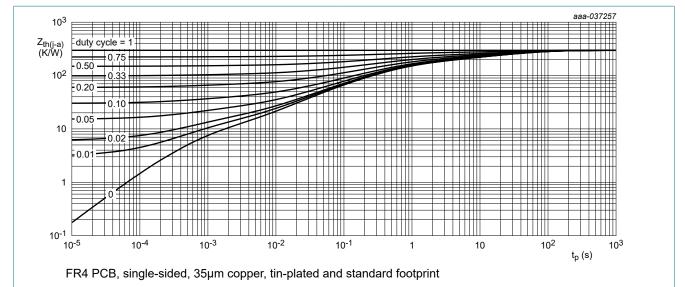
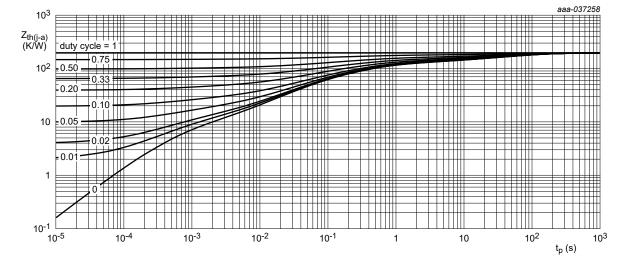


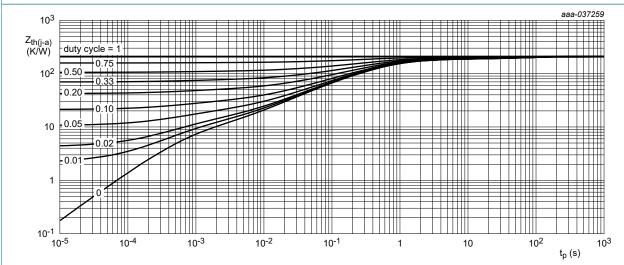
Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

### 50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$



FR4 PCB, single-sided, 35µm copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.

Fig. 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, tin-plated and standard footprint.

Fig. 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$

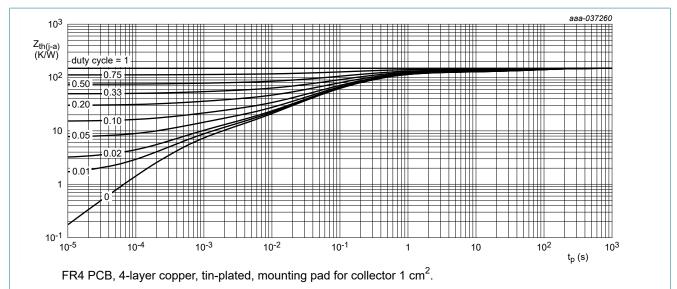


Fig. 5. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

## 10. Characteristics

**Table 7. Characteristics** 

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transist	or	1					
V <sub>(BR)CBO</sub>	collector-base breakdown voltage	I <sub>C</sub> = -100 μA; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C		-50	-	-	V
V <sub>(BR)CEO</sub>	collector-emitter breakdown voltage	$I_C = -10 \text{ mA}; I_B = 0 \text{ A}; T_{amb} = 25 \text{ °C}$		-50	-	-	V
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = -50 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	-100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = -50 V; I <sub>B</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	-0.5	μΑ
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	-0.72	mA
h <sub>FE</sub>	DC current gain	$V_{CE}$ = -5 V; $I_{C}$ = -50 mA; $T_{amb}$ = 25 °C		70	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	$I_C$ = -50 mA; $I_B$ = -2.5 mA; $T_{amb}$ = 25 °C		-	-	-100	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5 \text{ V}; I_{C} = -100 \mu\text{A}; T_{amb} = 25 ^{\circ}\text{C}$		-0.3	-0.6	-1	V
$V_{I(on)}$	on-state input voltage	$V_{CE}$ = -0.3 V; $I_{C}$ = -20 mA; $T_{amb}$ = 25 °C		-0.4	-0.8	-1.4	V
R1	bias resistor 1 (input)	T <sub>amb</sub> = 25 °C	[1]	0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		[1]	9	10	11	
C <sub>c</sub>	collector capacitance	$V_{CB} = -10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A};$ f = 1 MHz; $T_{amb} = 25 \text{ °C}$		-	7	-	pF
f <sub>T</sub>	transition frequency	$V_{CE}$ = -5 V; $I_{C}$ = -50 mA; f = 100 MHz; $T_{amb}$ = 25 °C	[2]	-	150	-	MHz

- [1] See section "Test information" for resistor calculation and test conditions.
- [2] Characteristics of built-in transistor.

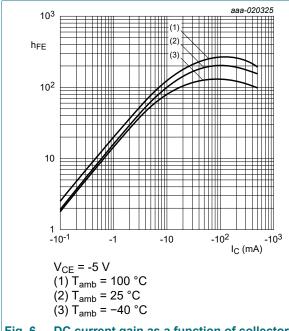


Fig. 6. DC current gain as a function of collector current; typical values

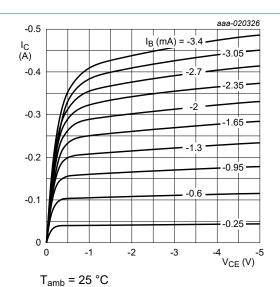
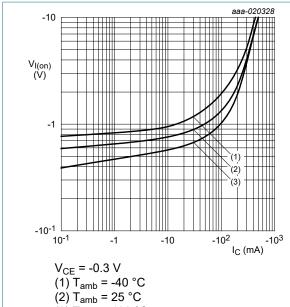


Fig. 7. Collector current as a function of collectoremitter voltage; typical values

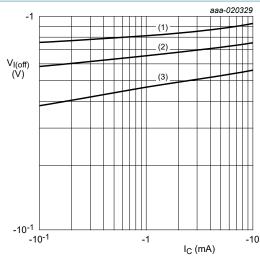
PIMP31PA

### 50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$



(3)  $T_{amb} = 100 \, ^{\circ}C$ 

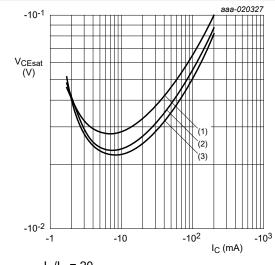
Fig. 8. On-state input voltage as a function of collector | Fig. 9. current; typical values



V<sub>CE</sub> = -5 V (1) T<sub>amb</sub> = -40 °C (2) T<sub>amb</sub> = 25 °C

(3)  $T_{amb} = 100 \, ^{\circ}C$ 

Off-state input voltage as a function of collector current; typical values



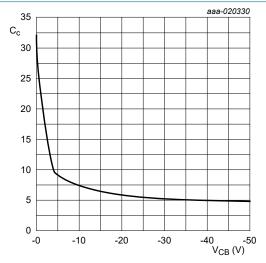
 $I_C/I_B = 20$ 

(1)  $T_{amb}$  = 100 °C

(2) T<sub>amb</sub> = 25 °C

(3)  $T_{amb} = -40 \, ^{\circ}C$ 

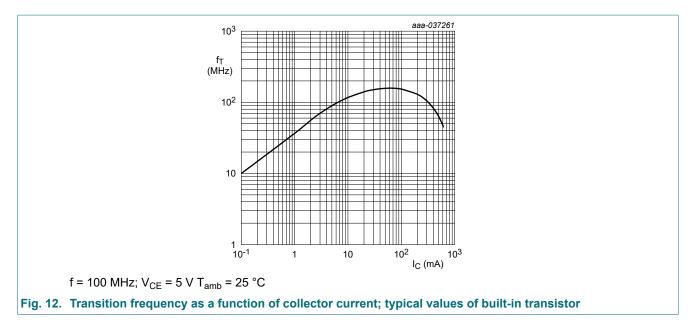
Fig. 10. Collector-emitter saturation voltage as a function of collector current; typical values



f = 1 MHz $T_{amb} = 25 \, ^{\circ}C$ 

Fig. 11. Collector capacitance as a function of collectorbase voltage; typical values

### 50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$



50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

## 11. Test information

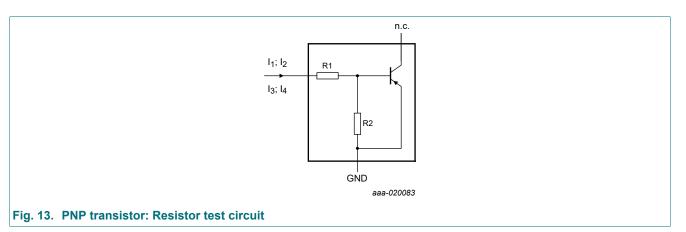
#### **Resistor calculation**

• Calculation of bias resistor 1 (R1):

$$R_{I} = \frac{V(I_{2}) - V(I_{1})}{I_{2} - I_{1}}$$

· Calculation of bias resistor ratio (R2/R1):

$$\frac{R2}{R1} = \frac{V(I4) - V(I3)}{R1 \cdot (I4 - I3)} - 1$$



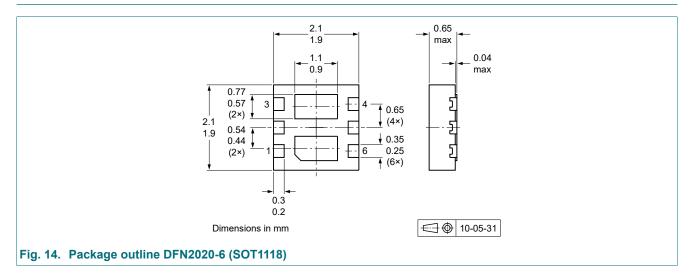
### **Resistor test conditions**

**Table 8. Resistor test conditions** 

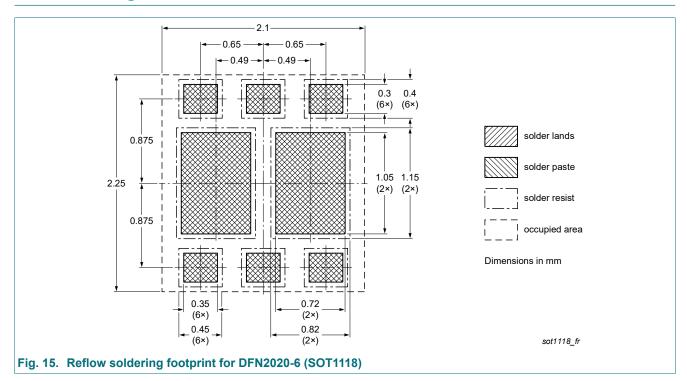
PIMP31PA	R1 (kΩ)	R2 (kΩ)	Test conditions				
			I <sub>1</sub>	l <sub>2</sub>	l <sub>3</sub>	14	
TR1/TR2 (PNP)	1	10	-0.7 mA	-0.8 mA	0.45 mA	0.55 mA	

50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

# 12. Package outline



## 13. Soldering



50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

# 14. Revision history

### Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PIMP31PA v.1	20230831	Product data sheet	-	-

### 50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$

## 15. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <a href="https://www.nexperia.com">https://www.nexperia.com</a>.

#### **Definitions**

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

#### **Disclaimers**

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal

injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <a href="http://www.nexperia.com/profile/terms">http://www.nexperia.com/profile/terms</a>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by sustained.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

#### **Trademarks**

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

PIMP31PA

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2023. All rights reserved

### 50 V, 500 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$

## **Contents**

General description	1
Features and benefits	1
Applications	. 1
Quick reference data	1
Pinning information	2
Ordering information	2
Marking	2
Limiting values	. 3
Thermal characteristics	. 4
Characteristics	7
Test information	10
Package outline	11
Soldering	11
Revision history	12
Legal information	13
	Features and benefits

For more information, please visit: http://www.nexperia.com For sales office addresses, please send an email to: salesaddresses@nexperia.com Date of release: 31 August 2023

<sup>©</sup> Nexperia B.V. 2023. All rights reserved

# 单击下面可查看定价,库存,交付和生命周期等信息

>>Nexperia(安世)