



# BUK6Y14-40P

40 V, P-channel Trench MOSFET

16 March 2020

Product data sheet

## 1. General description

P-channel enhancement mode MOSFET in an LFPAK56 (Power SO8) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

This product has been designed and qualified to AEC-Q101 standard for use in high-performance automotive applications such as reverse battery protection.

## 2. Features and benefits

- High thermal power dissipation capability
- Suitable for thermally demanding environments due to 175 °C rating
- Trench MOSFET technology
- AEC-Q101 qualified

## 3. Applications

- Reverse battery protection
- Power management
- High-side loadswitch
- Motor drive

## 4. Quick reference data

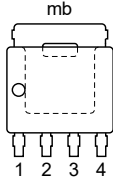
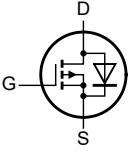
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-40	V
$V_{GS}$	gate-source voltage	[1]	-20	-	20	V
$I_D$	drain current	$V_{GS} = -10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	-64	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$	-	-	110	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -10.8\text{ A}; T_j = 25\text{ °C}$	-	11	14	mΩ

[1]  $V_{GS} = -20\text{ V}/+5\text{ V}$  according AEC-Q101 at  $T_j = 175\text{ °C}$ ;  $V_{GS} = -20\text{ V}/+20\text{ V}$  according AEC-Q101 at  $T_j = 150\text{ °C}$

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFPAK56; Power-SO8 (SOT669)</p>	 <p>017aaa094</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6Y14-40P	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK6Y14-40P	6Y1440P

## 8. Limiting values

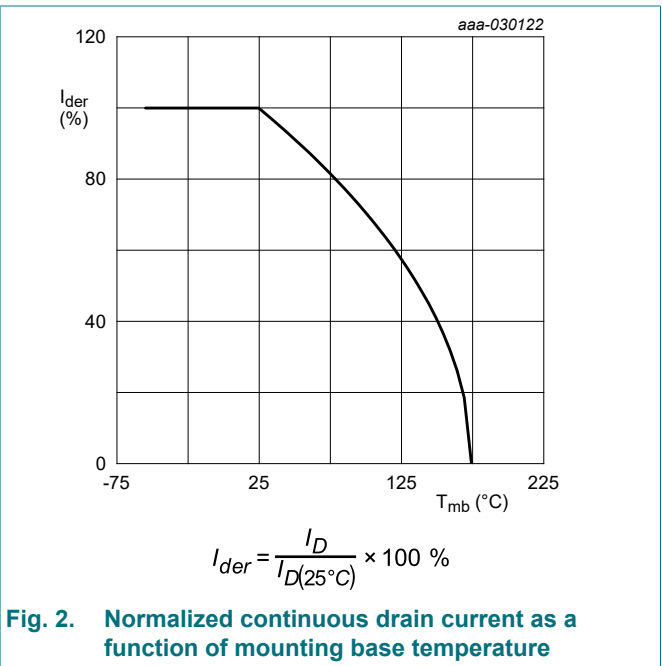
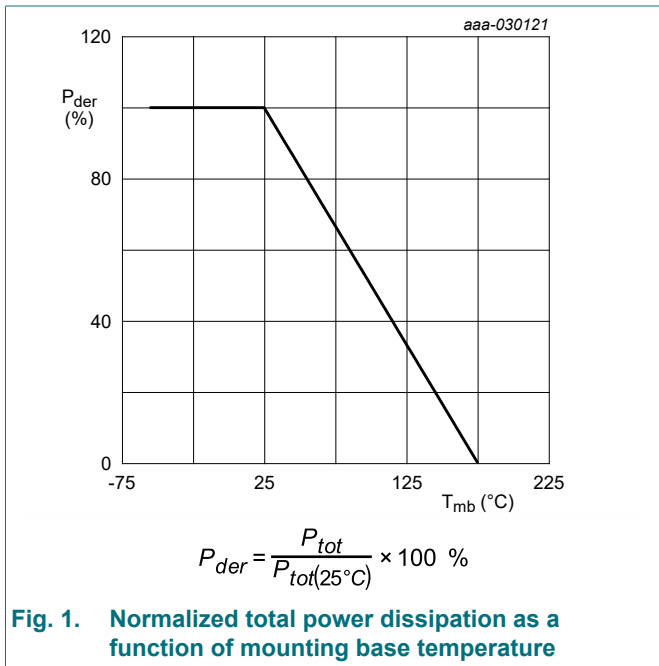
**Table 5. Limiting values**

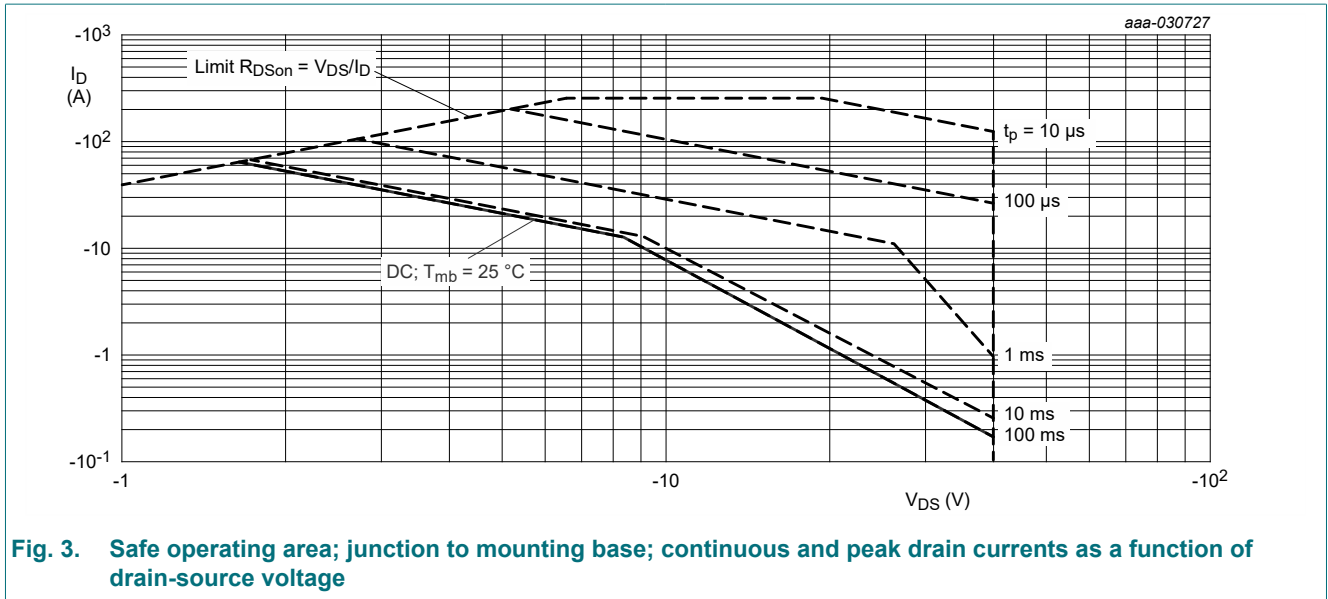
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C	-	-40	V
V <sub>GS</sub>	gate-source voltage	[1]	-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -10 V; T <sub>mb</sub> = 25 °C	-	-64	A
		V <sub>GS</sub> = -10 V; T <sub>mb</sub> = 100 °C	-	-46	A
I <sub>DM</sub>	peak drain current	single pulse; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	-257	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C	-	110	W
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>amb</sub>	ambient temperature		-55	175	°C
T <sub>stg</sub>	storage temperature		-65	175	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	-64	A
I <sub>SM</sub>	peak source current	single pulse; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	-257	A
<b>ESD maximum rating</b>					
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[2]	1000	V
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	T <sub>j(initial)</sub> = 25 °C; I <sub>D</sub> = -4.6 A; DUT in avalanche (unclamped)	-	94	mJ

[1] V<sub>GS</sub> = -20 V/+5 V according AEC-Q101 at T<sub>j</sub> = 175 °C; V<sub>GS</sub> = -20 V/+20 V according AEC-Q101 at T<sub>j</sub> = 150 °C

[2] Measured between all pins.





### 9. Thermal characteristics

Table 6. Thermal characteristics

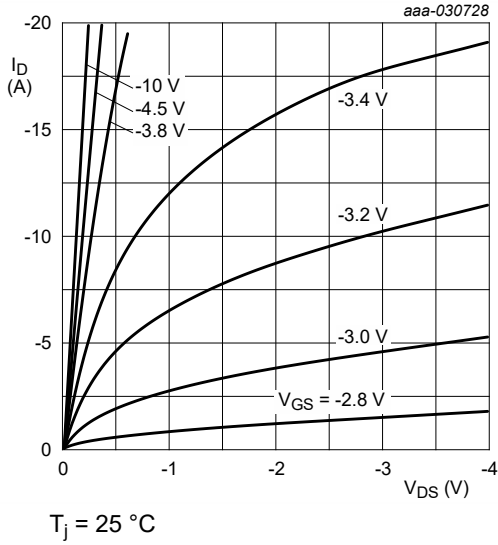
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	1.1	1.4	K/W



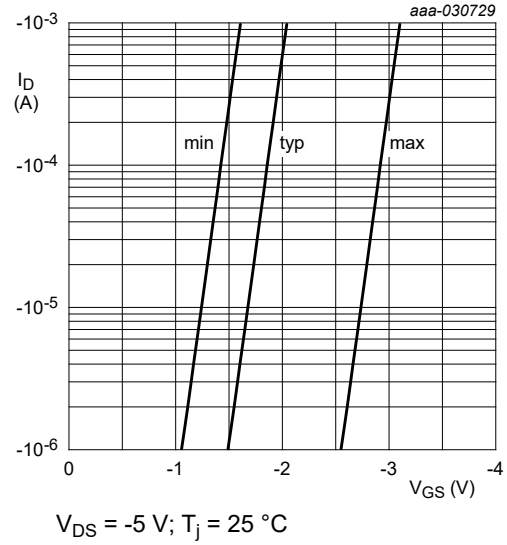
## 10. Characteristics

Table 7. Characteristics

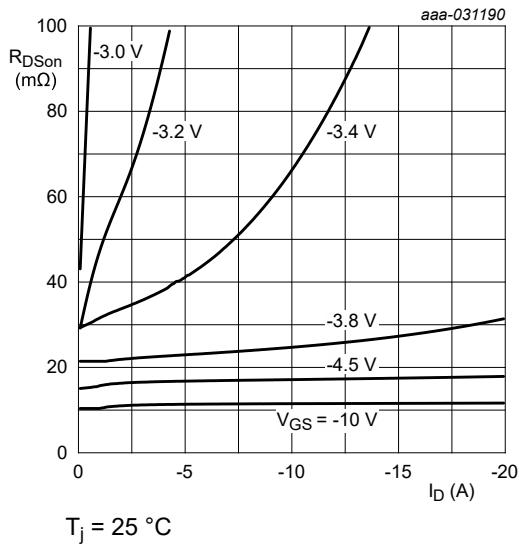
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-40	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	-1.5	-2	-3	V
$I_{DSS}$	drain leakage current	$V_{DS} = -40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	-10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10 \text{ V}; I_D = -10.8 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	11	14	m $\Omega$
		$V_{GS} = -10 \text{ V}; I_D = -10.8 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$	-	21	25	m $\Omega$
		$V_{GS} = -4.5 \text{ V}; I_D = -8.1 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	17	25	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 \text{ V}; I_D = -4.8 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	20	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	8.83	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -20 \text{ V}; I_D = -10.8 \text{ A}; V_{GS} = -10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	42.7	64	nC
$Q_{GS}$	gate-source charge		-	7.1	-	nC
$Q_{GD}$	gate-drain charge		-	9.3	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -20 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2300	-	pF
$C_{oss}$	output capacitance		-	315	-	pF
$C_{rss}$	reverse transfer capacitance		-	183	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -20 \text{ V}; I_D = -10.8 \text{ A}; V_{GS} = -10 \text{ V}; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	10	-	ns
$t_r$	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	82	-	ns
$t_f$	fall time		-	555	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -64.4 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-0.7	-1.2	V
$t_{rr}$	reverse recovery time	$I_S = -64.4 \text{ A}; dI_S/dt = 100 \text{ A}/\mu\text{s}; V_{GS} = -10 \text{ V}; V_{DS} = -20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	32	-	ns
$Q_r$	recovered charge		-	18	-	nC



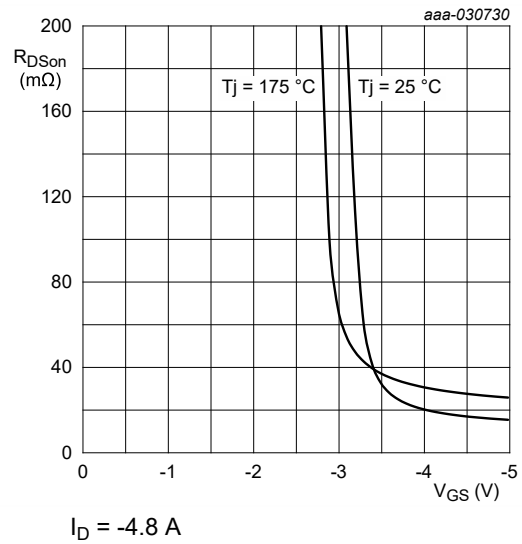
**Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



**Fig. 6. Sub-threshold drain current as a function of gate-source voltage**



**Fig. 7. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values**

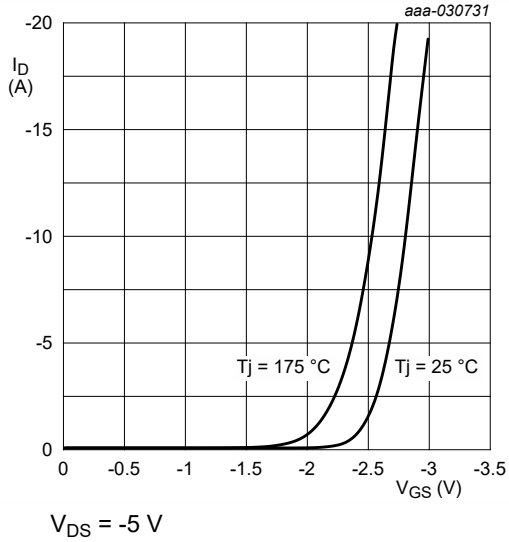
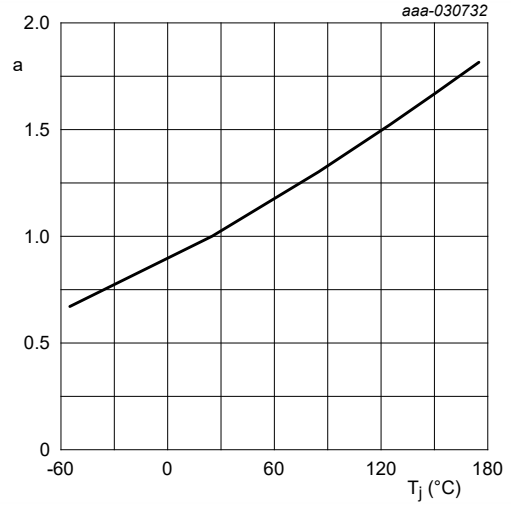
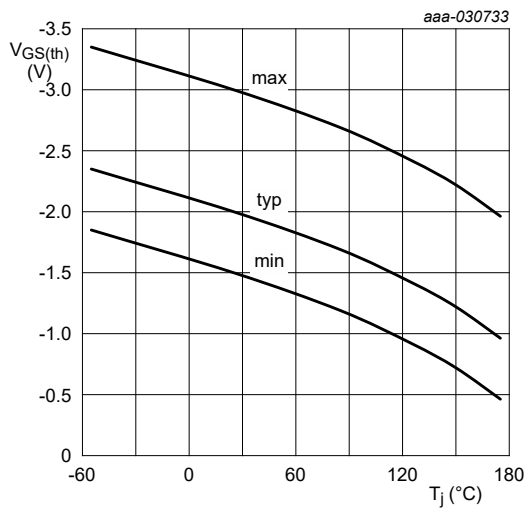


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



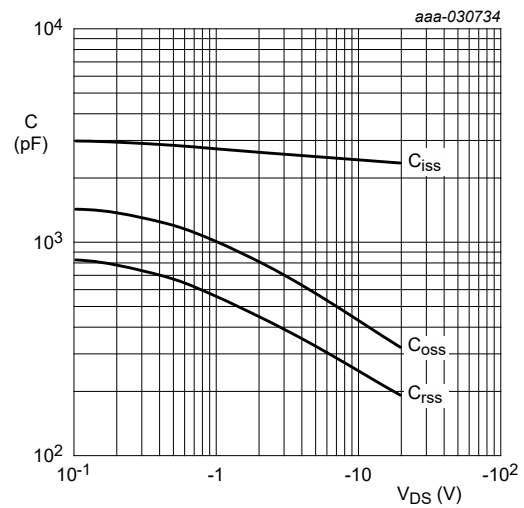
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig. 10. Normalized drain-source on-state resistance as a function of junction temperature; typical values



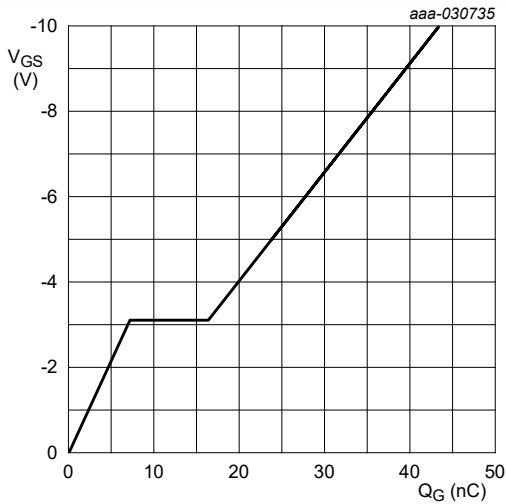
$I_D = -250\text{ }\mu\text{A}$ ;  $V_{DS} = V_{GS}$

Fig. 11. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}$ ;  $V_{GS} = 0\text{ V}$

Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = -20$  V;  $I_D = -4.8$  A;  $T_j = 25$  °C

Fig. 13. Gate-source voltage as a function of gate charge; typical values

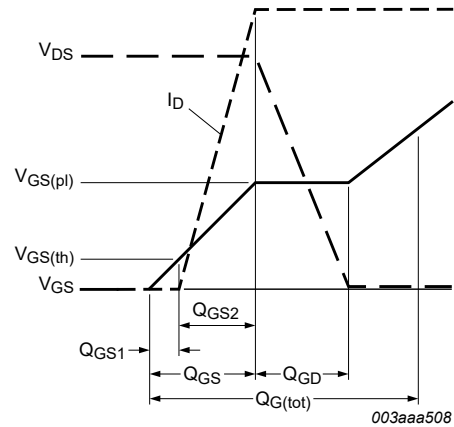
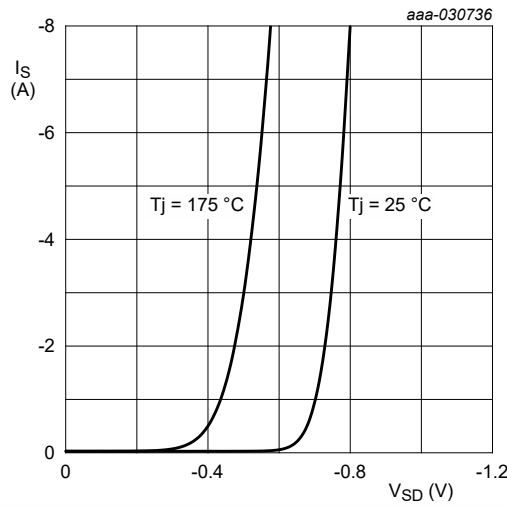


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0$  V

Fig. 15. Source current as a function of source-drain voltage; typical values



## 11. Test information

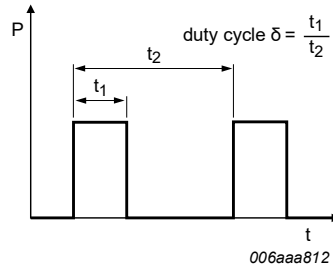
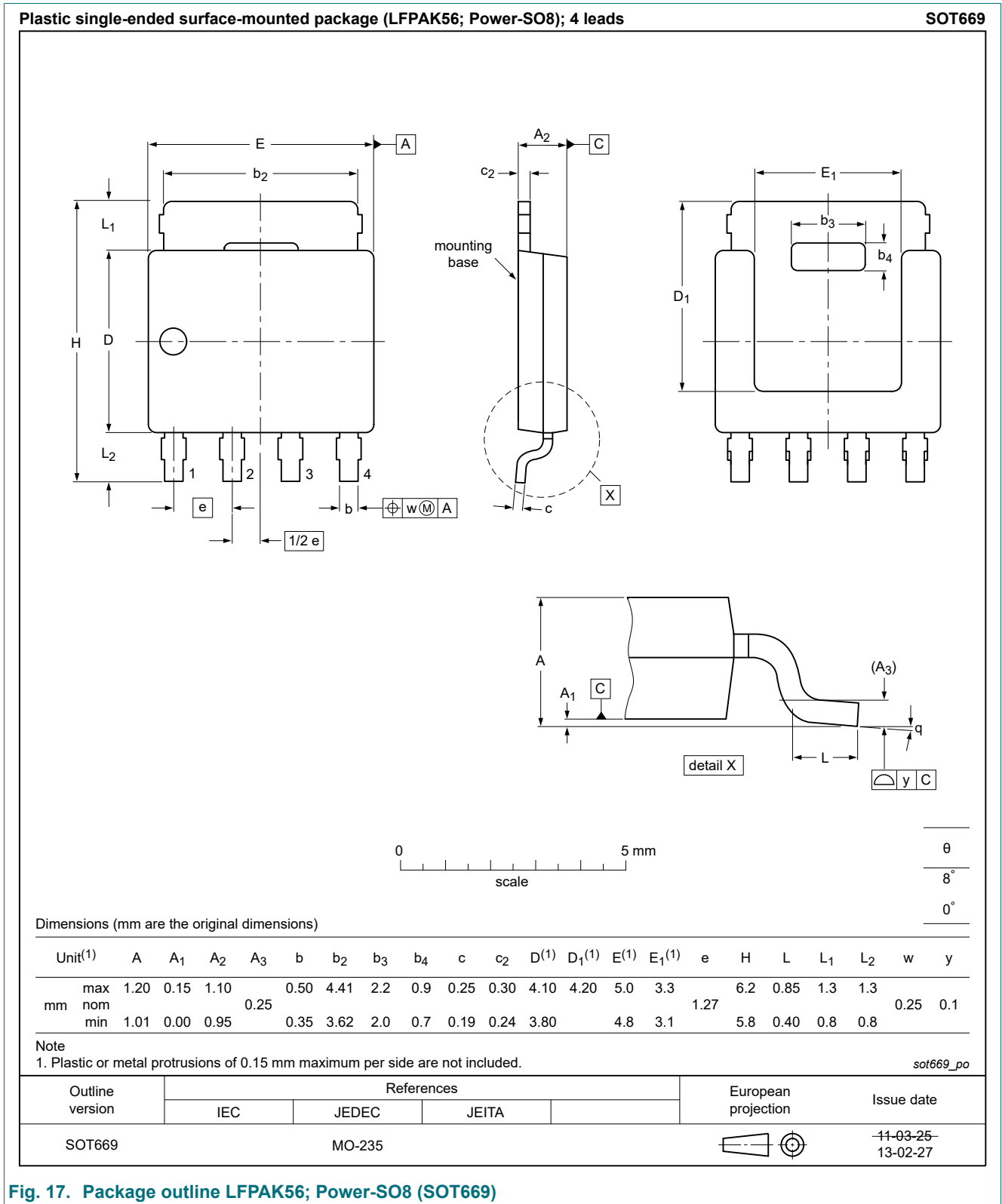


Fig. 16. Duty cycle definition

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

**12. Package outline**



**Fig. 17. Package outline LFAK56; Power-SO8 (SOT669)**

### 13. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6Y14-40P v.1	20200316	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Date of release: 16 March 2020

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