74ABT245

Octal transceiver with direction pin; 3-state

Rev. 6 — 24 June 2024 Product data sheet

1. General description

The 74ABT245 is an 8-bit transceiver with 3-state outputs. The device features an output enable ($\overline{OE}$) and send/receive (DIR) for direction control. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Octal bidirectional bus interface
- 3-State buffers
- Supply voltage range from 4.5 to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Output capability: +64 mA/–32 mA
- Power-up 3-State
- Live insertion/extraction permitted
- Inputs are disabled during 3-state mode
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT245D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ABT245PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

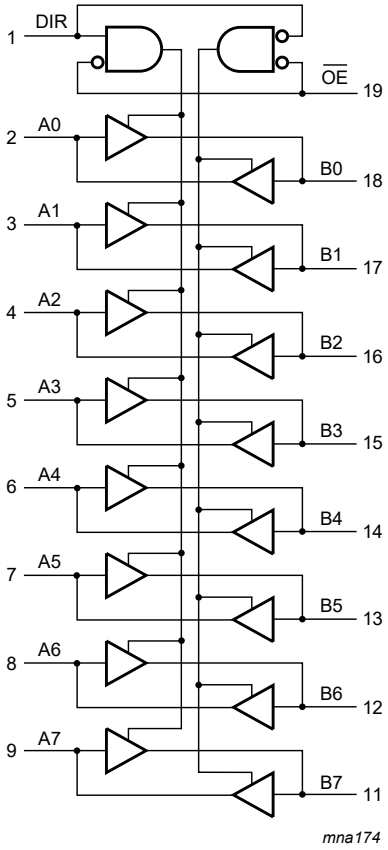


Fig. 1. Logic diagram

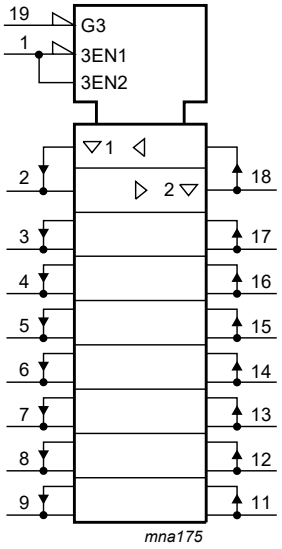
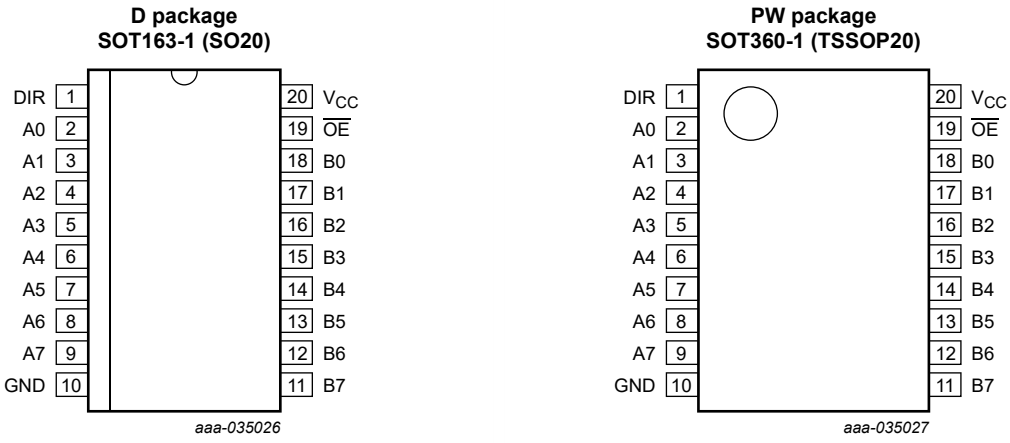


Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control input
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B0, B1, B2, B3, B4, B5, B6, B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
$\overline{OE}$	19	output enable input (active LOW)
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

Input		Input/output	
$\overline{OE}$	DIR	An	Bn
L	L	output An = Bn	input
L	H	input	output Bn = An
H	X	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW-state	-	128	mA
T_j	junction temperature	[2]	-	150	°C
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
I_{OH}	HIGH-level output current		-	-	-32	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −45 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = -18 mA	-1.2	-0.9	-	-1.2	-	V
V_{IH}	HIGH-level input voltage		2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}						
		I_{OH} = -3 mA	2.5	2.9	-	2.5	-	V
		I_{OH} = -32 mA	2.0	2.4	-	2.0	-	V
		V_{CC} = 5.0 V; V_I = V_{IL} or V_{IH}						
		I_{OH} = -3 mA	3.0	3.4	-	3.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}; I_{OL} = 64 mA	-	0.42	0.55	-	0.55	V
I_I	input leakage current	Control pins; V_{CC} = 5.5 V; V_I = GND or 5.5 V	-	±0.01	±1.0	-	±1.0	µA
		Data pins; V_{CC} = 5.5 V; V_I = GND or 5.5 V	-	±5	±100	-	±100	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_O or V_I ≤ 4.5 V	-	±5.0	±100	-	±100	µA
$I_{O(pu/pd)}$	power-up/ power-down output current	V_{CC} = 2.0 V; V_O = 0.5 V; V_I = GND or V_{CC}; $\overline{OE}$ = don't care [1]	-	±5.0	±50	-	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}						
		output HIGH-state at V_O = 2.7 V	-	5.0	50	-	50	µA
		output LOW-state at V_O = 0.5 V	-	-5.0	-50	-	-50	µA
I_{CEX}	output high leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}	-	5.0	50	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V [2]	-40	-100	-180	-40	-180	mA

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −45 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}						
		outputs HIGH-state	-	50	250	-	250	µA
		outputs LOW-state	-	24	30	-	30	mA
		outputs disabled	-	50	250	-	250	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V						
		outputs enabled; one input at 3.4 V and other inputs at V_{CC} or GND [3]	-	0.5	1.5	-	1.5	mA
		outputs disabled; one data input at 3.4 V and other inputs at V_{CC} or GND [3]	-	50	250	-	250	µA
		outputs disabled; one enable input at 3.4 V and other inputs at V_{CC} or GND [3]	-	0.5	1.5	-	1.5	mA
C_I	input capacitance	DIR; $\overline{OE}$; V_I = 0 V or V_{CC}	-	4	-	-	-	pF
$C_{I/O}$	input/output capacitance	outputs disabled; V_O = 0 V or V_{CC}	-	7	-	-	-	pF

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 % a transition time of up to 100 µs is permitted.
[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
[3] This is the increase in supply current for each input at 3.4 V.

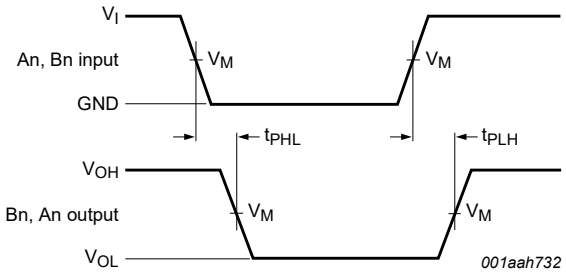
10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	T_{amb} = 25 °C; V_{CC} = 5.0 V			T_{amb} = −40 °C to 85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An; see Fig. 3	1.0	2.2	4.1	1.0	4.6	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An; see Fig. 3	1.0	2.9	4.2	1.0	4.6	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$ to An or Bn; see Fig. 4	1.3	3.0	4.8	1.3	5.3	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to An or Bn; see Fig. 4	2.3	4.0	5.8	2.3	6.3	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to An or Bn; see Fig. 4	1.0	4.7	6.2	1.0	7.2	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to An or Bn; see Fig. 4	1.0	4.1	5.8	1.0	6.3	ns

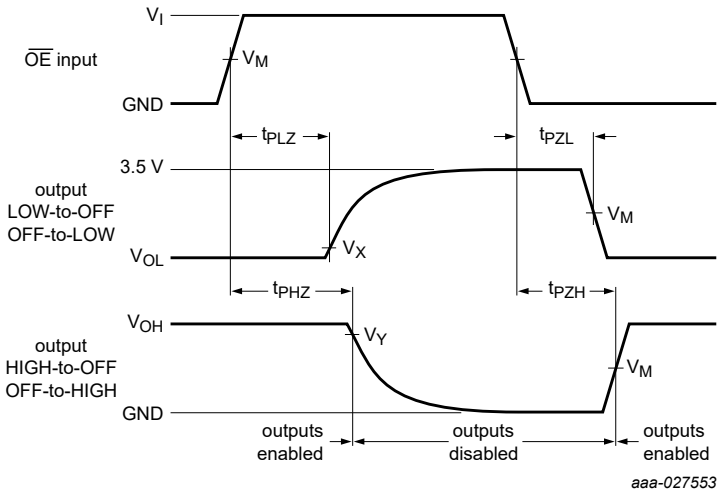
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig. 3. Input (An or Bn) to output (Bn or An) propagation delays



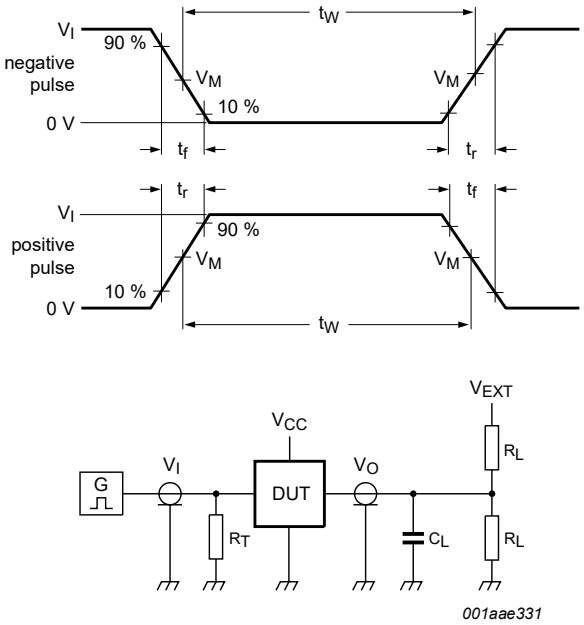
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig. 4. 3-state output enable and disable propagation delays

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = Test voltage for switching times.

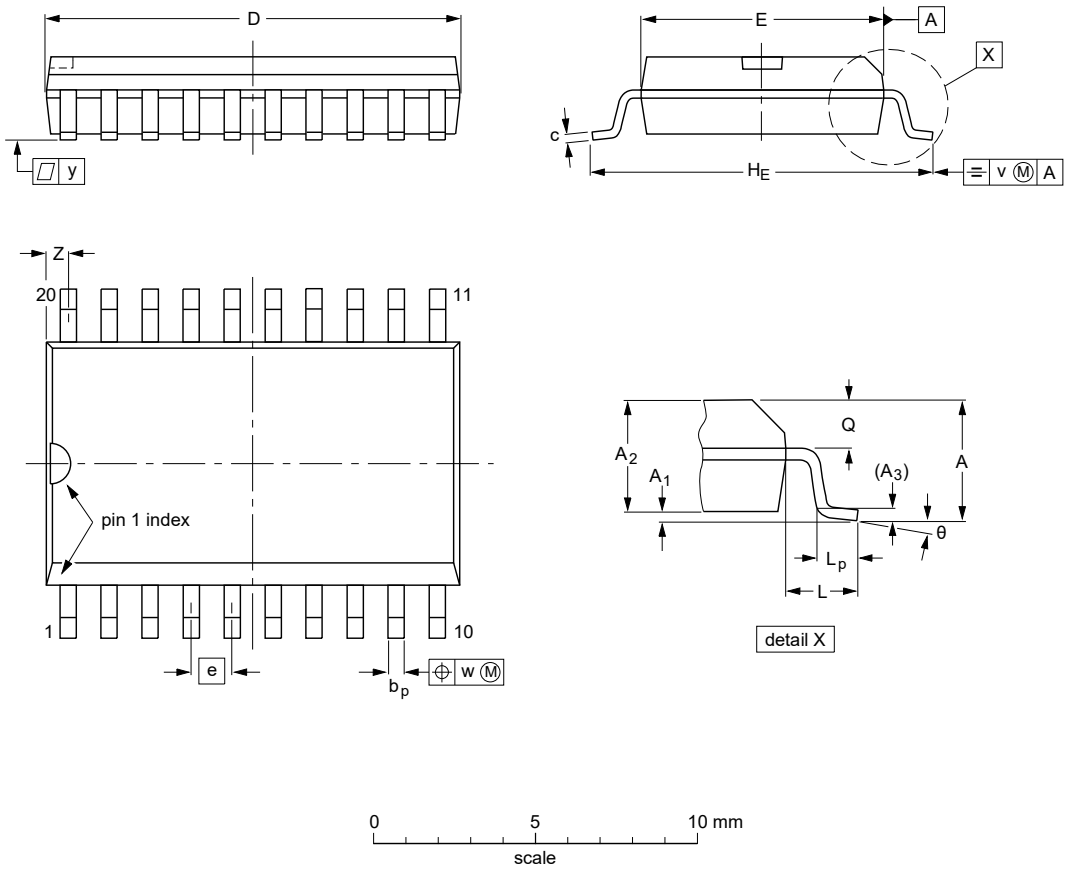
Fig. 5. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3.0 V	≤ 1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	7 V	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

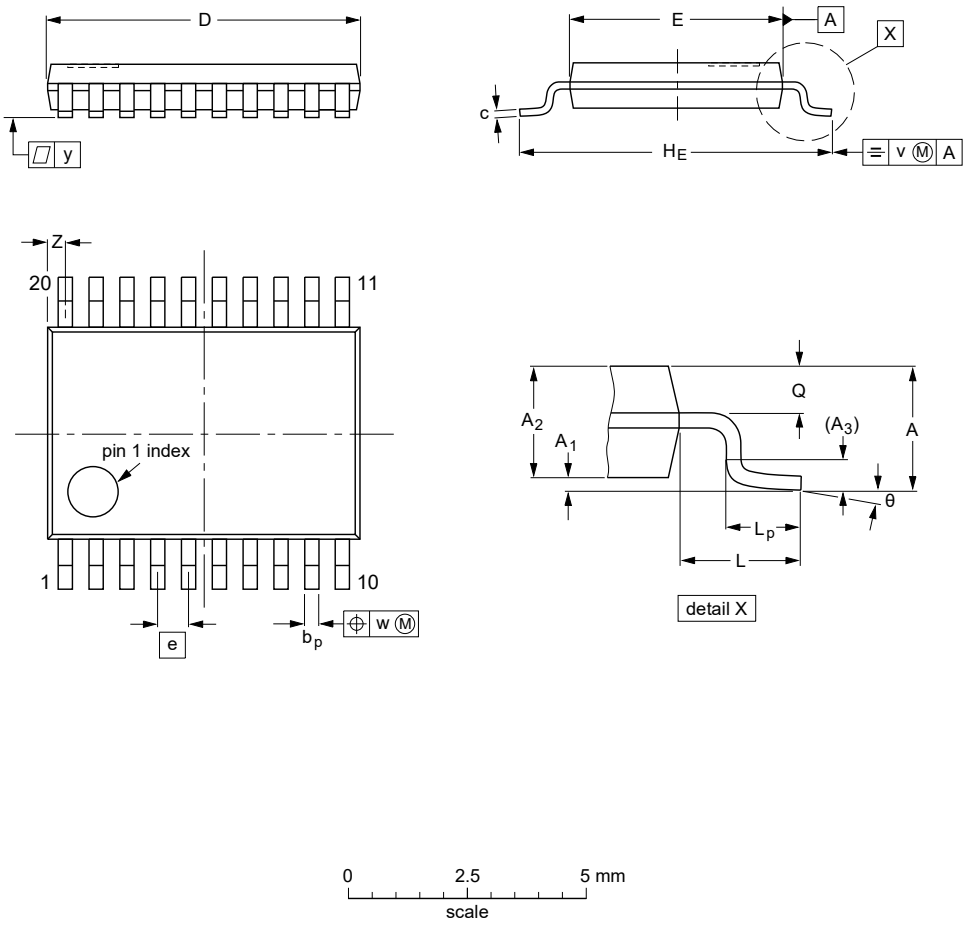
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig. 6. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 7. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT245 v.6	20240624	Product data sheet	-	74ABT245 v.5
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74ABT245 v.5	20210709	Product data sheet	-	74ABT245 v.4
Modifications:	• Section 1 and Section 2 updated. • Type number 74ABT245DB (SOT339-1 / SSOP20) removed.			
74ABT245 v.4	20171006	Product data sheet	-	74ABT245 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74ABT245 v.3	20030206	Product data sheet	ECN 853-1447 29305	74ABT245 v.2
Modifications:	• Delete all references to N package. DIP20 package option discontinued.			
74ABT245 v.2	19980116	Product specification	ECN 853-1447 18867	74ABT245 v.1
74ABT245 v.1	19960910	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

Date of release: 24 June 2024

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