



PMV35EPE

30 V, P-channel Trench MOSFET

6 July 2016

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic level compatible
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

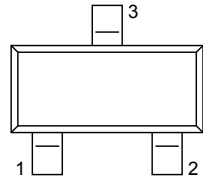
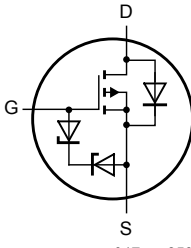
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-	-30	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t \leq 5\text{ s}$	[1]	-	-	-5.3	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -4.2\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$		-	35	45	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 TO-236AB (SOT23)	 017aaa259
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV35EPE	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PMV35EPE	EK%

[1] % = placeholder for manufacturing site code

8. Limiting values

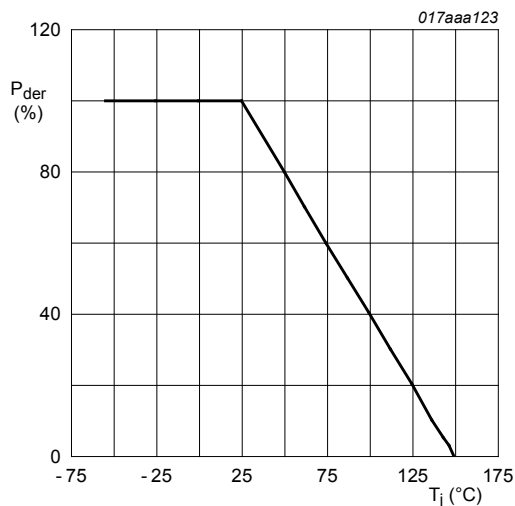
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-30	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = -10 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-5.3	A
		V _{GS} = -10 V; T _{amb} = 25 °C	[1]	-	-4.2	A
		V _{GS} = -10 V; T _{amb} = 100 °C	[1]	-	-2.7	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-17	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	480	mW
			[1]	-	1.2	W
		T _{sp} = 25 °C		-	6.95	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-4	A

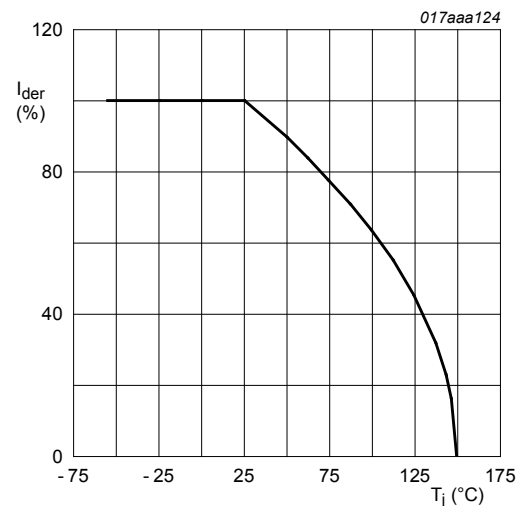
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



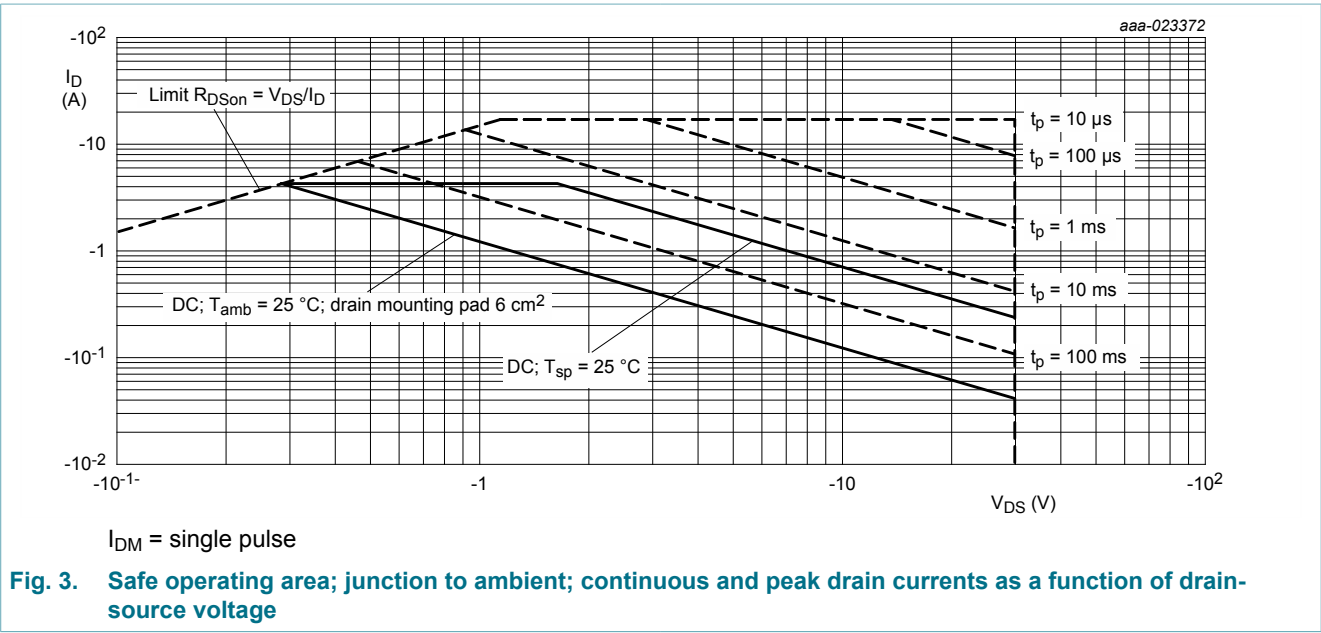
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

Fig. 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

Fig. 2. Normalized continuous drain current as a function of junction temperature

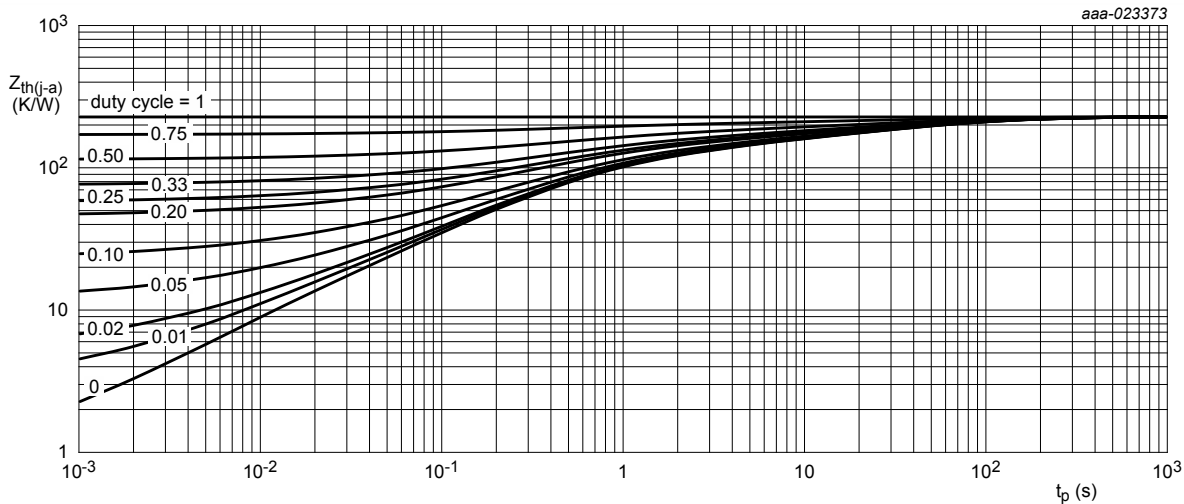


9. Thermal characteristics

Table 6. Thermal characteristics

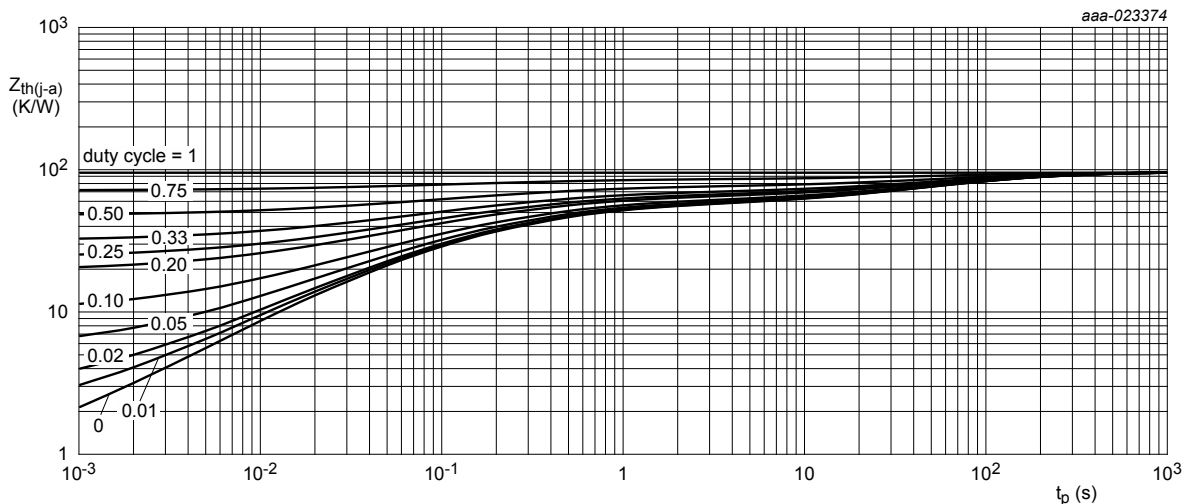
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	227	261	K/W
			[2]	-	91	104	K/W
		$t \leq 5\text{ s}$	[2]	-	57	66	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	13	18	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-30	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} =V _{GS} ; T _j = 25 °C		-1	-2	-3	V
I _{DSS}	drain leakage current	V _{DS} = -30 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	2	μA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-2	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -4.2 A; T _j = 25 °C		-	35	45	mΩ
		V _{GS} = -10 V; I _D = -4.2 A; T _j = 150 °C		-	51	67	mΩ
		V _{GS} = -4.5 V; I _D = -3.3 A; T _j = 25 °C		-	49	72	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -4.2 A; T _j = 25 °C		-	13.5	-	S
R _G	gate resistance	f = 1 MHz		-	13	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -15 V; I _D = -4.2 A; V _{GS} = -10 V; T _j = 25 °C		-	12.8	19.2	nC
Q _{GS}	gate-source charge			-	2.2	-	nC
Q _{GD}	gate-drain charge			-	2.2	-	nC
C _{iss}	input capacitance	V _{DS} = -15 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	793	-	pF
C _{oss}	output capacitance			-	134	-	pF
C _{rss}	reverse transfer capacitance			-	84	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -15 V; I _D = -4.2 A; V _{GS} = -10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	6	-	ns
t _r	rise time			-	19	-	ns
t _{d(off)}	turn-off delay time			-	36	-	ns
t _f	fall time			-	19	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -4 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.8	-1.2	V

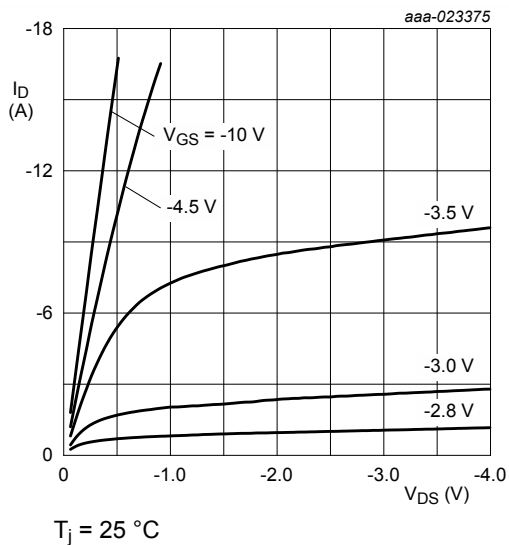


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

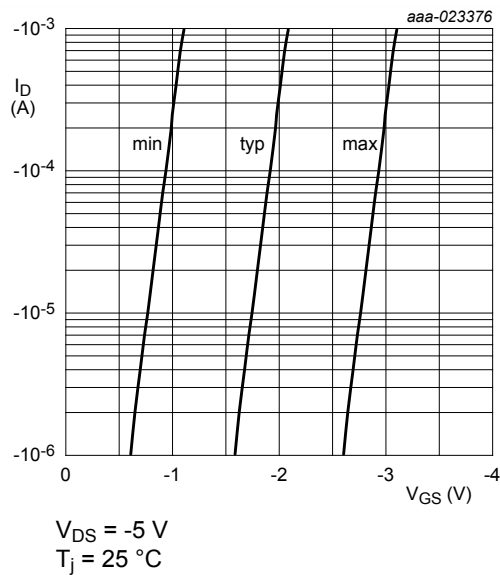


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

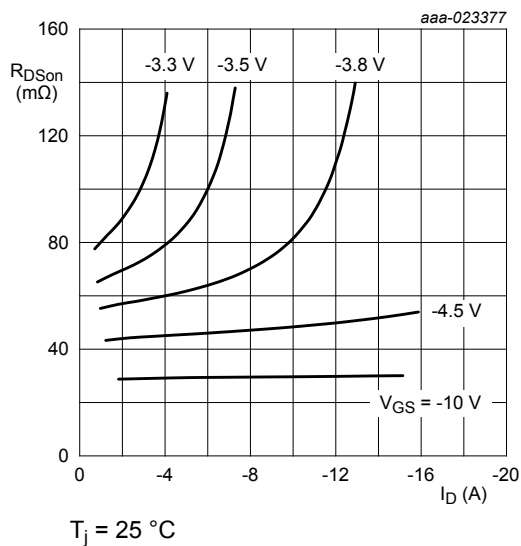


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

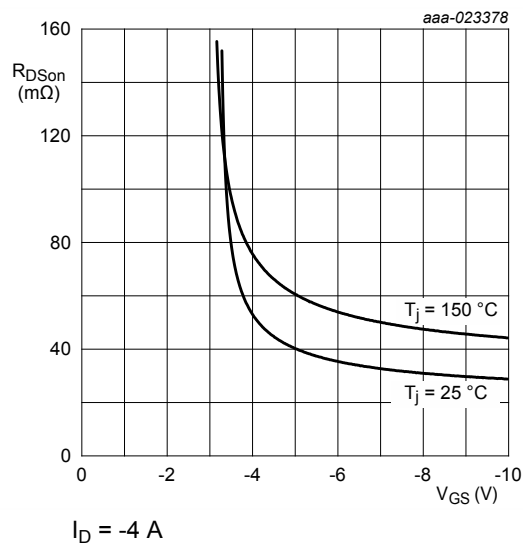


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

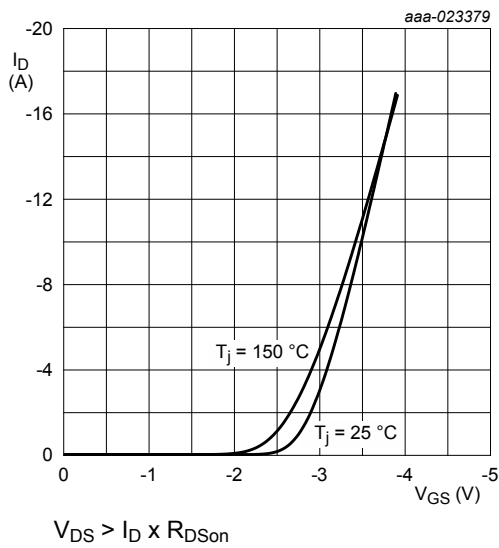


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

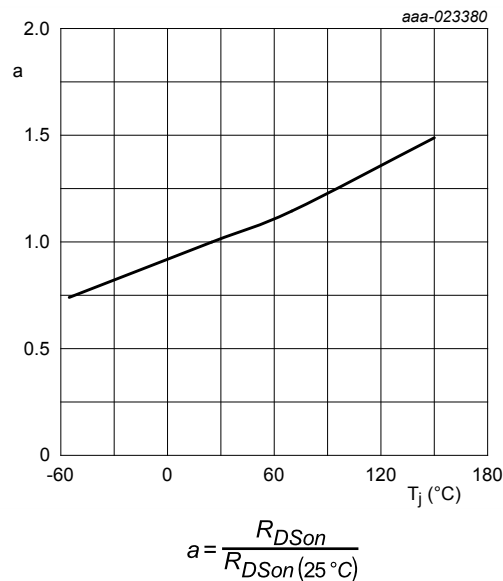


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

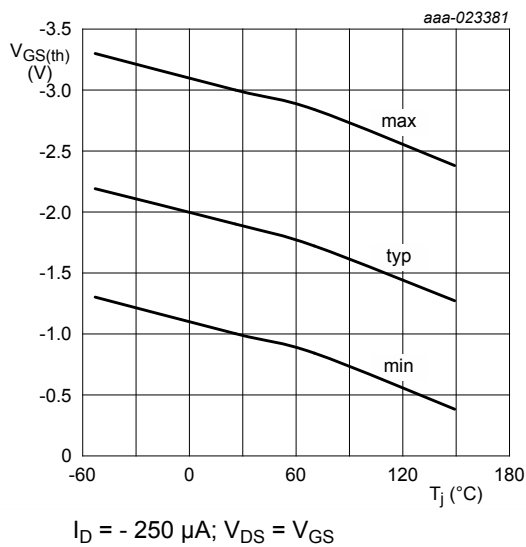


Fig. 12. Gate-source threshold voltage as a function of junction temperature

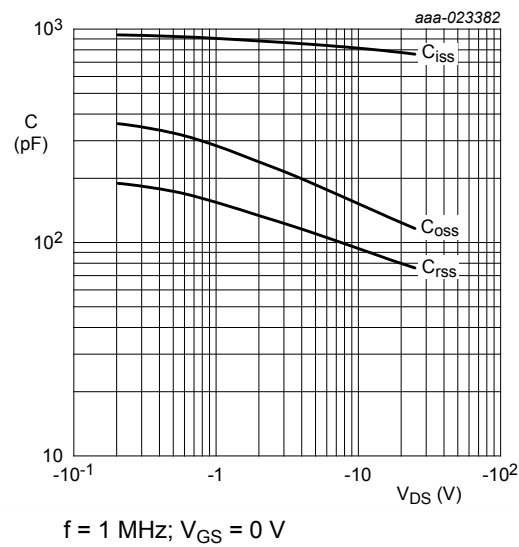


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

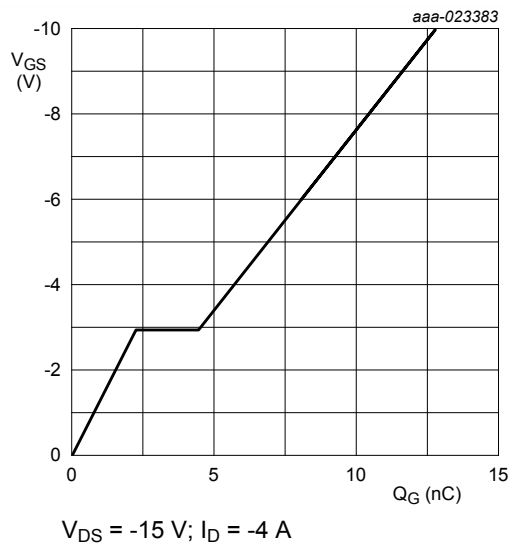


Fig. 14. Gate-source voltage as a function of gate charge; typical values

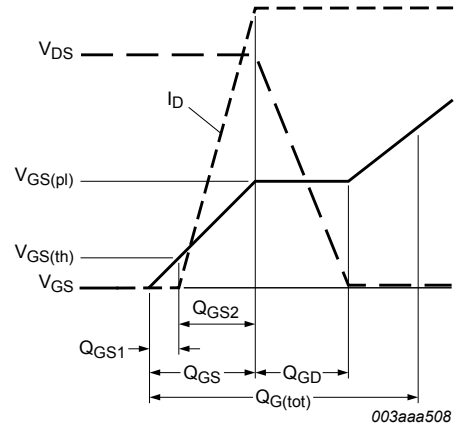


Fig. 15. Gate charge waveform definitions

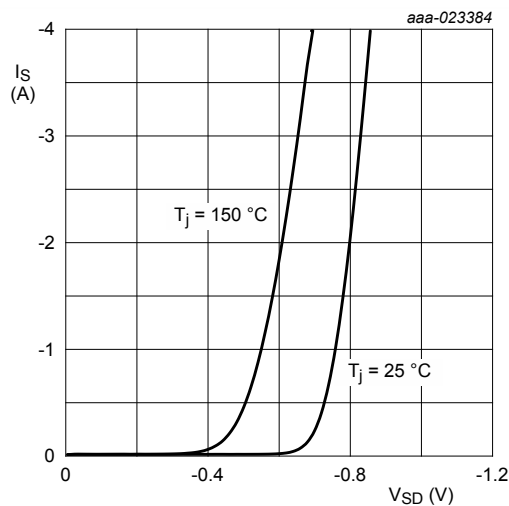


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

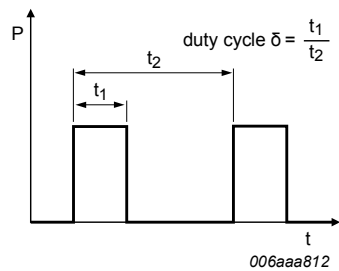


Fig. 17. Duty cycle definition

12. Package outline

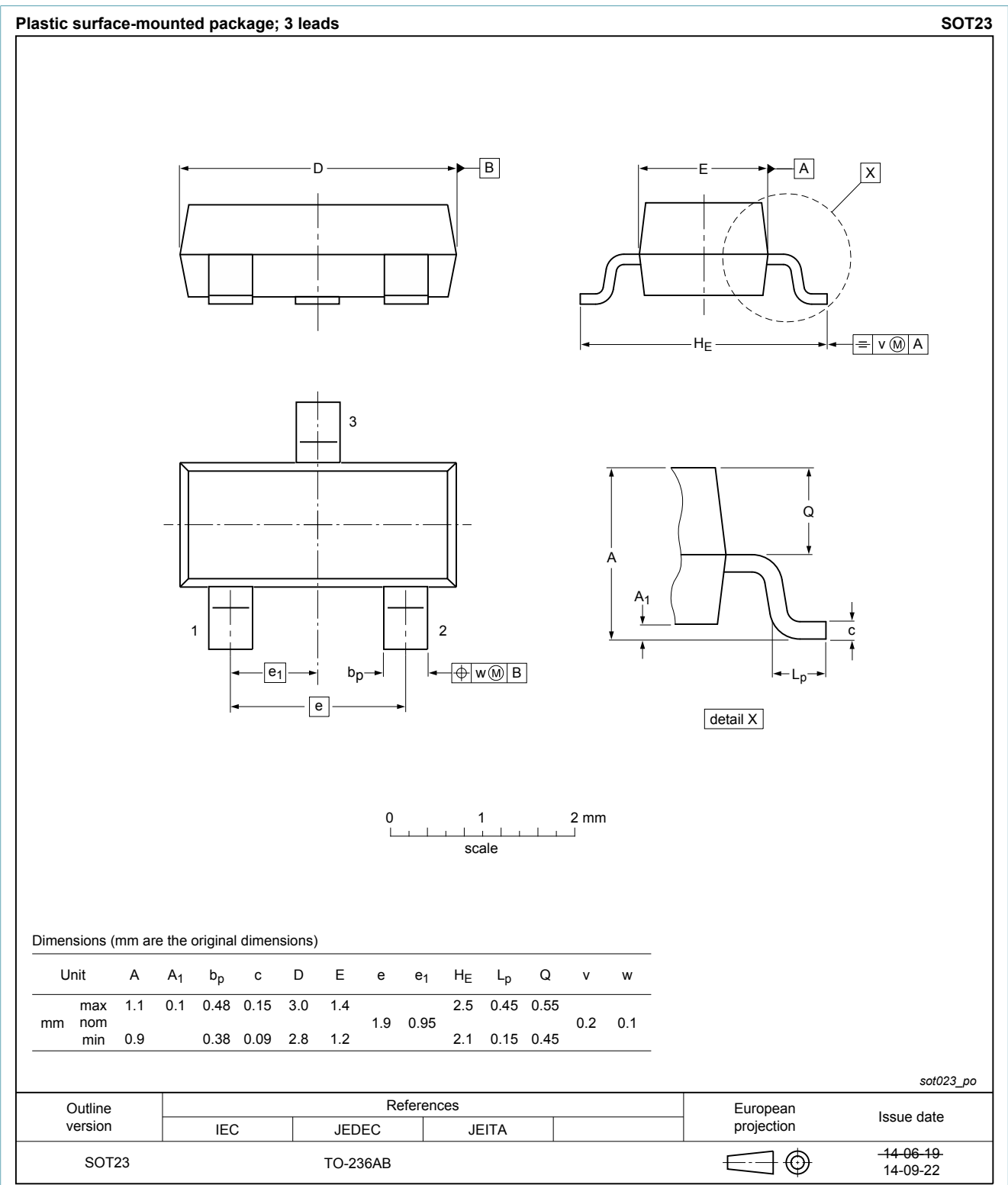


Fig. 18. Package outline TO-236AB (SOT23)

13. Soldering

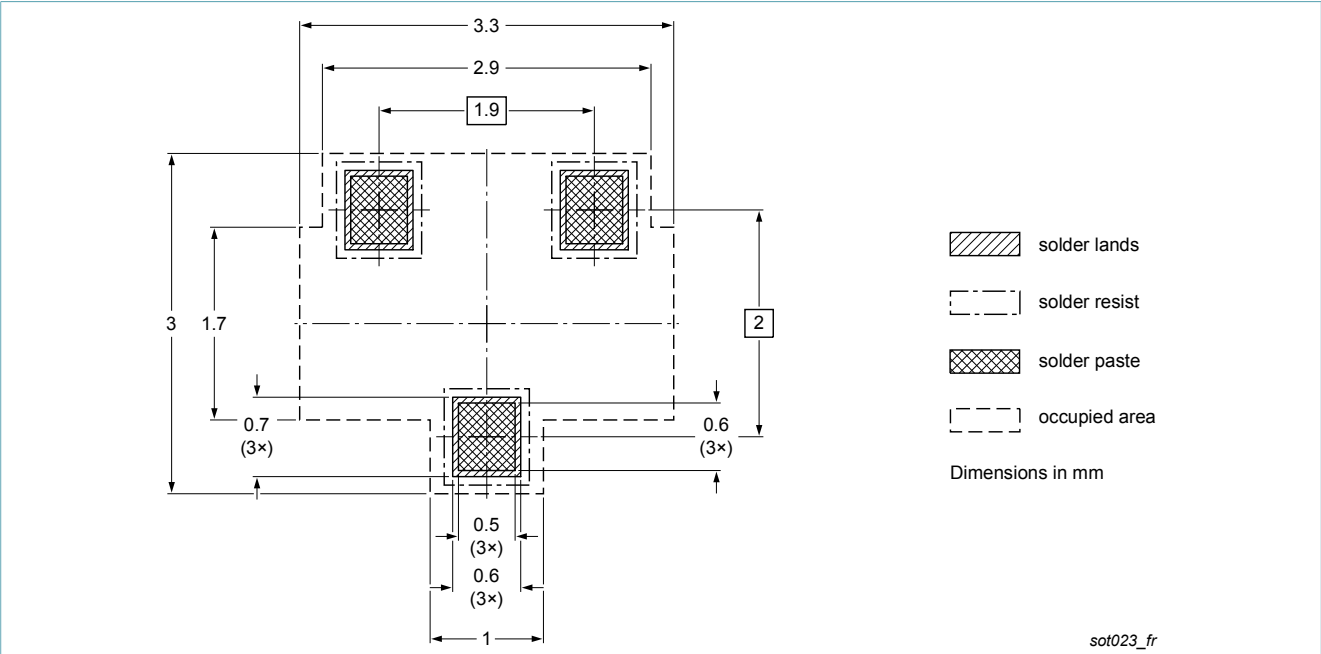


Fig. 19. Reflow soldering footprint for TO-236AB (SOT23)

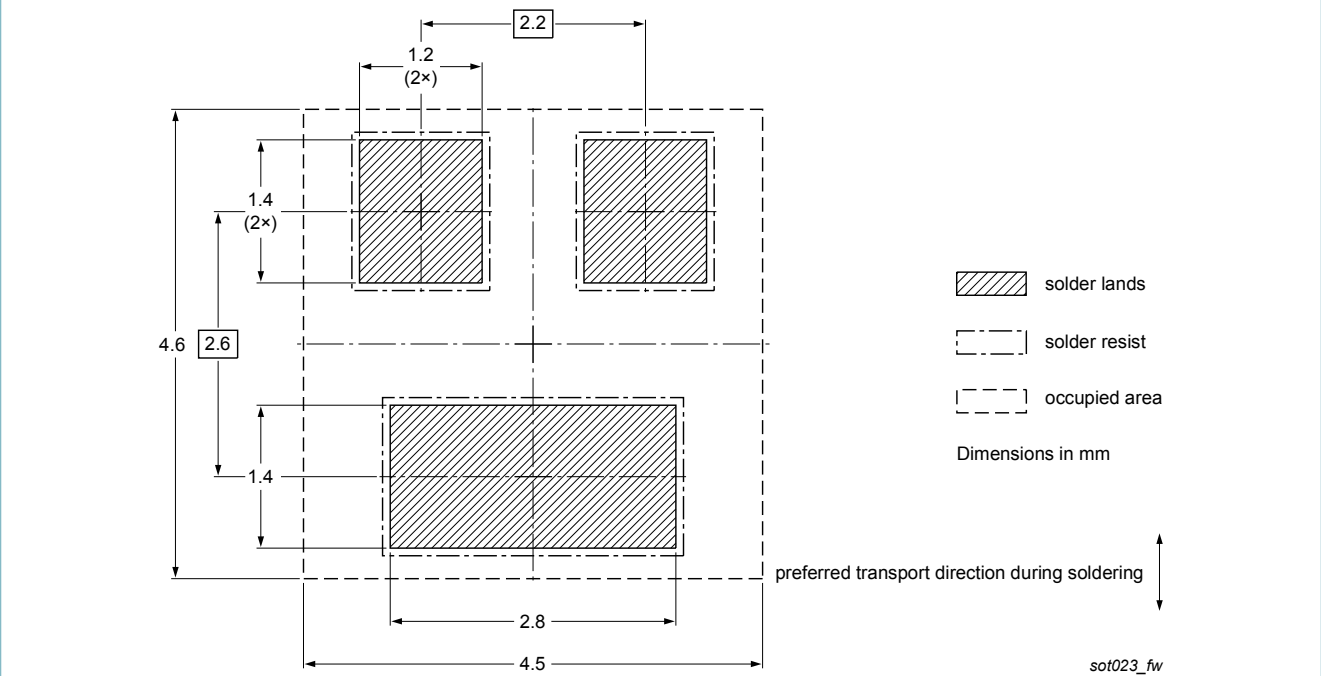


Fig. 20. Wave soldering footprint for TO-236AB (SOT23)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMV35EPE v.1	20160706	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 06 July 2016

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