

# CBT3253

## Dual 1-of-4 FET multiplexer/demultiplexer

Rev. 5 — 18 April 2024

Product data sheet

### 1. General description

The CBT3253 is a dual 1-of-4 high-speed TTL-compatible FET multiplexer/demultiplexer. The low ON-resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The select control inputs (S0, S1) can select the data path, when both output enable inputs ( $1\overline{OE}$ ,  $2\overline{OE}$ ) are LOW. When  $n\overline{OE}$  is HIGH, the switch terminals are in the high impedance OFF-state, independent of S0 and S1.

### 2. Features and benefits

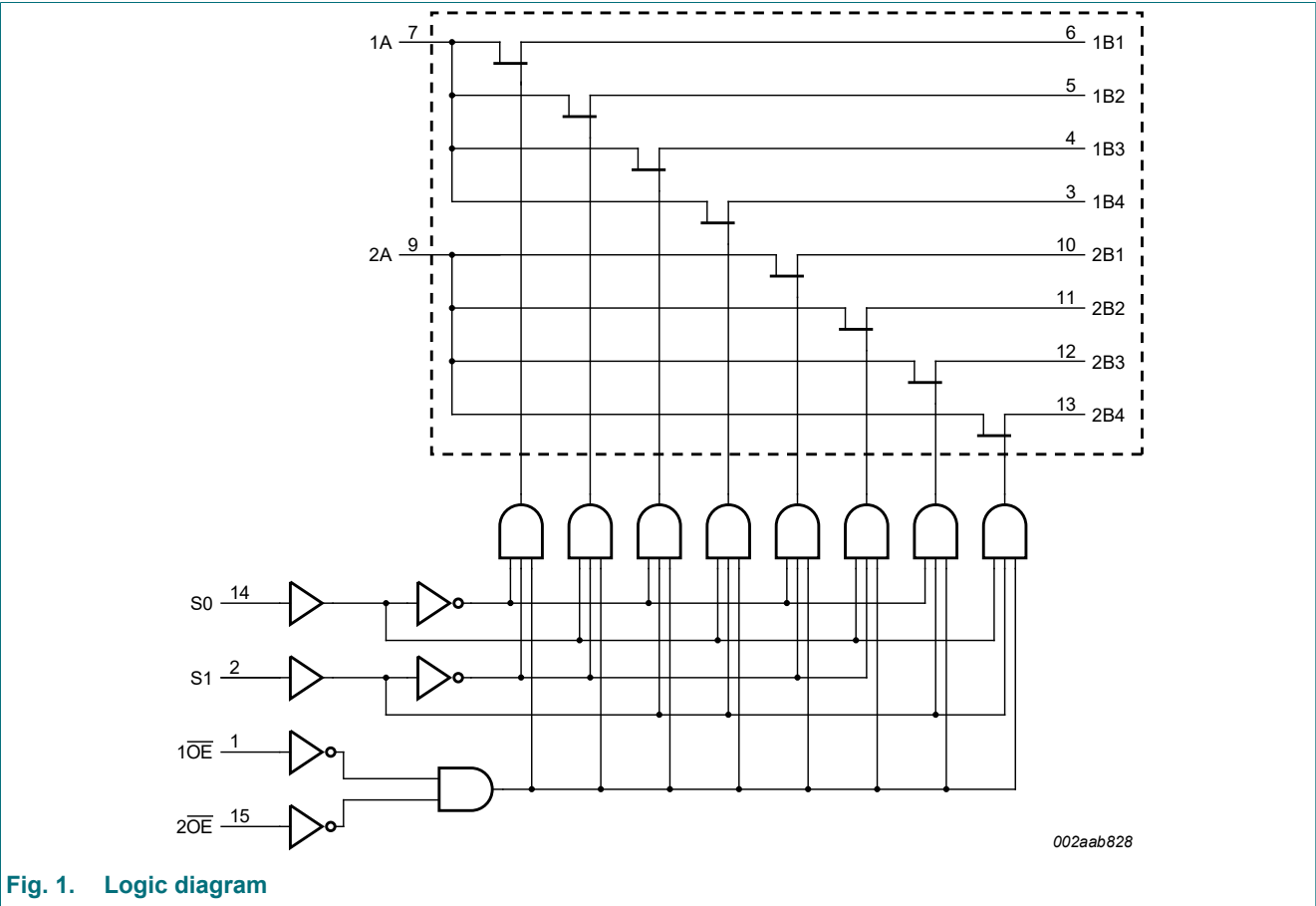
- 5  $\Omega$  switch connection between two ports
- Direct interface with TTL levels
- Overvoltage tolerant control inputs to 5.5 V
- Minimal propagation delay through the switch
- Latch-up protection exceeds 100 mA per JEDEC standard JESD78 class II level A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

### 3. Ordering information

Table 1. Ordering information

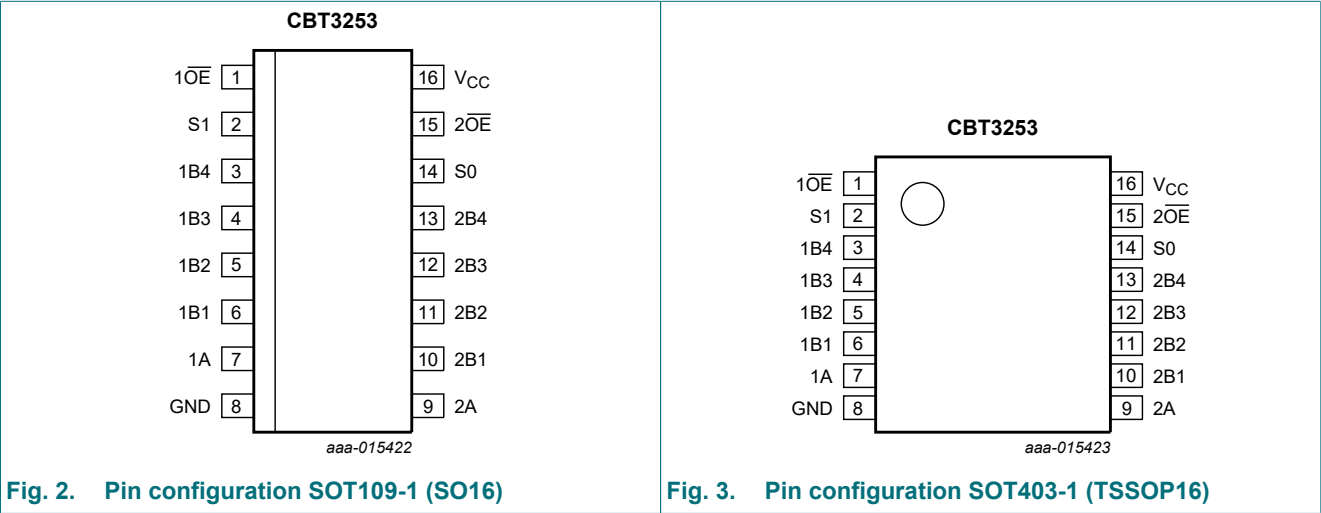
Type number	Temperature range	Package		
		Name	Description	Version
<a href="#">CBT3253D</a>	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	<a href="#">SOT109-1</a>
<a href="#">CBT3253PW</a>	-40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	<a href="#">SOT403-1</a>

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 15	output enable (active LOW)
S1, S0	2, 14	select control input
1B4, 1B3, 1B2, 1B1	3, 4, 5, 6	1B outputs/inputs
1A	7	1A input/output
GND	8	ground (0 V)
2A	9	2A input/output
2B1, 2B2, 2B3, 2B4	10, 11, 12, 13	2B outputs/inputs
V <sub>CC</sub>	16	positive supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Inputs				Switch
1OE	2OE	S1	S0	
X	H	X	X	disconnect 1A to 1Bn and 2A to 2Bn
H	X	X	X	disconnect 1A to 1Bn and 2A to 2Bn
L	L	L	L	1A to 1B1 and 2A to 2B1
L	L	L	H	1A to 1B2 and 2A to 2B2
L	L	H	L	1A to 1B3 and 2A to 2B3
L	L	H	H	1A to 1B4 and 2A to 2B4

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage	[1]	-0.5	+7.0	V
I <sub>SW</sub>	switch current	continuous current through each switch	-	128	mA
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		4.5	5.5	V
$V_{IH}$	HIGH-level input voltage		2.0	-	V
$V_{IL}$	LOW-level input voltage		-	0.8	V
$T_{amb}$	ambient temperature	operating in free-air	-40	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C.}$			Unit
			Min	Typ[1]	Max	
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5\text{ V}; I_I = -18\text{ mA}$	-	-	-1.2	V
$V_{pass}$	pass voltage	$V_I = V_{CC} = 5.0\text{ V}; I_O = -100\text{ }\mu\text{A}$	3.6	3.9	4.2	V
$I_I$	input leakage current	$V_{CC} = 5.5\text{ V}; V_I = \text{GND or } 5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{CC}$	supply current	$V_{CC} = 5.5\text{ V}; I_O = 0\text{ mA}; V_I = V_{CC} \text{ or GND}$	-	-	3	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input; $V_{CC} = 5.5\text{ V};$ one input at 3.4 V, other inputs at $V_{CC}$ or GND [2]	-	-	2.5	mA
$C_I$	input capacitance	control pins; $V_I = 3\text{ V or } 0\text{ V}$	-	4.5	-	pF
$C_{io(off)}$	off-state input/output capacitance	A port; $V_O = 3\text{ V or } 0\text{ V}; \overline{nOE} = V_{CC}$	-	11.4	-	pF
		B port; $V_O = 3\text{ V or } 0\text{ V}; \overline{nOE} = V_{CC}$	-	3.8	-	pF
$C_{io(on)}$	on-state input/output capacitance	A port and B port	-	18.6	-	pF
$R_{ON}$	ON resistance	$V_{CC} = 4.5\text{ V}$ [3]				
		$V_I = 0\text{ V}; I_I = 64\text{ mA}$	-	5	7	$\Omega$
		$V_I = 0\text{ V}; I_I = 30\text{ mA}$	-	5	7	$\Omega$
		$V_I = 2.4\text{ V}; I_I = -15\text{ mA}$	-	10	15	$\Omega$

[1] All typical values are measured at  $V_{CC} = 5\text{ V}; T_{amb} = 25\text{ °C}$ .  
[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.  
[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. The lowest voltage of the two (A or B) terminals determines the ON resistance.

10. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ; for test circuit, see Fig. 6.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$		Unit
			Min	Max	
$t_{pd}$	propagation delay	nA to nBn or nBn to nA; see Fig. 4 [1] [2]	-	0.25	ns
		Sn to nA; see Fig. 4 [1] [2]	1.2	6.2	ns
$t_{en}$	enable time	Sn to nBn; see Fig. 5 [2]	1.3	6.3	ns
		nOE to nA or nBn; see Fig. 5 [2]	1.4	6.4	ns
$t_{dis}$	disable time	Sn to nBn; see Fig. 5 [2]	1.1	7.2	ns
		nOE to nA or nBn; see Fig. 5 [2]	1.0	7	ns

- [1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance).
- [2]  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ ;  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ ;  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

10.1. Waveforms and test circuit

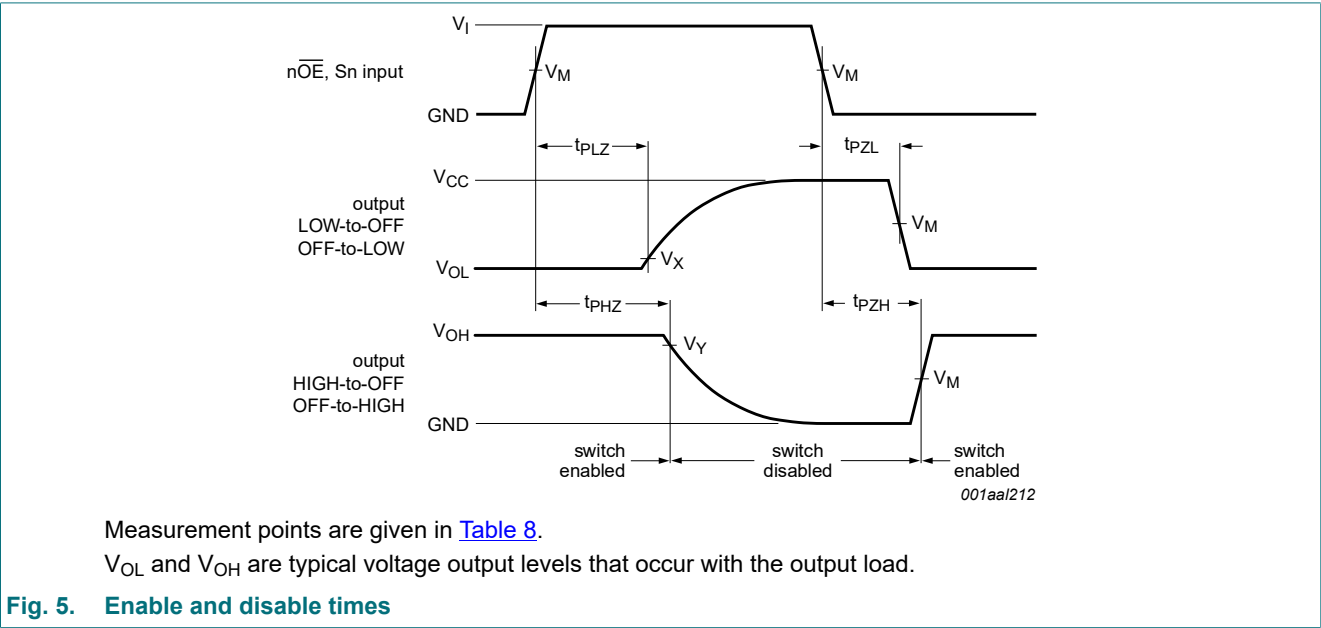
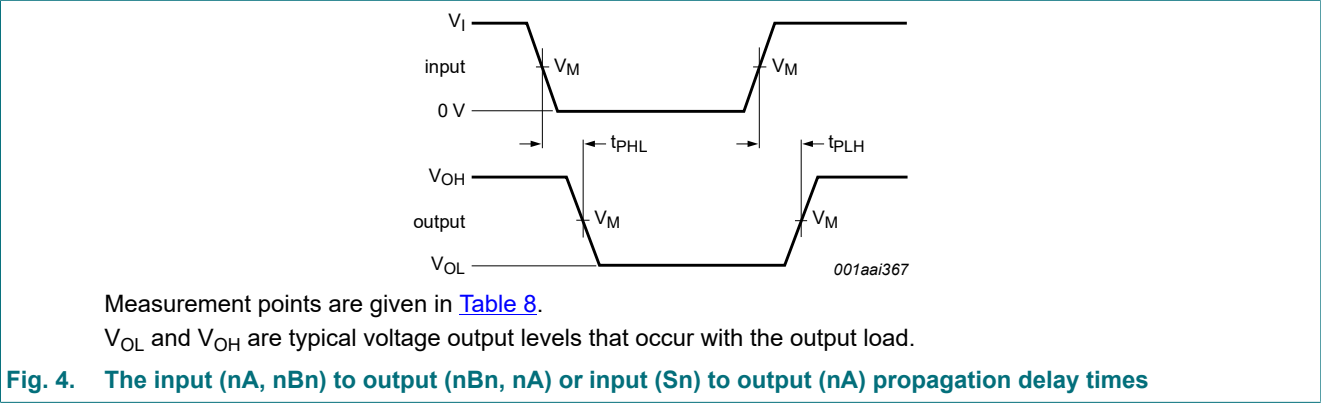


Table 8. Measurement points

Supply voltage	Input		Output		
V <sub>CC</sub>	V <sub>I</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
4.5 V to 5.5 V	GND to 3.0 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V

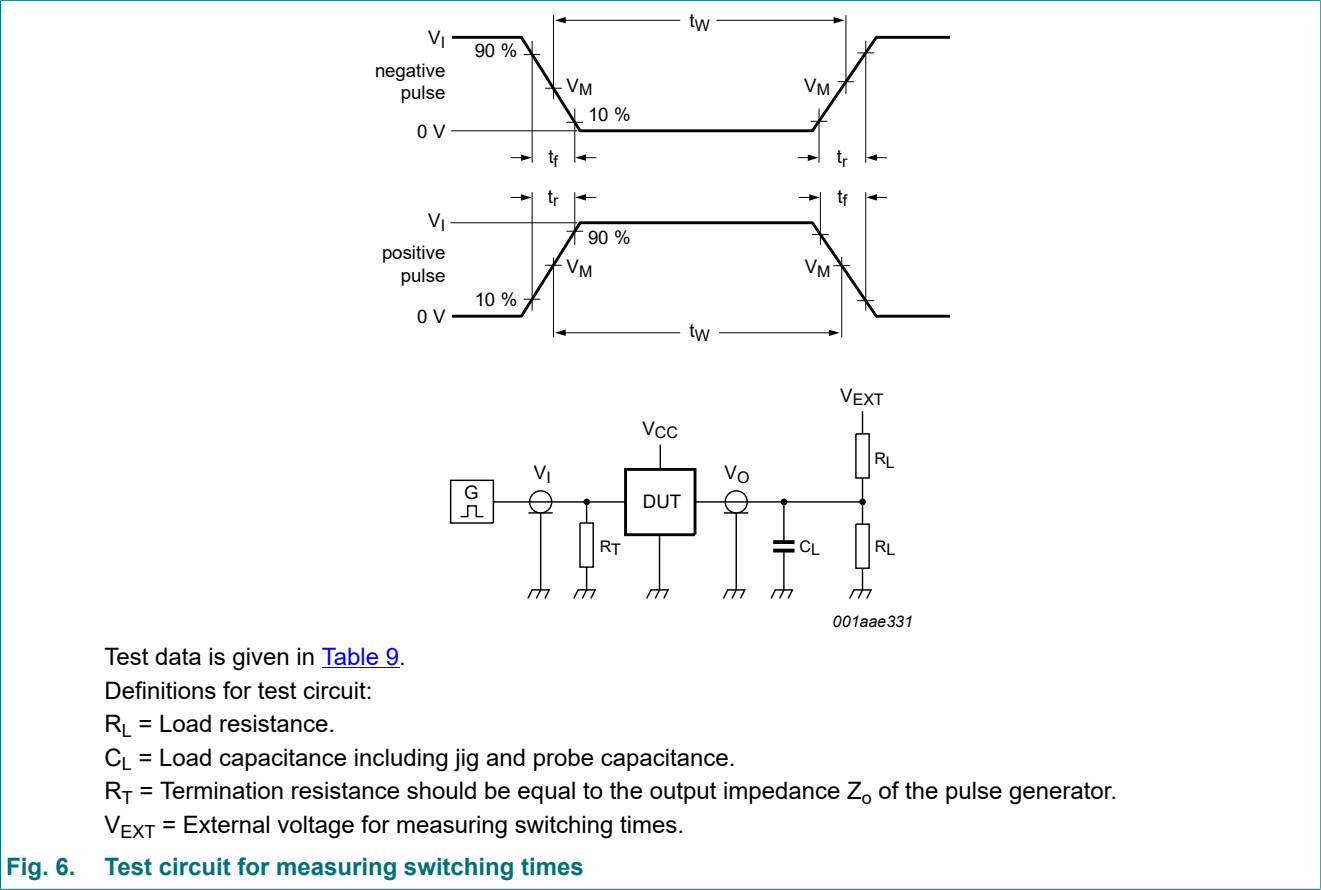


Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>		
V <sub>CC</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>
4.5 V to 5.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

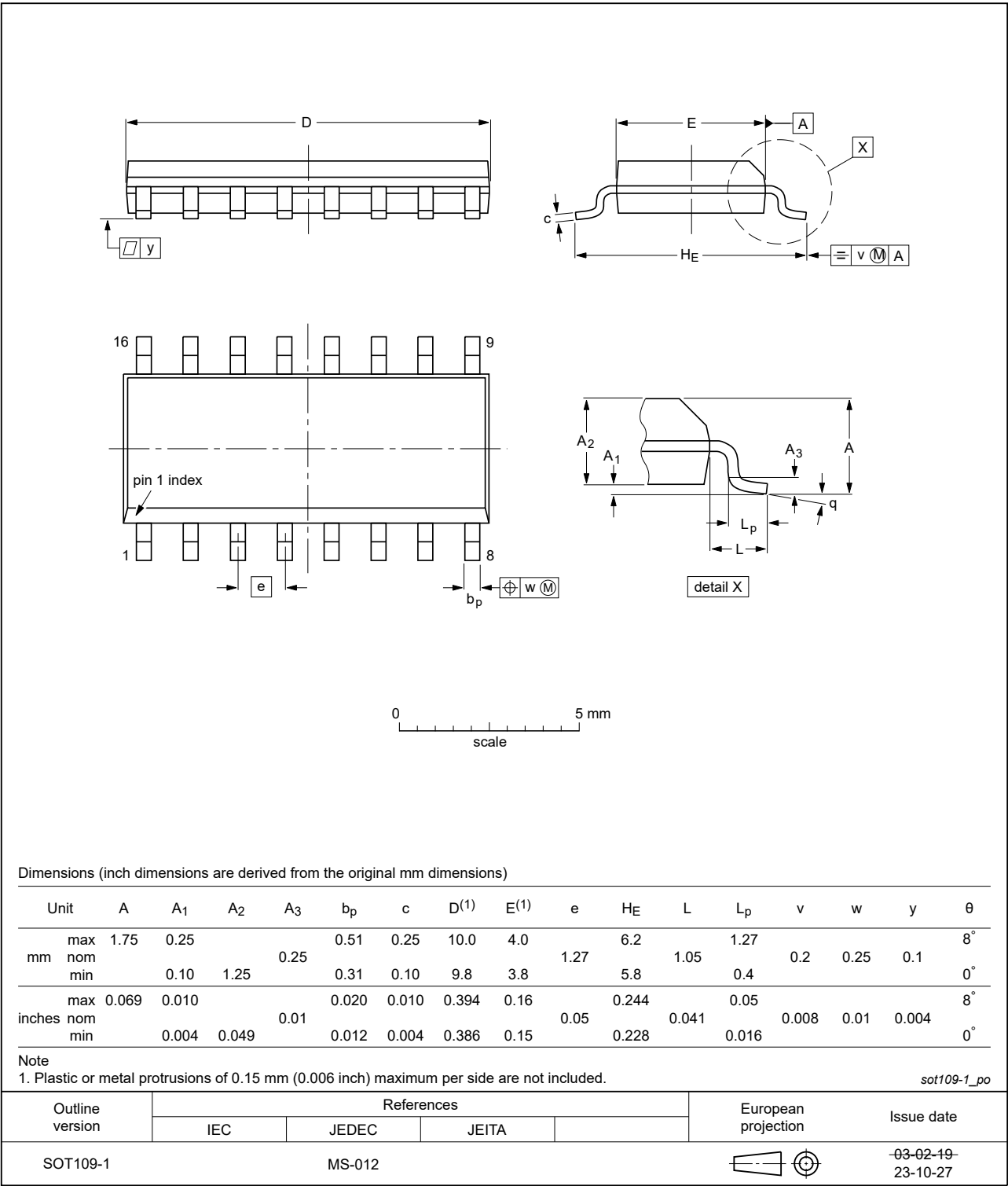


Fig. 7. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

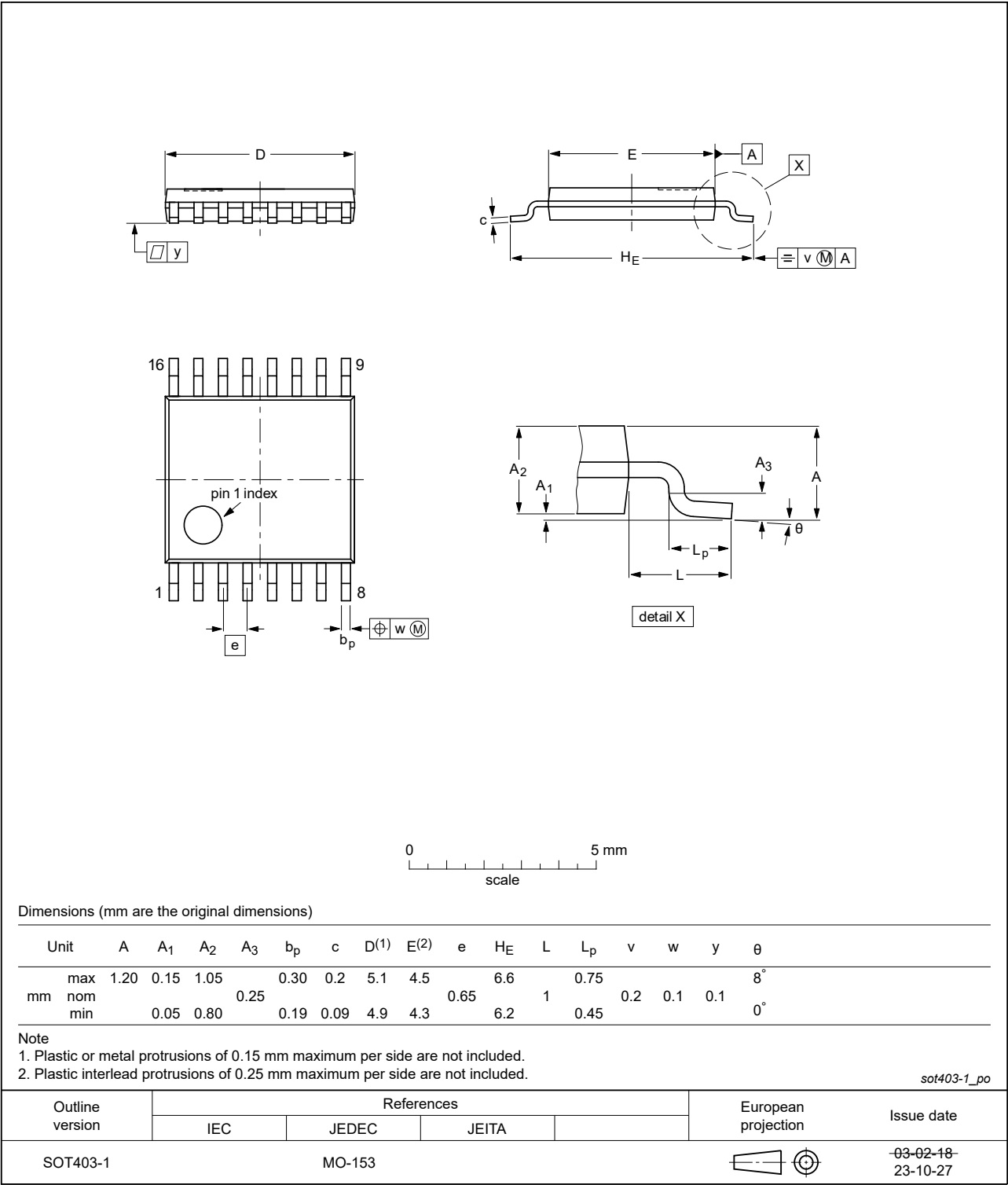


Fig. 8. Package outline SOT403-1 (TSSOP16)



12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3253 v.5	20240418	Product data sheet	-	CBT3253 v.4
Modifications:	<ul style="list-style-type: none"><li><a href="#">Fig. 7</a>, <a href="#">Fig. 8</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li><li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li></ul>			
CBT3253 v.4	20210323	Product data sheet	-	CBT3253 v.3
Modifications:	<ul style="list-style-type: none"><li><a href="#">Section 2</a> updated.</li><li>Type number CBT3253DB (SOT338-1 / SSOP16) removed.</li></ul>			
CBT3253 v.3	20181122	Product data sheet	-	CBT3253 v.2
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li>Type number CBT3253DS (SOT519-1/SSOP16) removed.</li></ul>			
CBT3253 v.2	20141203	Product data sheet	-	CBT3253 v.1
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li><a href="#">Section 1</a>: text changed to align with the function of the device.</li><li><a href="#">Fig. 1</a>: schematic changed.</li><li><a href="#">Table 3</a>: switch description changed to align with the function of the device.</li><li><a href="#">Table 6</a>:<ul style="list-style-type: none"><li>C<sub>io(off)</sub>, A port: changed typical value from 23.5 pF to 11.4 pF.</li><li>C<sub>io(off)</sub>, B port: changed typical value from 6.5 pF to 3.8 pF.</li><li>Added C<sub>io(on)</sub> specification.</li><li>Values for pass voltage modified.</li></ul></li></ul>			
CBT3253 v.1	20021104	Product data sheet	-	-

## 14. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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- [2] The term 'short data sheet' is explained in section "Definitions".
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