NCA9306-Q100

2-bit bidirectional multi-voltage level translator; open-drain; push-pull

Rev. 1 — 11 February 2022 Product data sheet

1. General description

The NCA9306-Q100 is a 2 channel bidirectional I²C and SMBus multi-voltage level translator with an enable (EN) pin input. It allows voltage translation between 0.95 V and 5 V without the use of a direction pin. It supports up to 100 MHz up translation and >100 MHz down translation at ≤ 30 pF capacitive load. There is no need for a direction pin which minimizes the system effort. The NCA9306-Q100 supports 5 V tolerant I/O pins to support mixed mode signal operation. The ability to set up different voltage translation levels on each channel makes the device very flexible and suitable for a lot of different applications.

The low ON-state resistance R_{ON} of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCLA and SDAA I/O are connected to the SCLB and SDAB I/O respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. As with the standard I²C bus-system, pull-up resistors are required to provide the logic HIGH levels on the translators bus. The NCA9306-Q100 has a standard open-drain configuration of the I²C-bus. The size of these pull-up resistors depend on the system. Each side of the translator must have a pull-up resistors. NCA9306-Q100 is designed to work with Standard-mode, Fast-mode and Fast-mode plus I²C bus devices in addition to the SMBus devices.

When the SDAA or SDAB pin is LOW, the clamp is in the ON-state and a low resistance connections exists between the SDAA and SDAB ports. Assuming the higher voltage is on the SDAB port when the SDAB port is HIGH, the voltage on the SDAA port is limited to the voltage set by refA. When the SDAA port is HIGH, the SDAB port is pulled to the refB supply voltage by the pull-up resistors. The SCLA or SCLB pins also follows the same behavior as described for SDAA or SDAB pins.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +125 °C
- 2-channel bidirectional voltage translator for SDA and SCL lines in mixed mode I²C bus applications
- Open-drain I²C-bus I/O ports (SCLA, SDAA, SCLB and SDAB)
- Provides bidirectional voltage translation with no direction pin
- High-impedance SCLA, SDAA, SCLB and SDAB for EN = LOW
- Up translation
  - < 100 MHz; C_L = 30 pF
  - < 40 MHz; C_L = 50 pF
- Down translation
  - > 100 MHz; C_L = 30 pF
  - < 40 MHz; C_L = 50 pF
- Hot insertion

- Bidirectional voltage level translation between:
  - 0.95 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
  - 1.2 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
  - 1.8 V and 2.5 V, 3.3 V and 5.0 V
  - 2.5 V and 3.3 V and 5.0 V
  - 3.3 V and 5.0 V
- Low standby current
- 5 V tolerant I²C-bus I/O pins to support mixed mode signal operation
- Low R_{ON} provides less signal distortion
- Latch-up performance exceeds 100 mA per JESD78 class II level A
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 1000 V

3. Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I²C, and other interfaces in Telecom infrastructure
- Industrial
- Personal computing
- Router and Industrial Automation

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NCA9306DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

5. Marking

Table 2. Marking

Type number	Marking code[1]
NCA9306DC-Q100	h9

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram

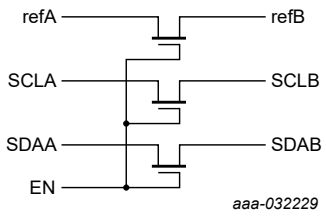


Fig. 1. Logic symbol

7. Pinning information

7.1. Pinning

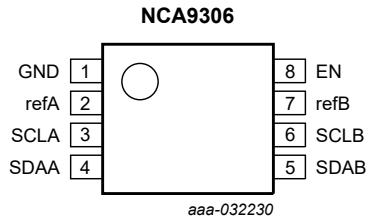


Fig. 2. Pin configuration SOT765-1 (VSSOP8)

7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1	ground (0 V)
refA	2	low-voltage side reference supply voltage for SCLA and SDAA
SCLA, SCLB	3, 6	data input/output SCL
SDAA, SDAB	4, 5	data input/output SDA
refB	7	high-voltage side reference supply voltage for SCLB and SDAB
EN	8	enable input (active HIGH)

8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	input/output
EN	**SCLn, SDAn channel**
H	SCLA = SCLB; SDAA = SDAB
L	Z

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	pins refA, refB, SCLn, SDAn and EN	[1]	-0.5	+7.0	V
$I_{I/O}$	input/output current	pins refA, refB, SCLn, SDAn; continuous channel current		-	+128	mA
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.
[2] For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	pins refA, refB, SCLn, SDAn and EN	0.0	5.0	V
$I_{I/O}$	input/output current	pins refA, refB, SCLn, SDAn; continuous channel current	-	+64	mA
T_{amb}	ambient temperature		-40	+125	°C

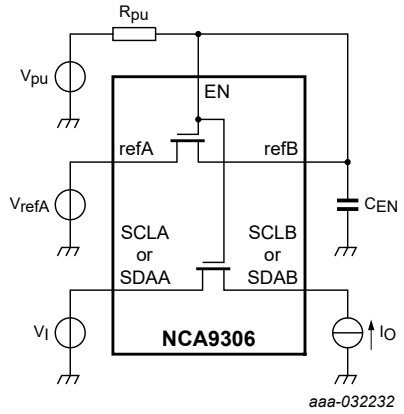
11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
V_{IK}	input clamping voltage	V_{EN} = 0 V; I_I = -18 mA	-1.2	-	-	V
I_I	leakage current	pins SCLn, SDAn, refA, refB and EN; V_I = GND to 5.0 V	-	1	5	µA
C_I	input capacitance	pins refA, refB and EN; V_I = 0 V or 3 V	-	6	-	pF
$C_{io(off)}$	OFF-state input/output capacitance	pins SCLn, SDAn; V_O = 0 V or 3 V; V_{EN} = 0.0 V	-	3.0	6.0	pF
$C_{io(on)}$	ON-state input/output capacitance	pins SCLn, SDAn; V_O = 0 V or 3 V; V_{EN} = 3.0 V	-	6.0	12.5	pF
R_{ON}	ON resistance	see Fig. 3				
		V_I = 0 V; V_{pu} = 5.0 V; I_O = 64 mA [2]				
		V_{refA} = 3.3 V	-	3	7	Ω
		V_{refA} = 1.8 V	-	4	10	Ω
		V_I = 0 V; V_{refB} = V_{EN} = 5.0 V; I_O = 32mA				
		V_{refA} = 1.8 V	-	4	9	Ω
		V_{refA} = 2.5 V	-	3	8	Ω
		V_I = 1.8 V; V_{refB} = V_{EN} = 5.0 V; I_O = 15 mA				
		V_{refA} = 3.3 V	-	4	13	Ω
		V_I = 1.0 V; V_{refB} = V_{EN} = 3.3 V; I_O = 10 mA				
		V_{refA} = 1.8 V	-	7	24	Ω
		V_I = 0 V; V_{refB} = V_{EN} = 3.3 V; I_O = 10 mA				
		V_{refA} = 1.0 V	-	5	18	Ω
		V_I = 0 V; V_{refB} = V_{EN} = 1.8 V; I_O = 10 mA				
		V_{refA} = 1.0 V	-	6	19	Ω

[1] All typical values are measured at T_{amb} = 25 °C.
[2] Measured by the voltage drop between the SCLn and SDAn pins at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (SCLn or SDAn) pins.



R_{pu} = 200 kΩ; C_{EN} = 100 nF (The SCLn and SDAn pins may be exchanged.)

Fig. 3. Test circuit for measuring R_{ON}

12. Dynamic characteristics

Table 8. Switching characteristics

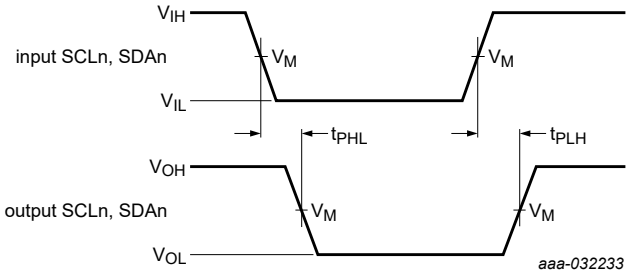
GND = 0 V; for waveform see Fig. 4; for test circuit see Fig. 5

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
Translating down						
t_{PLH}	LOW to HIGH propagation delay	SCLA, SDAA to SCLB, SDAB or SCLB, SDAB to SCLA, SDAA;				
		$V_{IH} = V_{pu} = V_{refA} + 1$ V				
		V_{refA} = 1.5 V; C_L = 15 pF	-	0.13	0.35	ns
		V_{refA} = 1.5 V; C_L = 30 pF	-	0.22	0.59	ns
		V_{refA} = 1.5 V; C_L = 50 pF	-	0.34	0.94	ns
		V_{refA} = 2.3 V; C_L = 15 pF	-	0.09	0.25	ns
		V_{refA} = 2.3 V; C_L = 30 pF	-	0.16	0.43	ns
		V_{refA} = 2.3 V; C_L = 50 pF	-	0.24	0.69	ns
t_{PHL}	HIGH to LOW propagation delay	SCLA, SDAA to SCLB, SDAB or SCLB, SDAB to SCLA, SDAA;				
		$V_{IH} = V_{pu} = V_{refA} + 1$ V				
		V_{refA} = 1.5 V; C_L = 15 pF	-	0.21	0.99	ns
		V_{refA} = 1.5 V; C_L = 30 pF	-	0.36	1.78	ns
		V_{refA} = 1.5 V; C_L = 50 pF	-	0.51	2.42	ns
		V_{refA} = 2.3 V; C_L = 15 pF	-	0.12	0.45	ns
		V_{refA} = 2.3 V; C_L = 30 pF	-	0.19	0.77	ns
		V_{refA} = 2.3 V; C_L = 50 pF	-	0.30	1.17	ns

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
Translating up						
t_{PLH}	LOW to HIGH propagation delay	SCLA, SDAA to SCLB, SDAB or SCLB, SDAB to SCLA, SDAA;				
		$V_{IH} = V_{refA}$; $V_{EXT} = V_{pu} = V_{refA} + 1$ V				
		V_{refA} = 1.5 V; C_L = 15 pF	-	0.06	0.11	ns
		V_{refA} = 1.5 V; C_L = 30 pF	-	0.14	0.32	ns
		V_{refA} = 1.5 V; C_L = 50 pF	-	0.26	0.58	ns
		V_{refA} = 2.3 V; C_L = 15 pF	-	0.06	0.13	ns
		V_{refA} = 2.3 V; C_L = 30 pF	-	0.13	0.28	ns
		V_{refA} = 2.3 V; C_L = 50 pF	-	0.20	0.50	ns
t_{PHL}	HIGH to LOW propagation delay	SCLA, SDAA to SCLB, SDAB or SCLB, SDAB to SCLA, SDAA;				
		$V_{IH} = V_{refA}$; $V_{EXT} = V_{pu} = V_{refA} + 1$ V				
		V_{refA} = 1.5 V; C_L = 15 pF	-	0.34	1.54	ns
		V_{refA} = 1.5 V; C_L = 30 pF	-	0.60	2.60	ns
		V_{refA} = 1.5 V; C_L = 50 pF	-	0.90	3.82	ns
		V_{refA} = 2.3 V; C_L = 15 pF	-	0.17	0.71	ns
		V_{refA} = 2.3 V; C_L = 30 pF	-	0.29	1.09	ns
		V_{refA} = 2.3 V; C_L = 50 pF	-	0.45	1.67	ns

[1] All typical values are measured at T_{amb} = 25 °C.

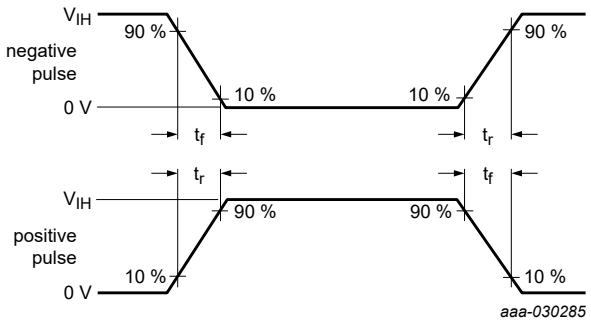
12.1. Waveforms and test circuit



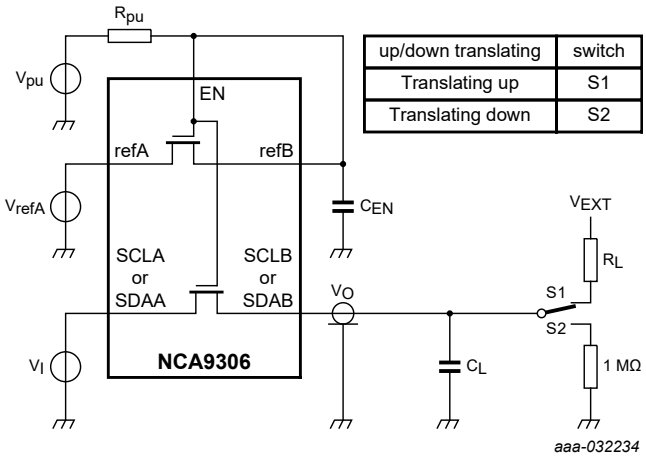
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The data input (SCLn, SDAn) to output (SCLn, SDAn) propagation delay times



a. V_I source waveform



up/down translating	switch
Translating up	S1
Translating down	S2

b. Test circuit

Test data is given in Table 9.
The SCLn and SDAn pins may be exchanged.
All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_O = 50 Ω.
Definitions test circuit:
C_L = Load capacitance including jig and probe capacitance; C_{EN} = Decoupling capacitance;
R_{pu} = Pull-up resistance; R_L = Load resistance; S1/S2 = Test selection switch

Fig. 5. Test circuit for measuring switching times

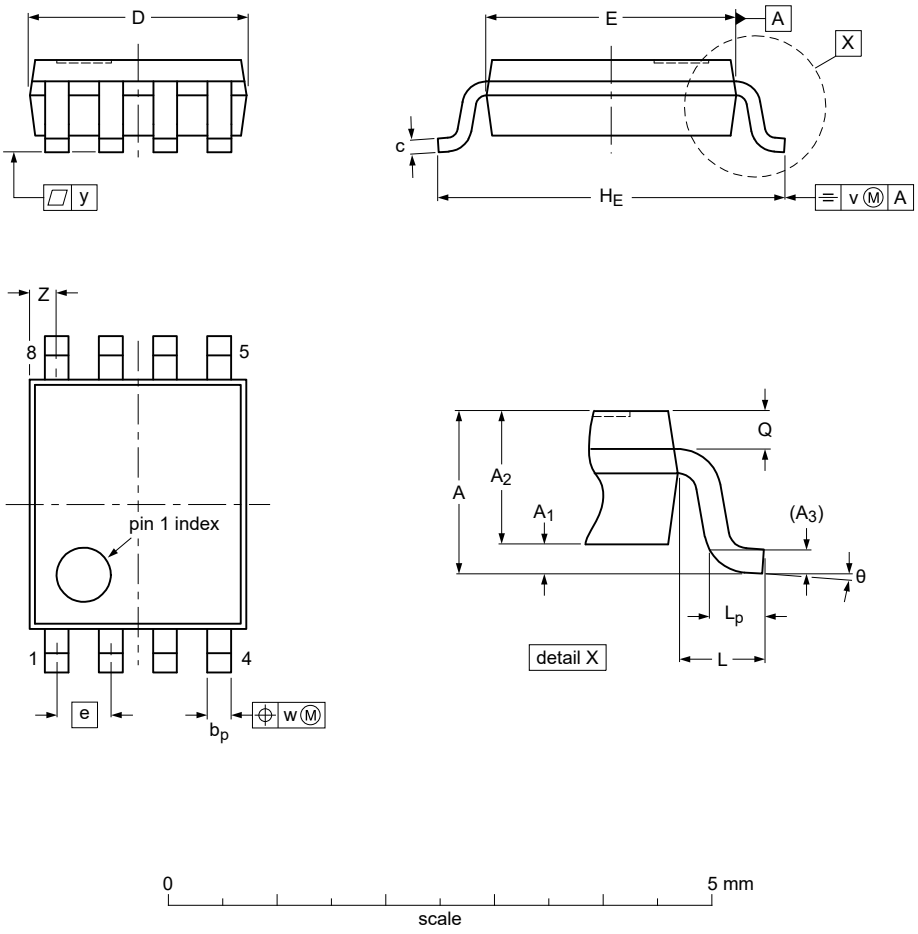
Table 9. Test data

Input		Output	Load			
t_r, t_f	V_M	V_M	C_L	C_{EN} [1]	R_L [1]	R_{pu}
≤ 2 ns	$0.5V_{refA}$	$0.5V_{refA}$	15 pF, 30 pF, 50 pF	100 nF	300 Ω	200 kΩ

[1] All typical values are measured at T_{amb} = 25 °C.

13. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
mm nom	1			0.12					0.5		0.4			0.2	0.08	0.1		
min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig. 6. Package outline SOT765-1 (VSSOP8)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I²C	Inter-Integrated Circuit
PMBus	Power Management Bus
PRR	Pulse Rate Repetition
SMBus	System Management Bus

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NCA9306_Q100 v.1	20220211	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 11 February 2022

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