



# PSMN2R0-55YLH

N-channel 50 V, 2.1 mOhm, 200 A continuous, logic level  
Application Specific MOSFET in LFPK56E

26 January 2022

Product data sheet

## 1. General description

200 Amp continuous current, logic level gate drive, N-channel enhancement mode MOSFET in LFPK56E package. Part of the ASFETs for Battery Isolation and DC Motor control family and using Nexperia's unique "SchottkyPlus" technology delivers high efficiency and low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. The ASFET is particularly suited to 36 V battery powered applications requiring strong avalanche capability, linear mode performance, use at high switching frequencies, and also safe and reliable switching at high load-current.

## 2. Features and benefits

- 200 A continuous current capability
- Optimised for 36 V (nominal) battery powered applications
- LFPK56E low-stress exposed lead-frame for ultimate reliability, optimum soldering and easy solder-joint inspection
- Copper-clip and solder die attach for low package inductance and resistance, and high  $I_{D(max)}$  rating
- Qualified to 175 °C
- Avalanche rated, 100% tested
- Low  $Q_G$ ,  $Q_{GD}$  and  $Q_{OSS}$  for high efficiency, especially at higher switching frequencies
- Superfast switching with soft body-diode recovery for low-spiking and ringing, recommended for low EMI designs
- Unique "SchottkyPlus" technology for Schottky-like switching performance and low  $I_{DSS}$  leakage
- Narrow  $V_{GS(th)}$  rating for easy paralleling and improved current sharing
- Very strong linear-mode / safe operating area characteristics for safe and reliable switching at high-current conditions

## 3. Applications

- Brushless DC motor control
- Synchronous rectifier in high-power AC-to-DC applications, e.g. server power supplies
- Battery protection and Battery Management Systems (BMS)
- Load switch
- 10 cell lithium-ion battery applications (36 V – 42 V)

## 4. Quick reference data

Table 1. Quick reference data

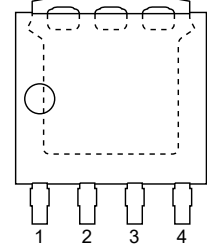
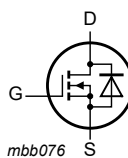
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	55	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	200	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	333	W
$T_j$	junction temperature		-55	-	175	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>	-	1.63	2.1	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>	-	1.83	2.4	mΩ
<b>Dynamic characteristics</b>						
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 27 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	14	31	nC
Q <sub>G(tot)</sub>	total gate charge		-	54	84	nC

[1] 200A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56E; Power-SO8 (SOT1023)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R0-55YLH	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56); 4 leads; 1.27 mm pitch	SOT1023

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R0-55YLH	2H055L

## 8. Limiting values

Table 5. Limiting values

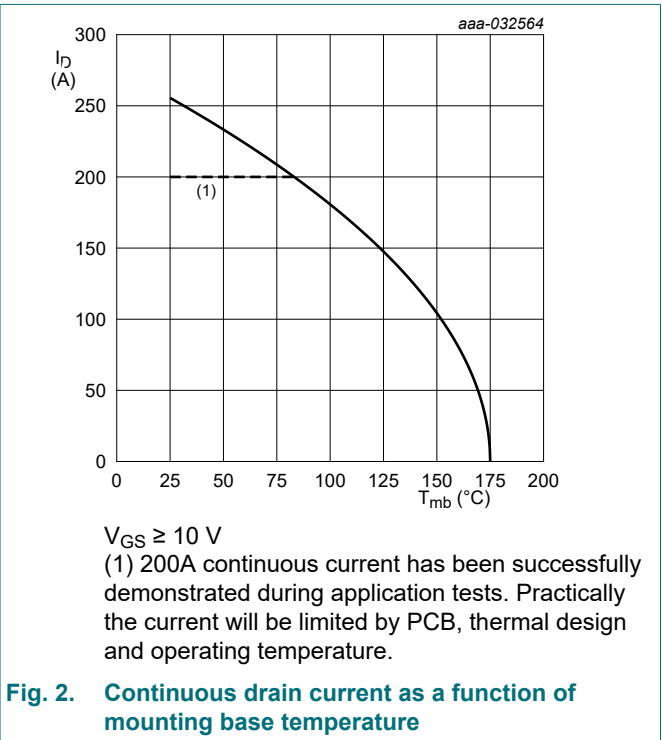
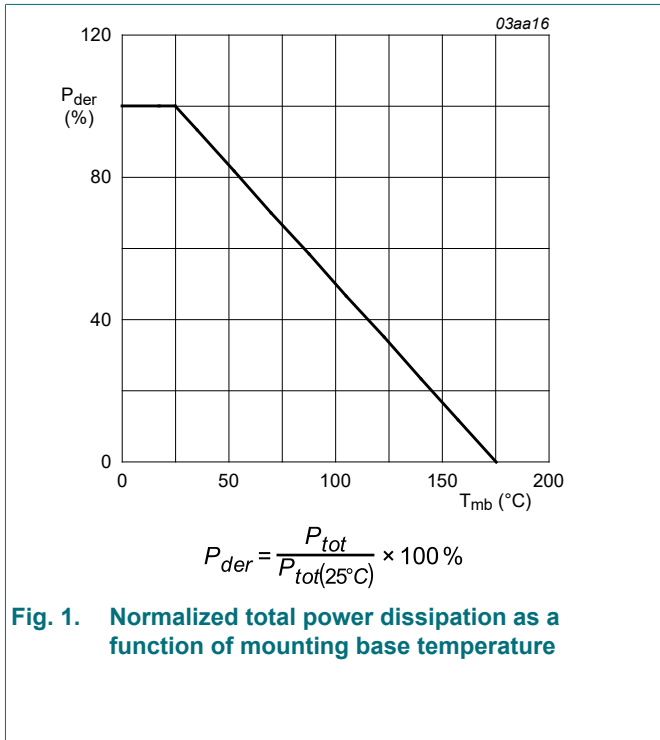
In accordance with the Absolute Maximum Rating System (IEC 60134).

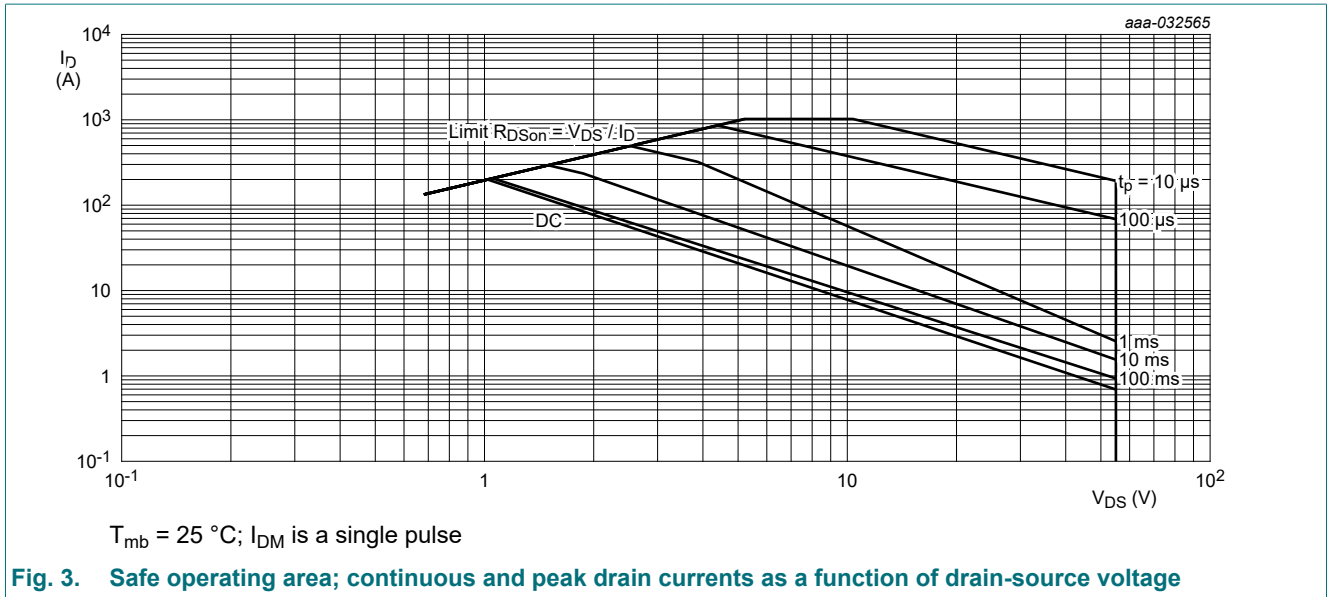
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	55	V
V <sub>DGR</sub>	drain-gate voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ	-	55	V

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Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>GS</sub>	gate-source voltage			-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	333	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	[1]	-	200	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <a href="#">Fig. 2</a>		-	181	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 3</a>		-	1049	A
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature			-	260	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	200	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	1049	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 50 A; V <sub>sup</sub> ≤ 55 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 417 μs	[2]	-	745	mJ
		I <sub>D</sub> = 25 A; V <sub>sup</sub> ≤ 55 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 1.98 s	[2]	-	1.77	J
I <sub>AS</sub>	non-repetitive avalanche current	V <sub>sup</sub> ≤ 55 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 Ω	[2]	-	115	A

- [1] 200A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test

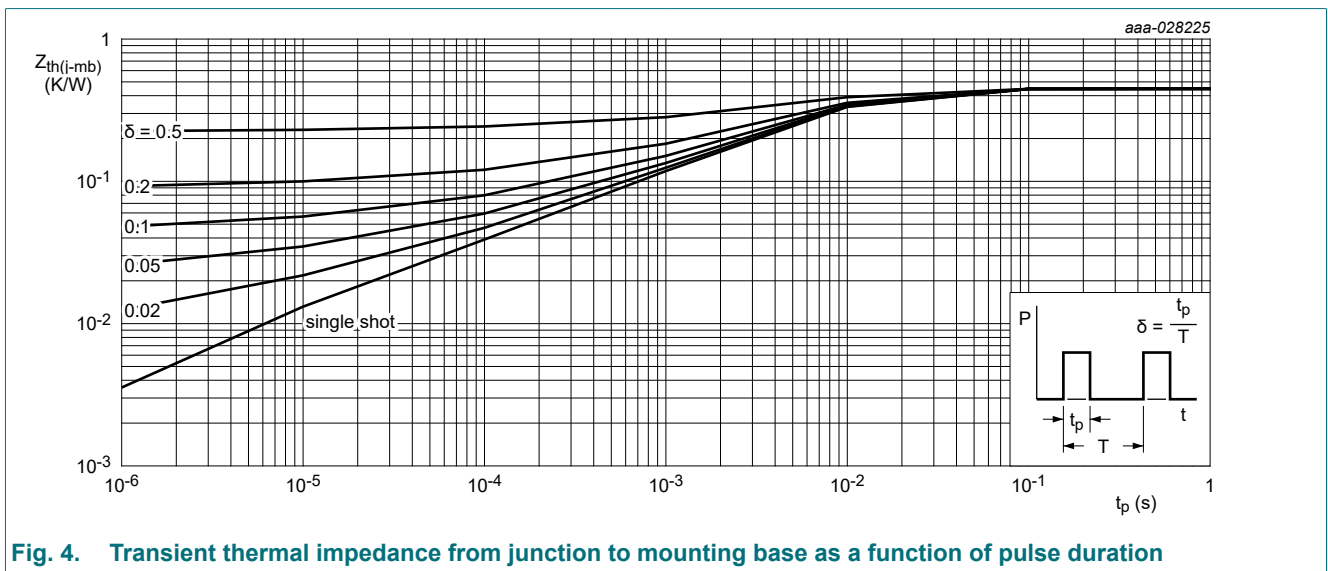


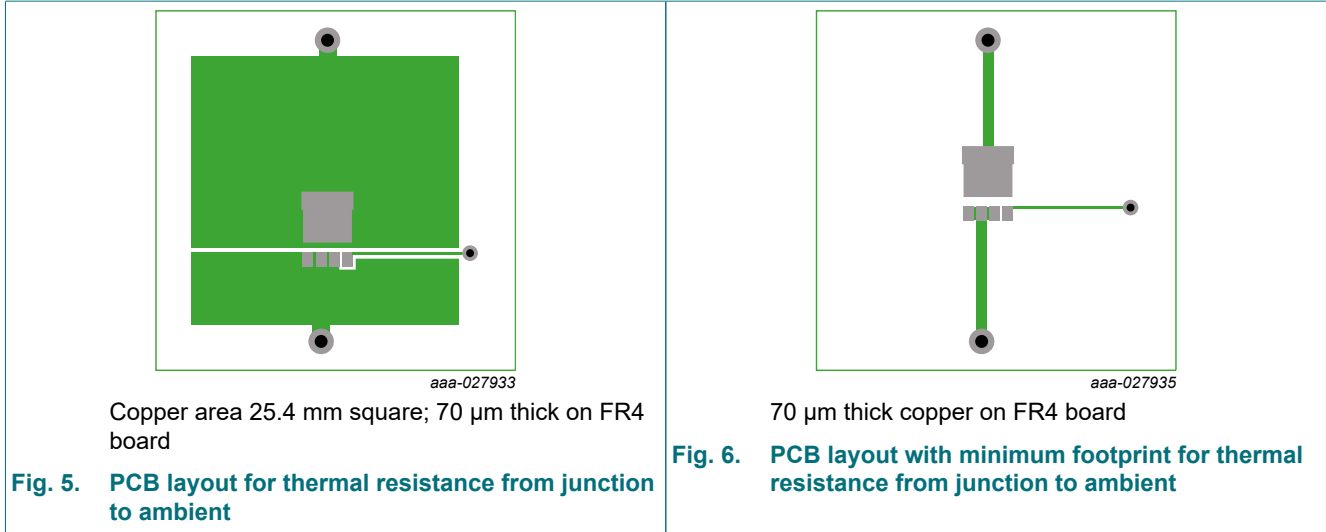


## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.33	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	42	-	K/W
		Fig. 6	-	85	-	K/W





## 10. Characteristics

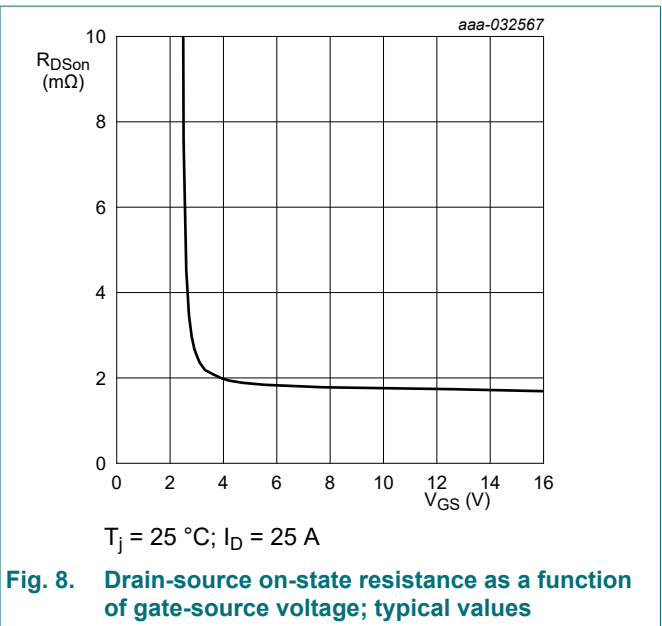
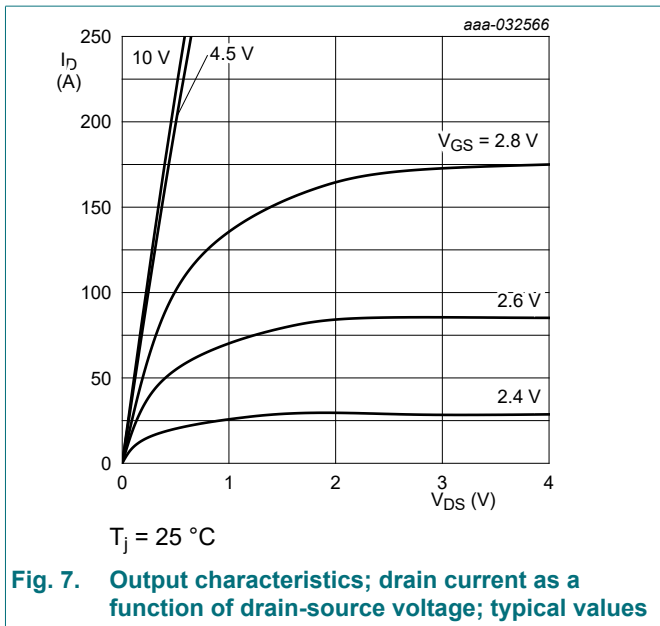
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	55	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	49.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.62	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-4.6	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 44 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	$\mu A$
		$V_{DS} = 44 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	3.5	-	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	1.63	2.1	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	-	4.3	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	1.83	2.4	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	-	4.9	m $\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.52	1.3	3.3	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 27 \text{ V}; V_{GS} = 4.5 \text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	54	84	nC
		$I_D = 25 \text{ A}; V_{DS} = 27 \text{ V}; V_{GS} = 10 \text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	119	184	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	64	-	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$Q_{GS}$	gate-source charge	$I_D = 25\text{ A}; V_{DS} = 27\text{ V}; V_{GS} = 4.5\text{ V};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	17	26	nC	
$Q_{GS(th)}$	pre-threshold gate-source charge		-	12	18	nC	
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	5.8	8.8	nC	
$Q_{GD}$	gate-drain charge		-	14	31	nC	
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}; V_{DS} = 27\text{ V};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	2.5	-	V	
$C_{iss}$	input capacitance	$V_{DS} = 27\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 14</a>	-	8109	11353	pF	
$C_{oss}$	output capacitance		-	704	986	pF	
$C_{rss}$	reverse transfer capacitance		-	226	542	pF	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 27\text{ V}; R_L = 1.1\text{ }\Omega; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega$	-	39	-	ns	
$t_r$	rise time		-	38	-	ns	
$t_{d(off)}$	turn-off delay time		-	60	-	ns	
$t_f$	fall time		-	28	-	ns	
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 27\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C}$	-	41	-	nC	
<b>Source-drain diode</b>							
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	0.75	1	V	
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 27\text{ V};$ <a href="#">Fig. 16</a>	-	36	-	ns	
$Q_r$	recovered charge		[1]	-	36	-	nC
$t_a$	reverse recovery rise time		-	-	21	-	ns
$t_b$	reverse recovery fall time		-	-	14	-	ns

[1] includes capacitive recovery



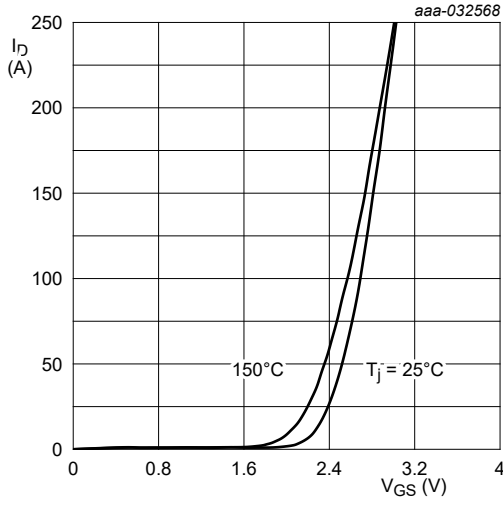


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

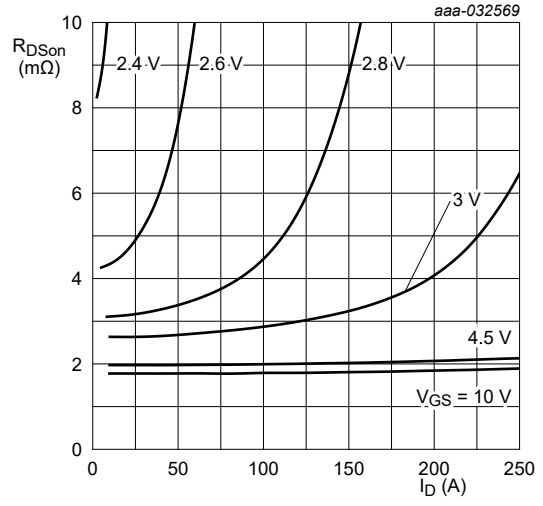
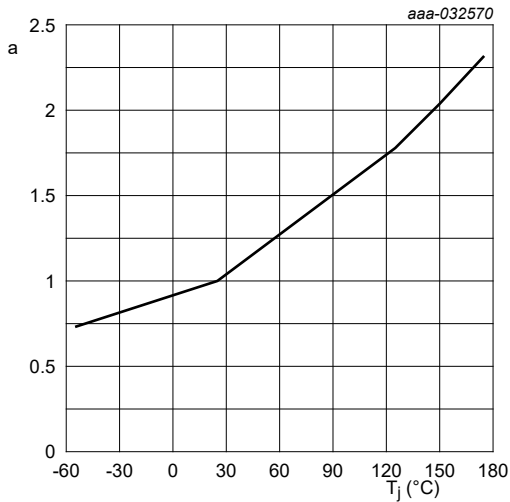


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

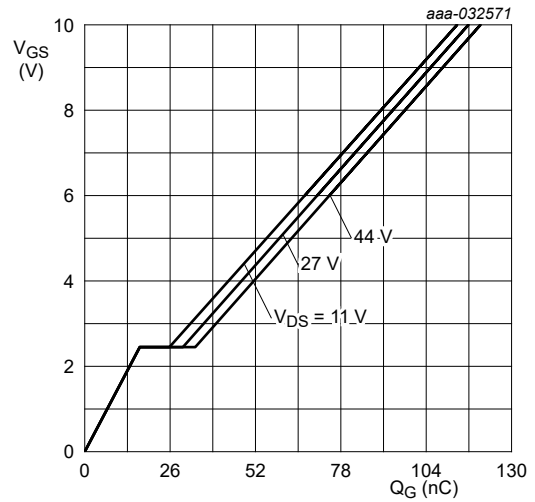


Fig. 12. Gate-source voltage as a function of gate charge; typical values

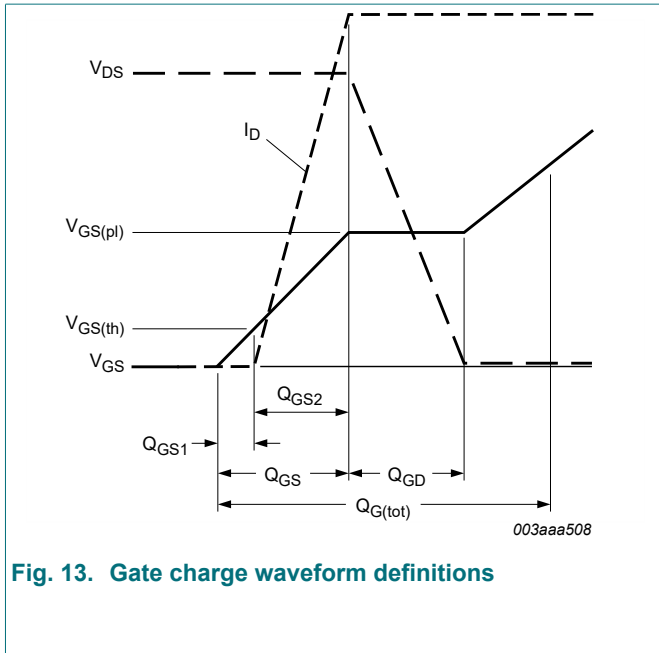


Fig. 13. Gate charge waveform definitions

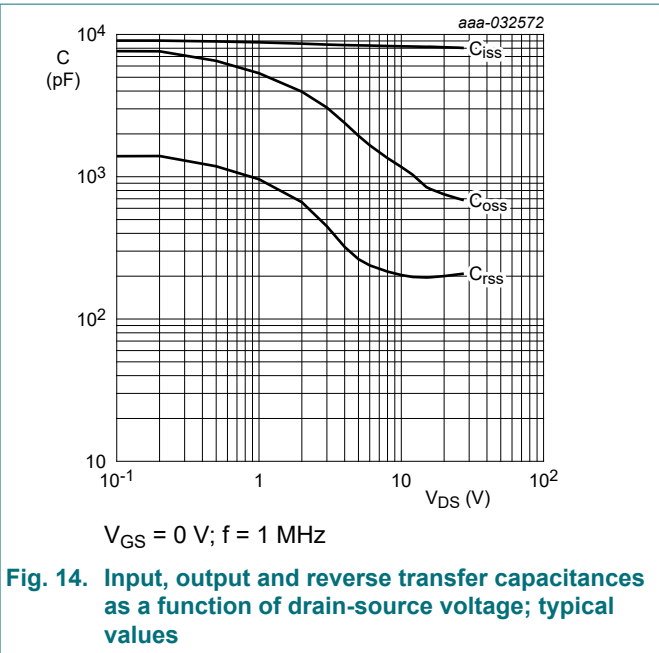


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

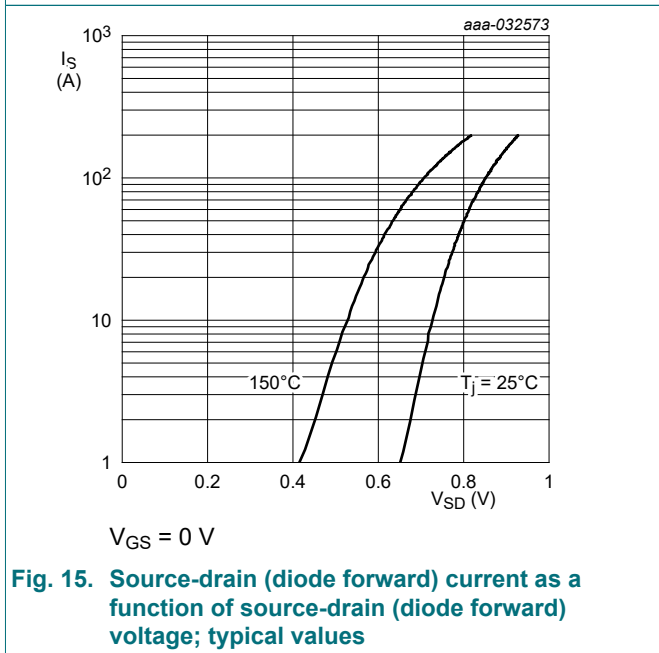


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

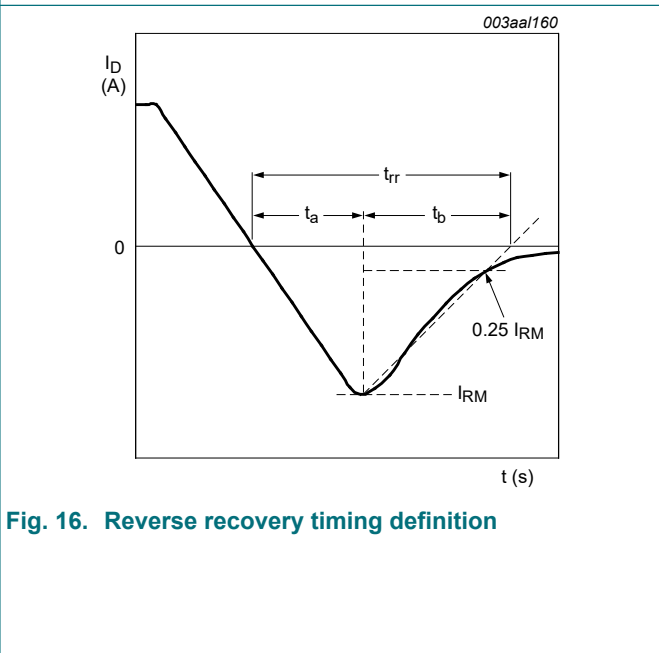


Fig. 16. Reverse recovery timing definition



### 11. Package outline

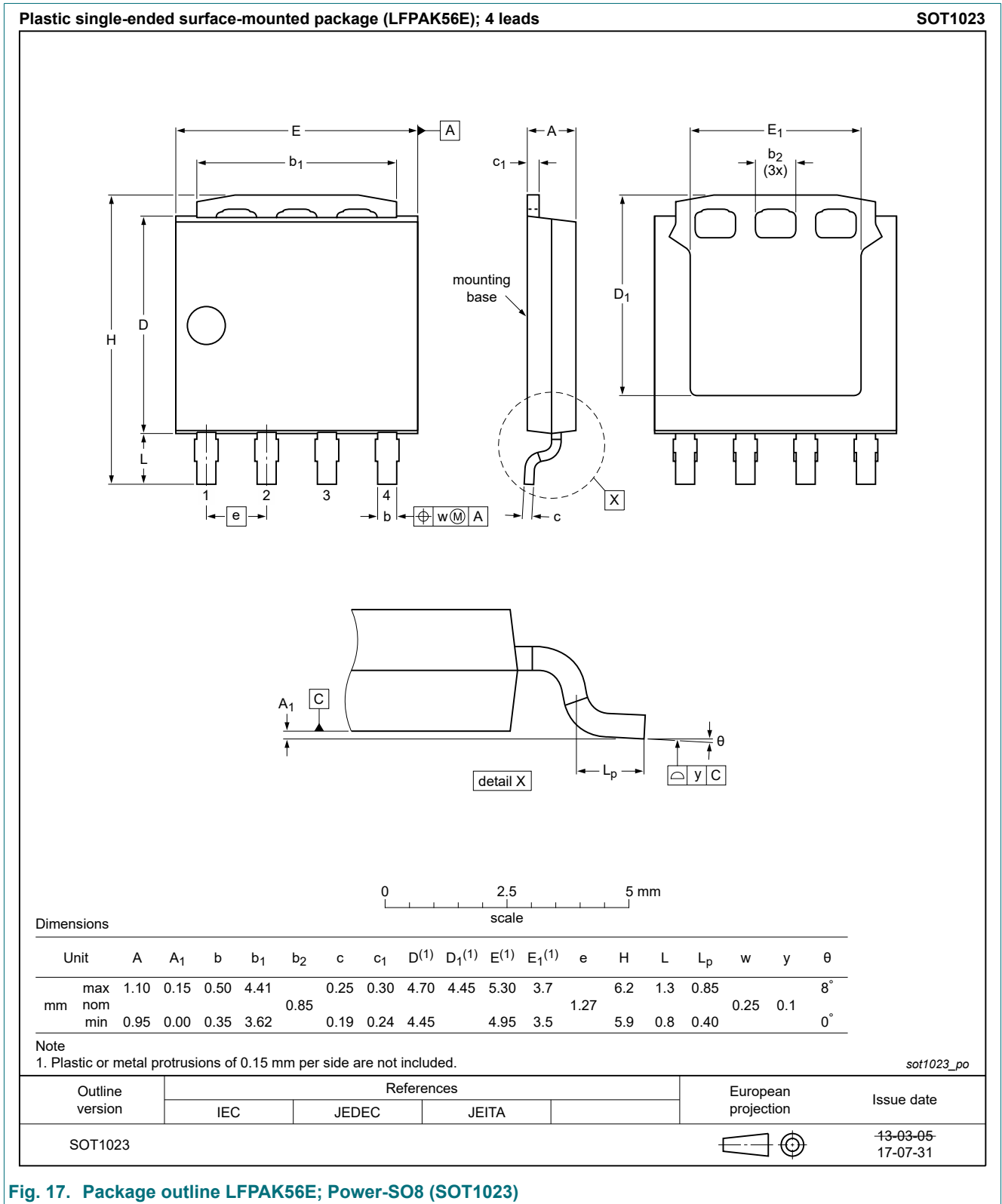


Fig. 17. Package outline LPAK56E; Power-SO8 (SOT1023)

## 12. Soldering

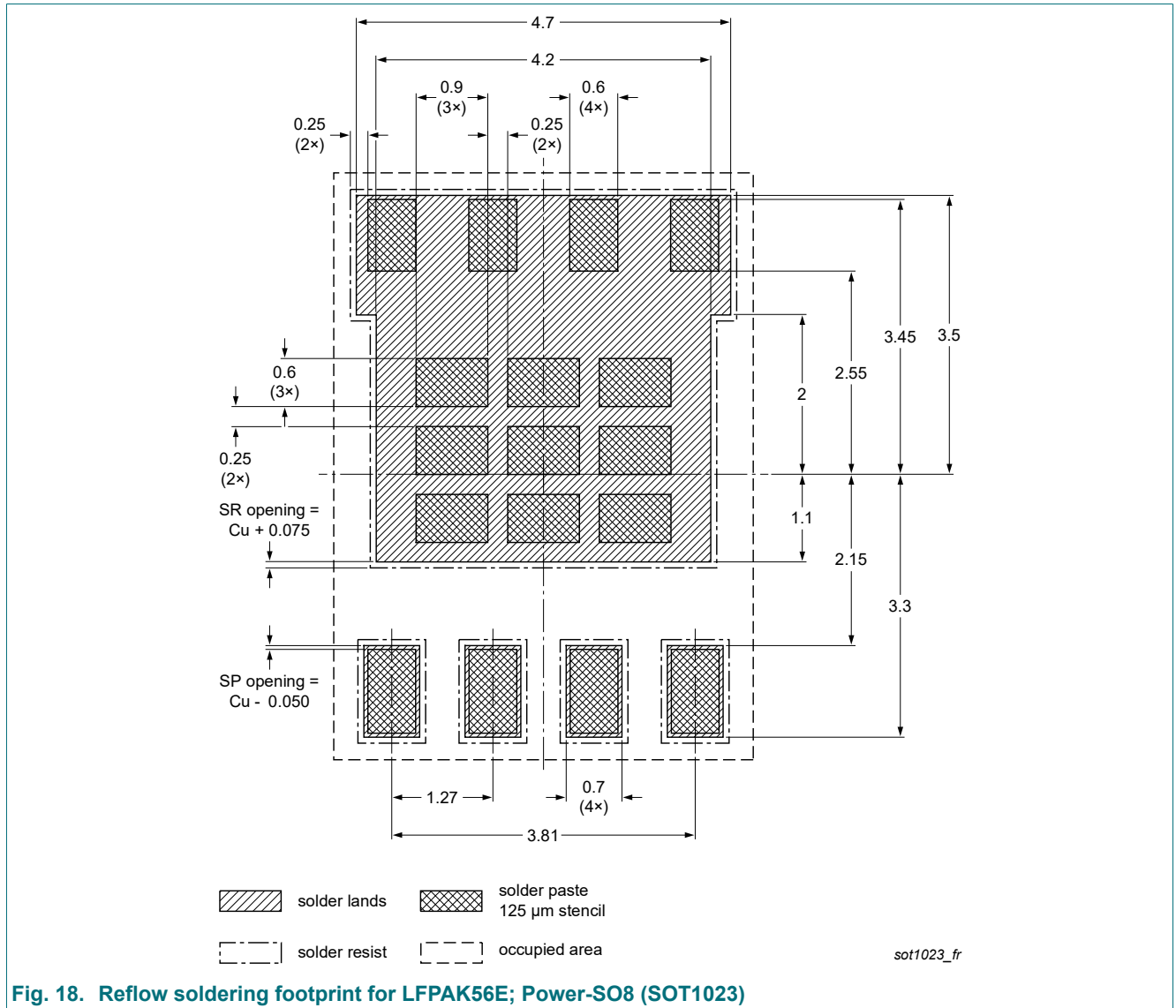


Fig. 18. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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