



PSMN3R5-30YL

N-channel 30 V 3.5 mΩ logic level MOSFET in LPAK

3 August 2018

Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in industrial and communications applications.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

3. Applications

- Class-D amplifiers
- DC-to-DC converters
- Motor control
- Server power supplies

4. Quick reference data

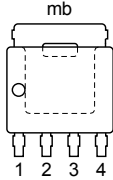
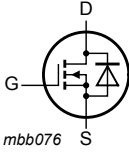
Table 1. Quick reference data

Table 1. Quiescent characteristics data							
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	30	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	74	W
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C		-	2.43	3.5	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 10 A; V _{DS} = 12 V; V _{GS} = 4.5 V; Fig. 14 ; Fig. 15		-	5	-	nC
Q _{G(tot)}	total gate charge			-	19	-	nC
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 100 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped		-	-	54	mJ

[1] Continuous current is limited by package.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R5-30YL	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN3R5-30YL	3R530

8. Limiting values

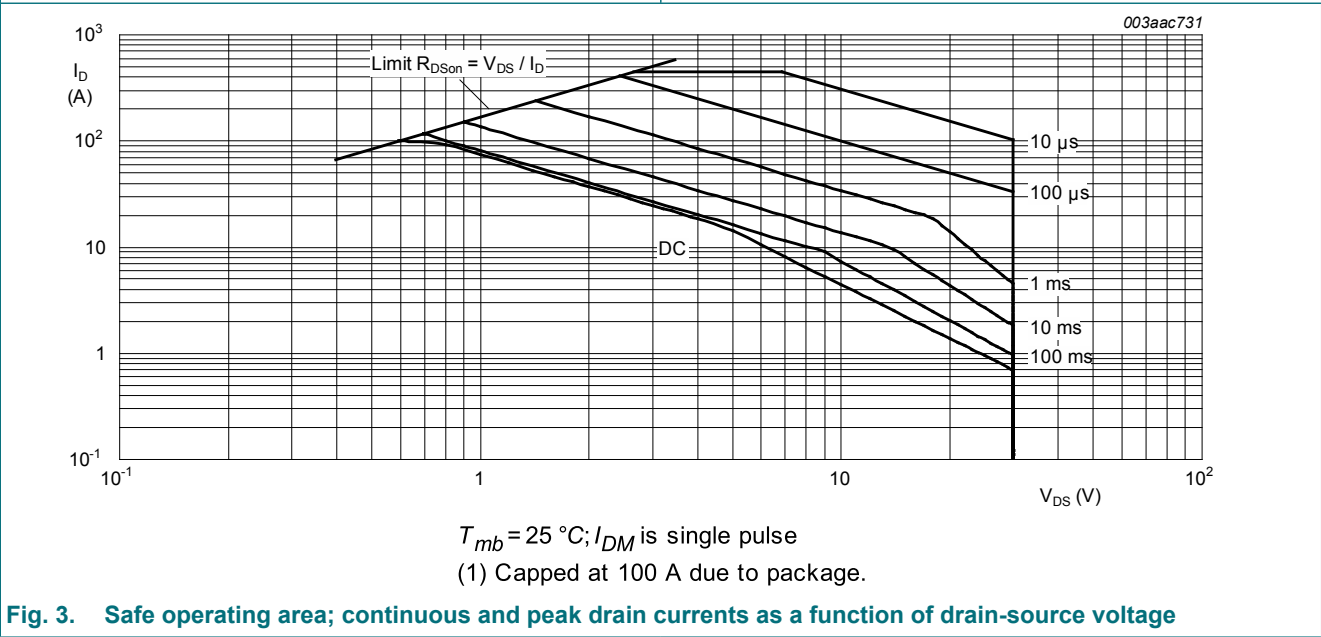
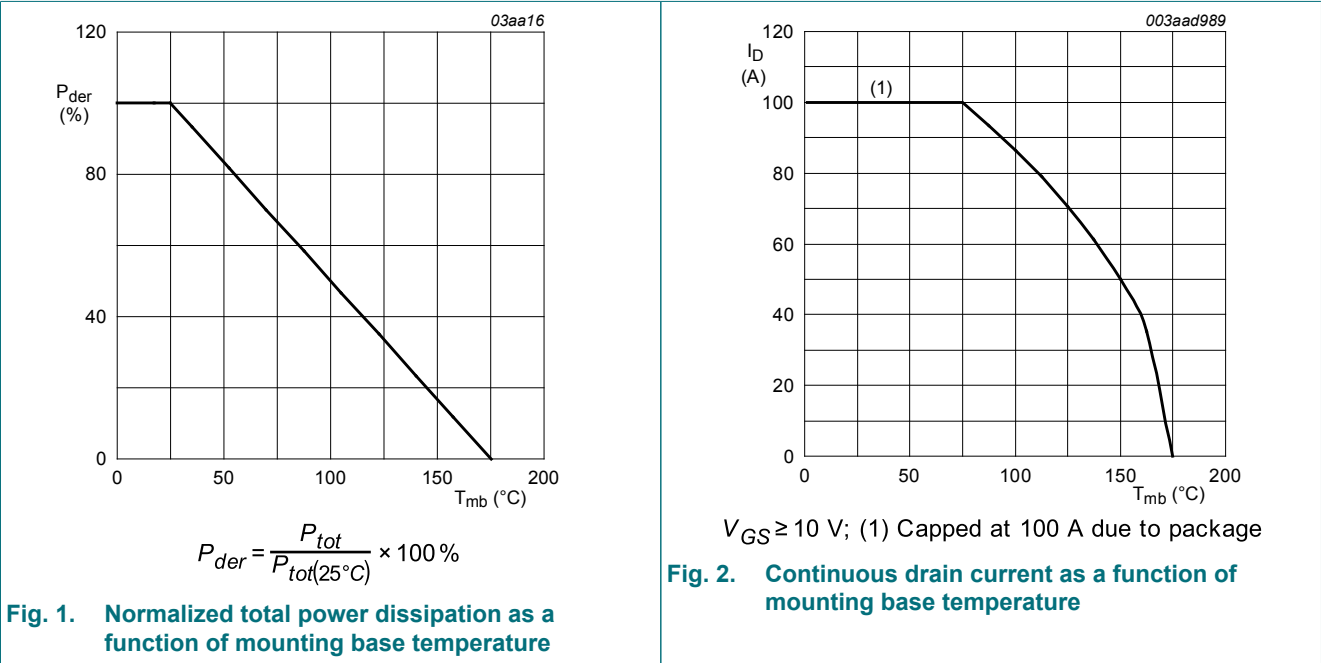
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	30	V
V_{DSM}	peak drain-source voltage	$t_p \leq 25\text{ ns}$; $f \leq 500\text{ kHz}$; $E_{DS(AL)} \leq 180\text{ nJ}$; pulsed		-	35	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$		-	30	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	74	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	[1]	-	86	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	100	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	447	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	447	A
Avalanche ruggedness						

Symbol	Parameter	Conditions		Min	Max	Unit
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped		-	54	mJ

[1] Continuous current is limited by package.



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	0.6	1.68	K/W

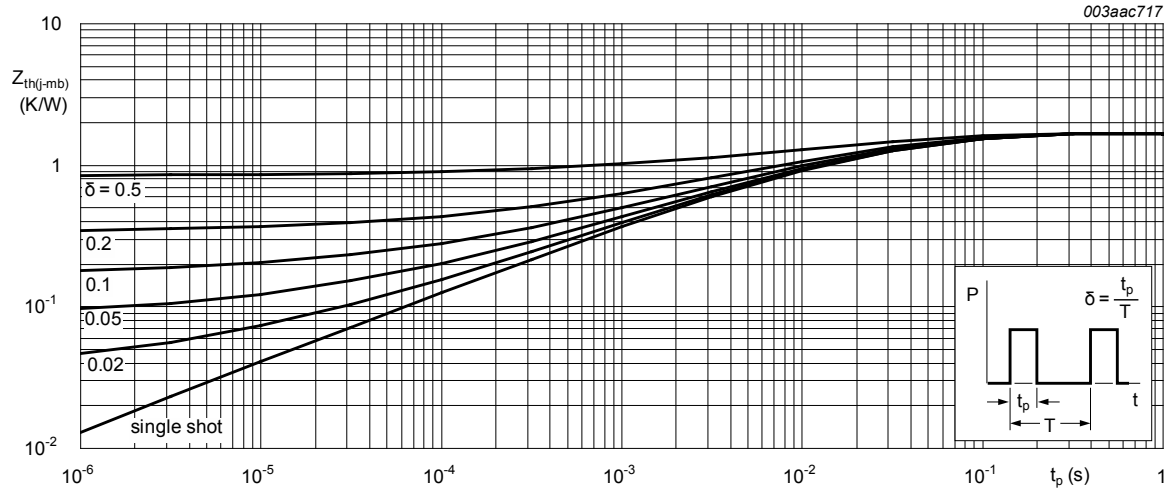


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

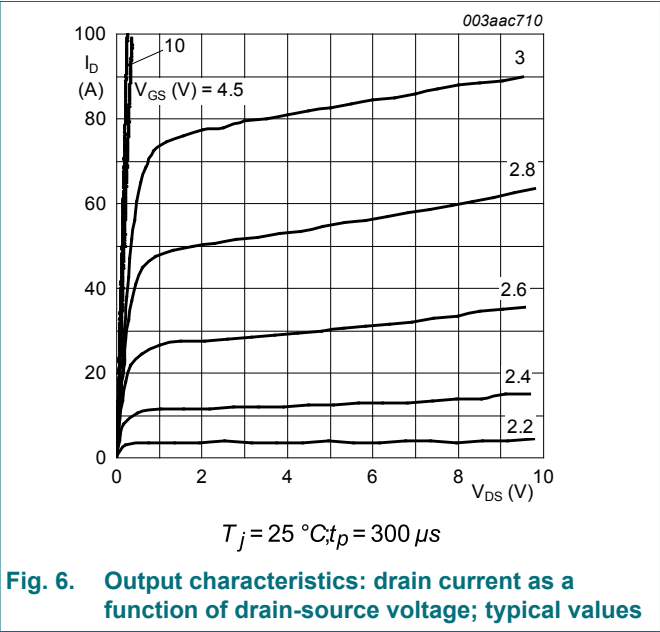
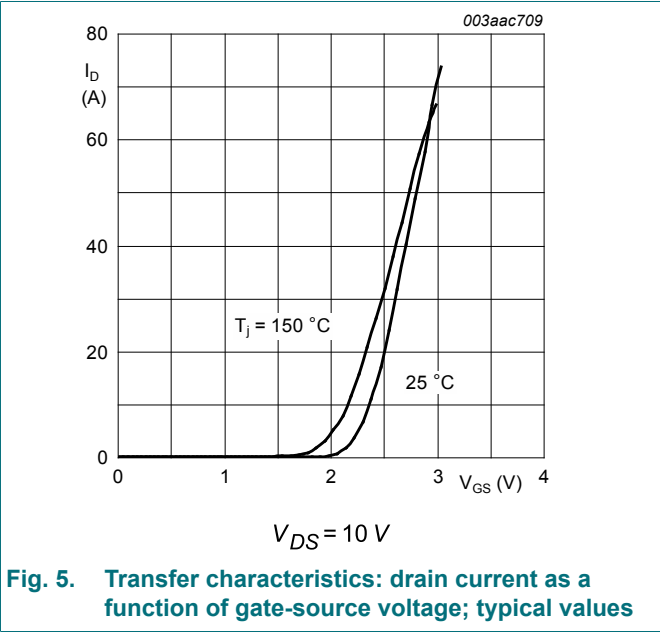
10. Characteristics

Table 7. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_J = 25 ^\circ C$	30	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_J = -55 ^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_J = 25 ^\circ C$; Fig. 11 ; Fig. 12	1.3	1.7	2.15	V
		$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_J = 150 ^\circ C$; Fig. 12	0.65	-	-	V
		$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_J = -55 ^\circ C$; Fig. 12	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V$; $V_{GS} = 0 V$; $T_J = 25 ^\circ C$	-	-	1	μA
		$V_{DS} = 30 V$; $V_{GS} = 0 V$; $T_J = 150 ^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V$; $V_{DS} = 0 V$; $T_J = 25 ^\circ C$	-	-	100	nA
		$V_{GS} = -16 V$; $V_{DS} = 0 V$; $T_J = 25 ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V$; $I_D = 15 A$; $T_J = 25 ^\circ C$	-	3.37	4.61	mΩ
		$V_{GS} = 10 V$; $I_D = 15 A$; $T_J = 150 ^\circ C$; Fig. 13	-	-	6	mΩ
		$V_{GS} = 10 V$; $I_D = 15 A$; $T_J = 25 ^\circ C$	-	2.43	3.5	mΩ
R_G	gate resistance	$f = 1 MHz$	-	0.53	1.5	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10 A$; $V_{DS} = 12 V$; $V_{GS} = 4.5 V$; Fig. 14 ; Fig. 15	-	19	-	nC
		$I_D = 0 A$; $V_{DS} = 0 V$; $V_{GS} = 10 V$	-	37	-	nC
		$I_D = 10 A$; $V_{DS} = 12 V$; $V_{GS} = 10 V$; Fig. 14 ; Fig. 15	-	41	-	nC
Q_{GS}	gate-source charge	$I_D = 10 A$; $V_{DS} = 12 V$; $V_{GS} = 4.5 V$; Fig. 14 ; Fig. 15	-	6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	4	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q _{GS(th-pl)}	post-threshold gate-source charge			-	2	-	nC
Q _{GD}	gate-drain charge			-	5	-	nC
V _{GS(pl)}	gate-source plateau voltage	V _{DS} = 12 V; Fig. 14 ; Fig. 15		-	2.4	-	V
C _{iss}	input capacitance	V _{DS} = 12 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 16		-	2458	3441	pF
C _{oss}	output capacitance			-	532	718	pF
C _{rss}	reverse transfer capacitance			-	252	353	pF
t _{d(on)}	turn-on delay time	V _{DS} = 12 V; R _L = 0.5 Ω; V _{GS} = 4.5 V; R _{G(ext)} = 4.7 Ω		-	33	-	ns
t _r	rise time			-	50	-	ns
t _{d(off)}	turn-off delay time			-	45	-	ns
t _f	fall time			-	18	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 17		-	0.82	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V		-	37	-	ns
Q _r	recovered charge			-	31	-	nC



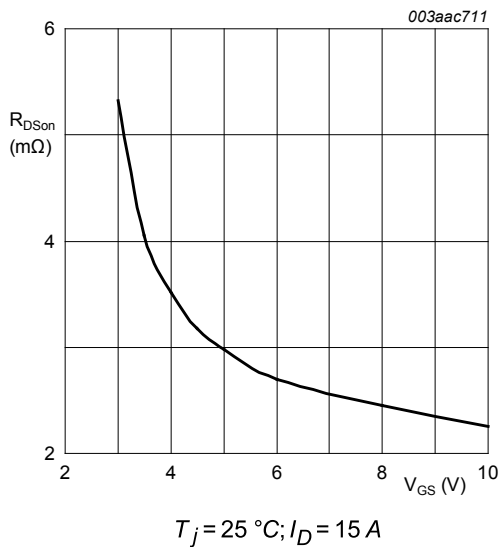


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

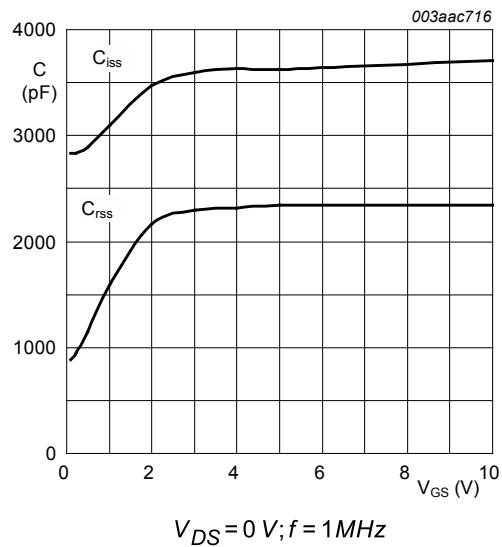


Fig. 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

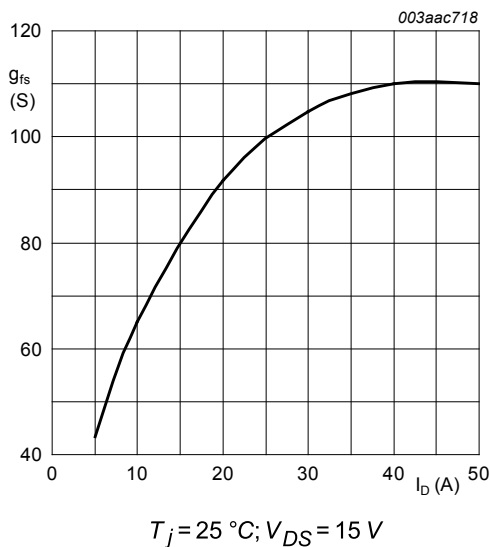


Fig. 9. Forward transconductance as a function of drain current; typical values

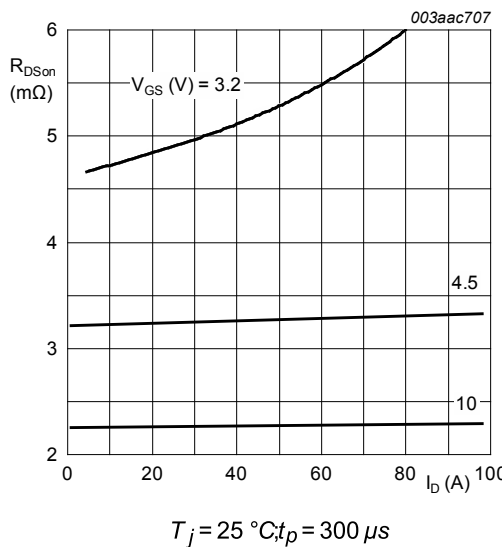


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

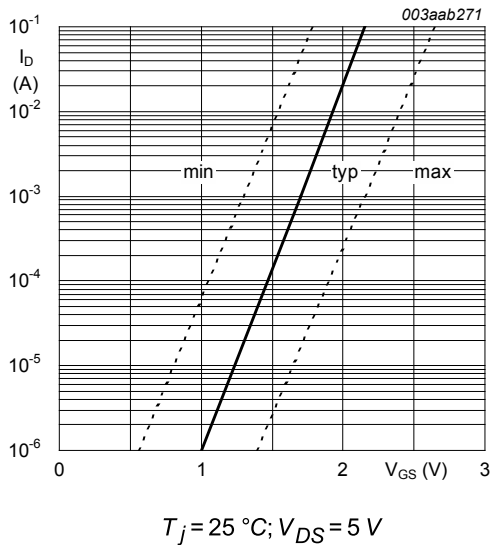


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

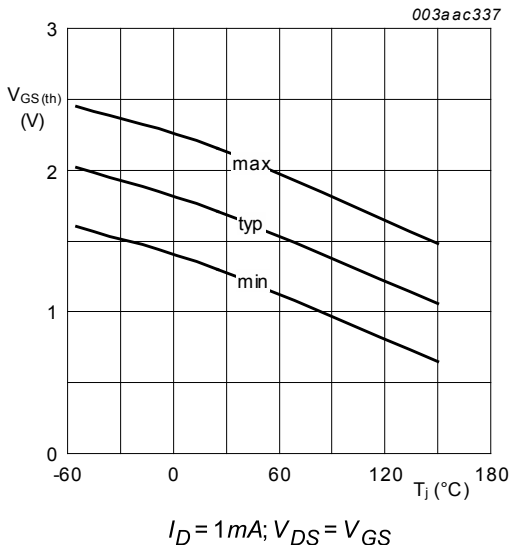


Fig. 12. Gate-source threshold voltage as a function of junction temperature

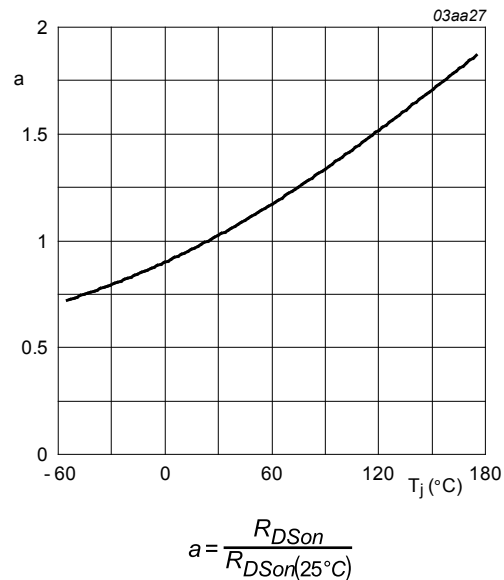


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

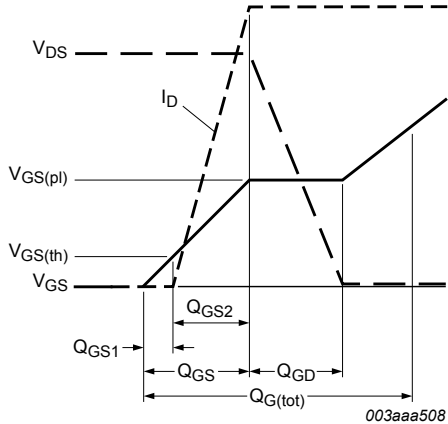


Fig. 14. Gate charge waveform definitions

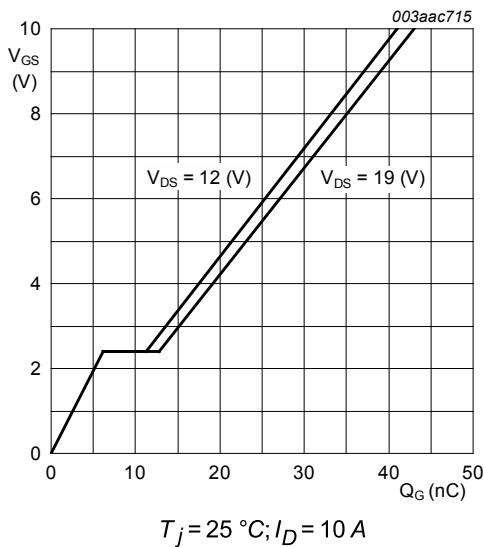


Fig. 15. Gate-source voltage as a function of gate charge; typical values

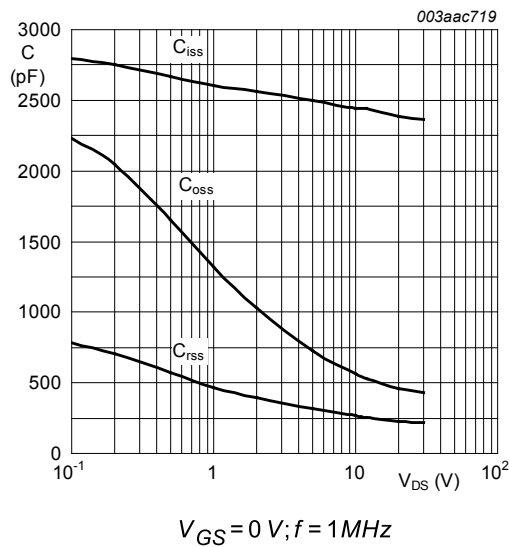


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

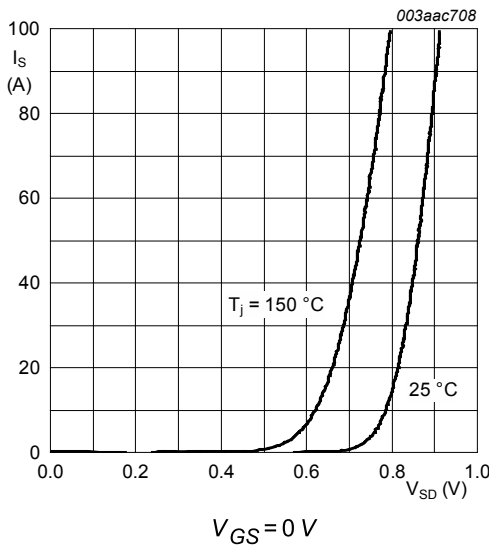


Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

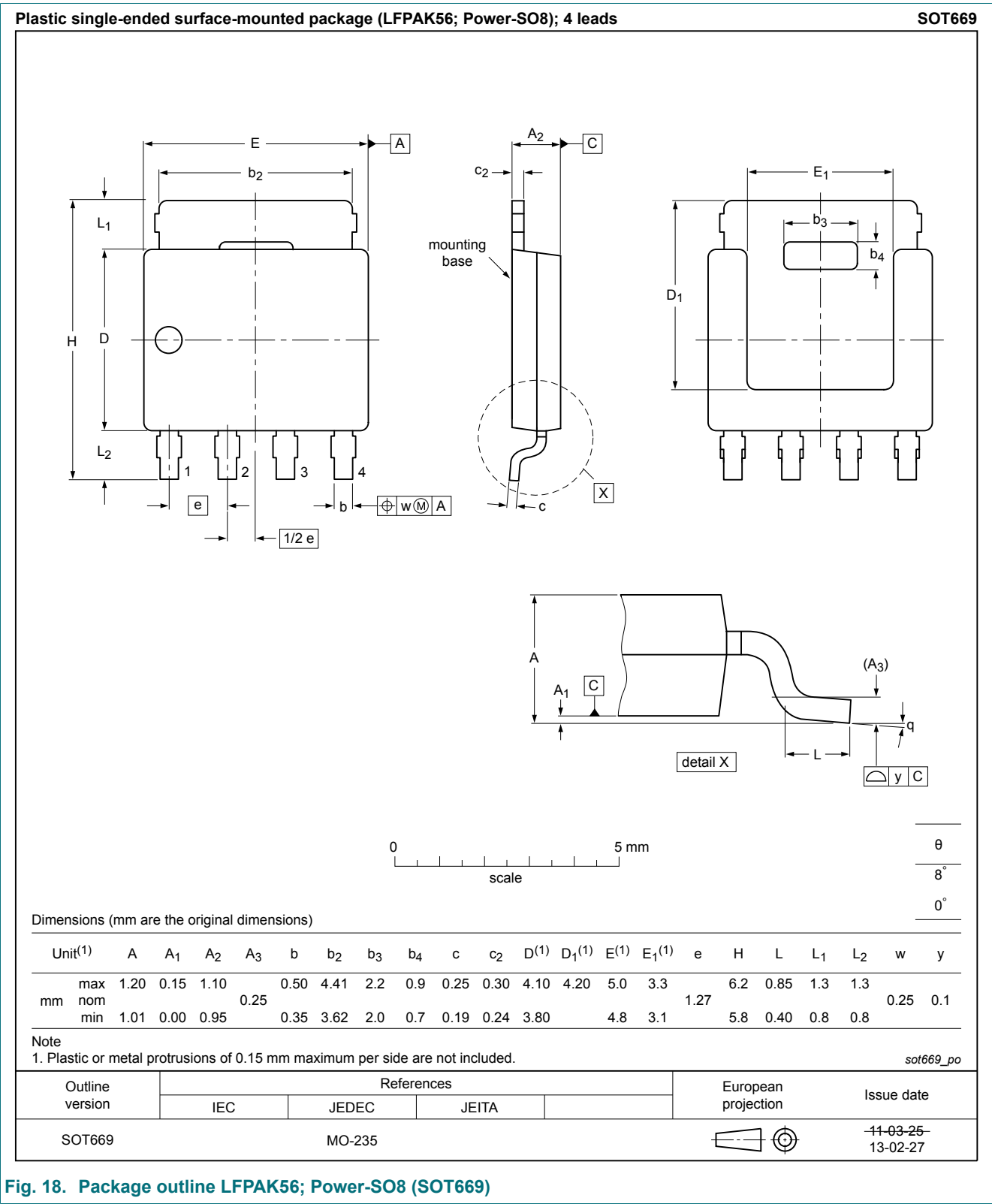


Fig. 18. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

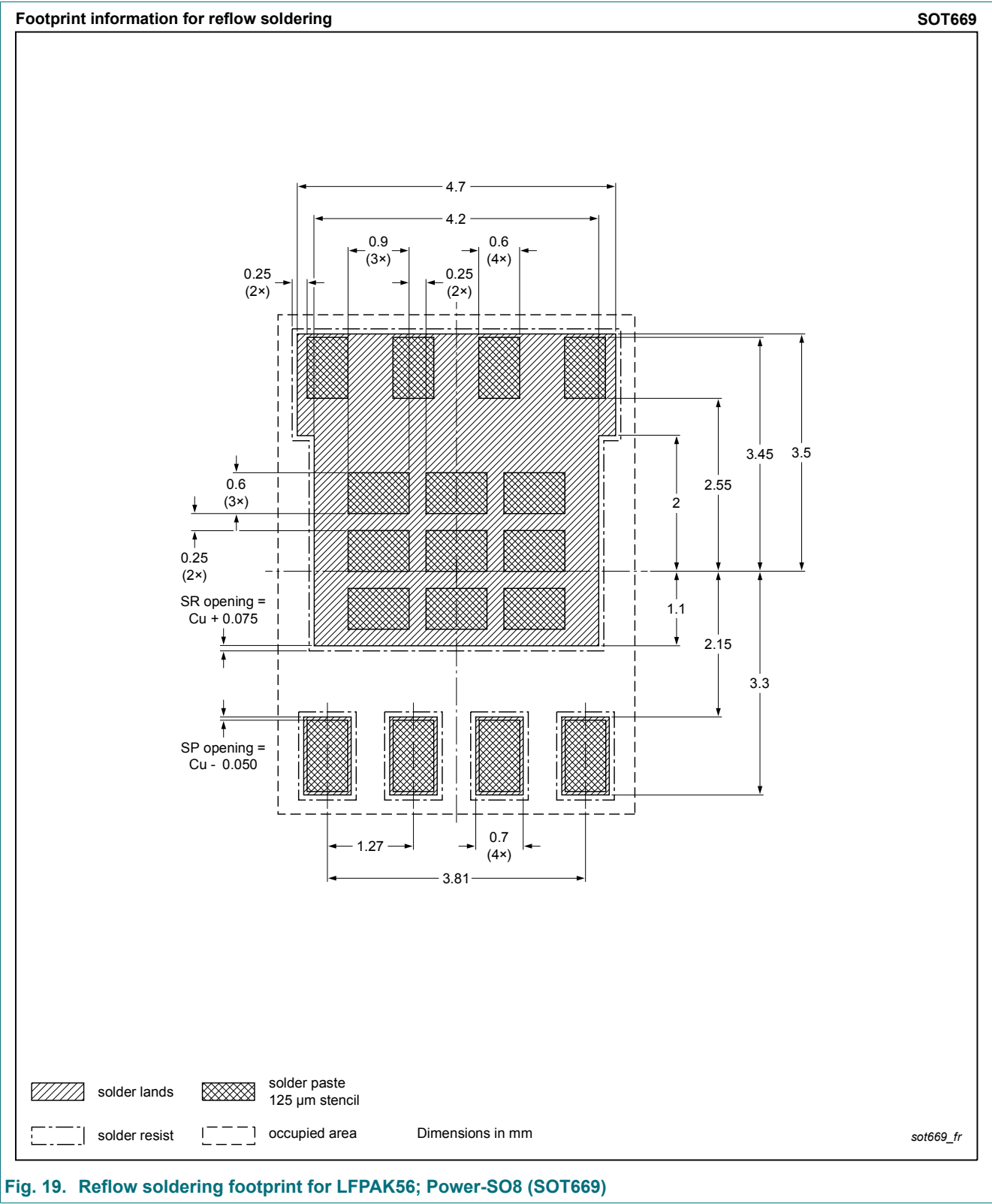


Fig. 19. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)

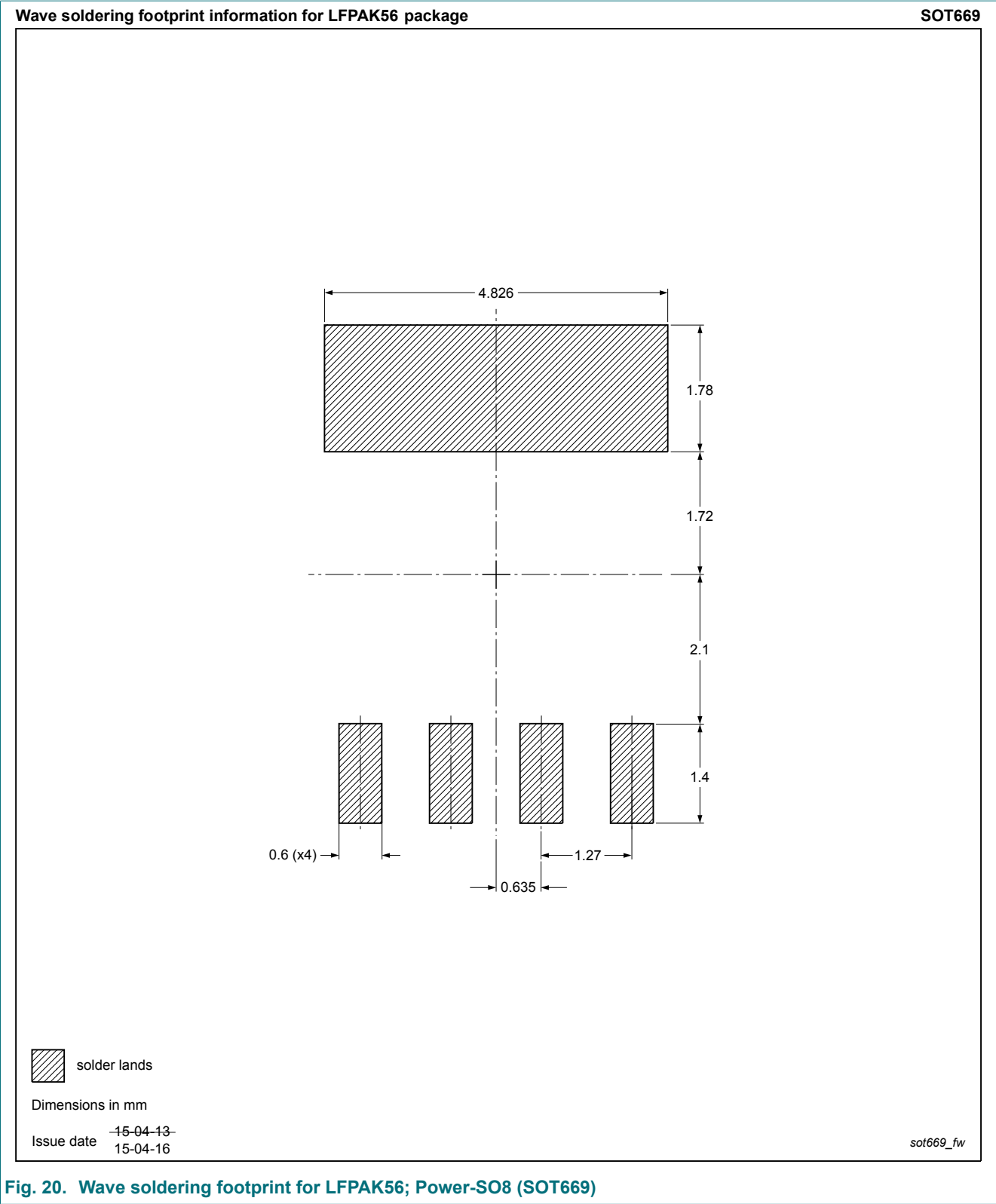


Fig. 20. Wave soldering footprint for LPAK56; Power-SO8 (SOT669)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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