

# HEF4021B

## 8-bit static shift register

Rev. 12 — 8 August 2024

Product data sheet

### 1. General description

The HEF4021B is an 8-bit static shift register (parallel-to-serial converter) with a synchronous serial data input (DS), a clock input (CP), an asynchronous active HIGH parallel load input (PL), eight asynchronous parallel data inputs (D0 to D7) and buffered parallel outputs from the last three stages (Q5 to Q7). Each register stage is a D-type master-slave flip-flop with a set direct (SD) and clear direct (CD) input. Information on D0 to D7 is asynchronously loaded into the register while PL is HIGH, independent of CP and DS. When PL is LOW, data on DS is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. Schmitt trigger action makes the clock input highly tolerant of slower rise and fall times.

The device operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### 2. Features and benefits

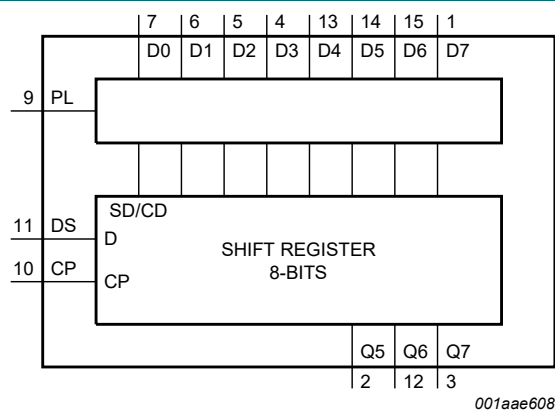
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Tolerant of slower rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

### 3. Ordering information

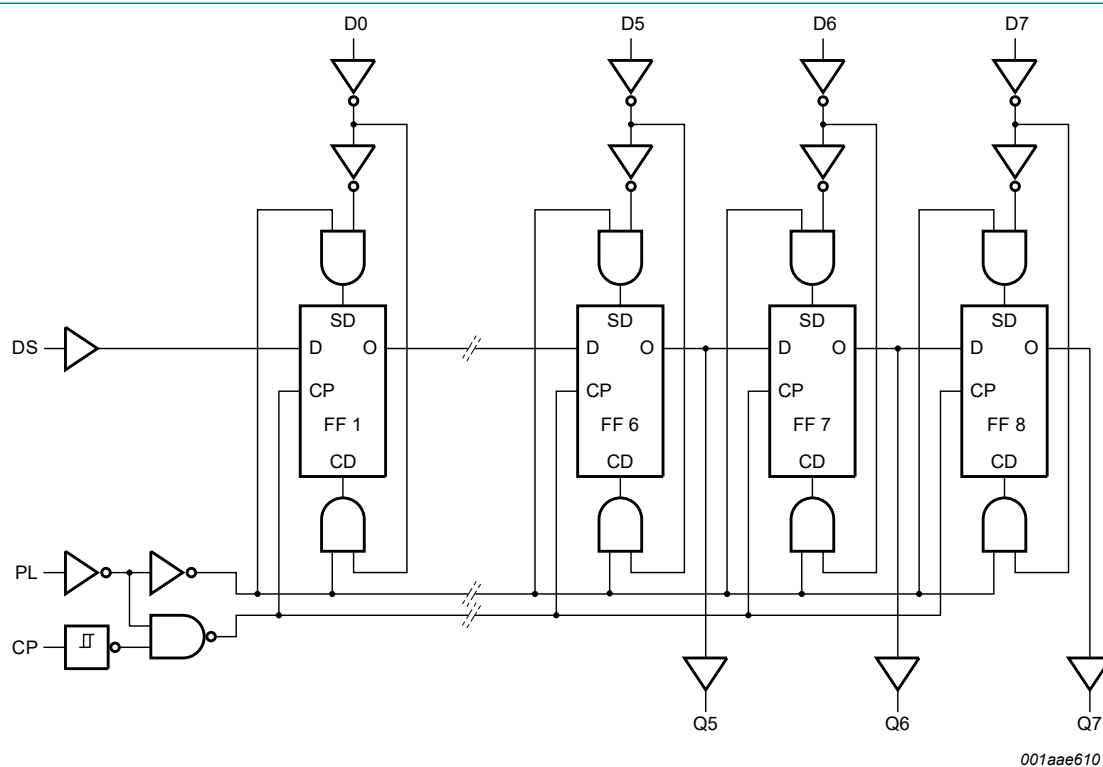
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">HEF4021BT</a>	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	<a href="#">SOT109-1</a>
<a href="#">HEF4021BTT</a>	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	<a href="#">SOT403-1</a>

#### 4. Functional diagram



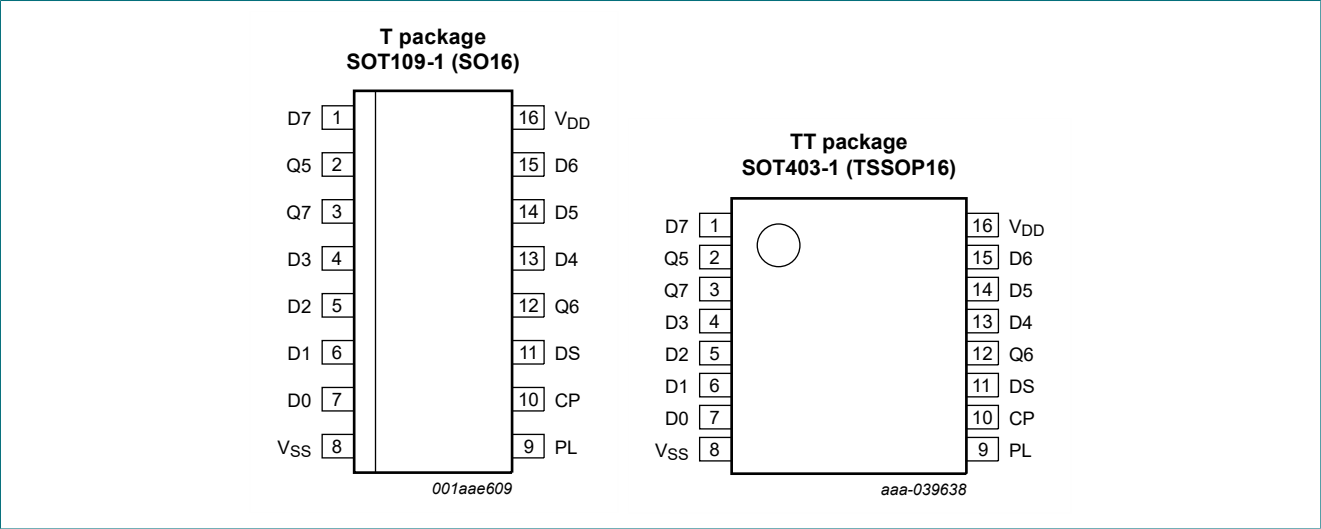
**Fig. 1. Functional diagram**



**Fig. 2. Logic diagram**

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q5, Q6, Q7	2, 12, 3	buffered parallel output from the last three stages
D0, D1, D2, D3, D4, D5, D6, D7	7, 6, 5, 4, 13, 14, 15, 1	parallel data input
VSS	8	ground supply voltage
PL	9	parallel load input
CP	10	clock input (LOW-to-HIGH edge-triggered)
DS	11	serial data input
VDD	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;  
↑ = LOW to HIGH clock transition; ↓ = HIGH to LOW clock transition;  
data n = data (HIGH or LOW) on the DS input at the n<sup>th</sup> ↑ CP transition.

Number of clock transitions	Inputs			Outputs		
	CP	DS	PL	Q5	Q6	Q7
Serial operation						
1	↑	data 1	L	X	X	X
2	↑	data 2	L	X	X	X
3	↑	data 3	L	X	X	X
6	↑	X	L	data 1	X	X
7	↑	X	L	data 2	data 1	X
8	↑	X	L	data 3	data 2	data 1
	↓	X	L	no change	no change	no change
Parallel operation						
	X	X	H	D5	D6	D7

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+18	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA
V <sub>I</sub>	input voltage		-0.5	V <sub>DD</sub> + 0.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA
I <sub>I/O</sub>	input/output current		-	±10	mA
I <sub>DD</sub>	supply current		-	50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+125	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> -40 °C to +125 °C [1]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SOT109-1 (SO16) package: P<sub>tot</sub> derates linearly with 12.4 mW/K above 110 °C.  
For SOT403-1 (TSSOP16) package: P<sub>tot</sub> derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	supply voltage		3	-	15	V
V <sub>I</sub>	input voltage		0	-	V <sub>DD</sub>	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>DD</sub> = 5 V	-	-	3.75	μs/V
		V <sub>DD</sub> = 10 V	-	-	0.5	μs/V
		V <sub>DD</sub> = 15 V	-	-	0.08	μs/V

9. Static characteristics

Table 6. Static characteristics

V<sub>SS</sub> = 0 V; V<sub>I</sub> = V<sub>SS</sub> or V<sub>DD</sub> unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = +25 °C		T <sub>amb</sub> = +85 °C		T <sub>amb</sub> = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	I <sub>O</sub>   < 1 μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V <sub>IL</sub>	LOW-level input voltage	I <sub>O</sub>   < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>O</sub>   < 1 μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub>   < 1 μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I <sub>OH</sub>	HIGH-level output current	V <sub>O</sub> = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		V <sub>O</sub> = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V <sub>O</sub> = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V <sub>O</sub> = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I <sub>OL</sub>	LOW-level output current	V <sub>O</sub> = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V <sub>O</sub> = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V <sub>O</sub> = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I <sub>I</sub>	input leakage current	V <sub>DD</sub> = 15 V	15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>DD</sub>	supply current	I <sub>O</sub> = 0 A	5 V	-	5	-	5	-	150	-	150	μA
			10 V	-	10	-	10	-	300	-	300	μA
			15 V	-	20	-	20	-	600	-	600	μA
C <sub>I</sub>	input capacitance		-	-	-	-	7.5	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula[1]	Min	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	CP to Qn; see Fig. 3	5 V	98 ns + (0.55 ns/pF)C <sub>L</sub>	-	125	250	ns
			10 V	44 ns + (0.23 ns/pF)C <sub>L</sub>	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C <sub>L</sub>	-	40	80	ns
		PL to Qn; see Fig. 3	5 V	93 ns + (0.55 ns/pF)C <sub>L</sub>	-	120	240	ns
			10 V	44 ns + (0.23 ns/pF)C <sub>L</sub>	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C <sub>L</sub>	-	40	80	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	CP to Qn; see Fig. 3	5 V	88 ns + (0.55 ns/pF)C <sub>L</sub>	-	115	230	ns
			10 V	39 ns + (0.23 ns/pF)C <sub>L</sub>	-	50	100	ns
			15 V	32 ns + (0.16 ns/pF)C <sub>L</sub>	-	40	80	ns
		PL to Qnl; see Fig. 3	5 V	78 ns + (0.55 ns/pF)C <sub>L</sub>	-	105	210	ns
			10 V	39 ns + (0.23 ns/pF)C <sub>L</sub>	-	50	100	ns
			15 V	32 ns + (0.16 ns/pF)C <sub>L</sub>	-	40	80	ns
t <sub>t</sub>	transition time	Qn; see Fig. 3	5 V	10 ns + (1.00 ns/pF)C <sub>L</sub>	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C <sub>L</sub>	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C <sub>L</sub>	-	20	40	ns
t <sub>su</sub>	set-up time	DS to CP; see Fig. 4	5 V		+25	-15	-	ns
			10 V		+25	-10	-	ns
			15 V		+15	-5	-	ns
		Dn to PL; see Fig. 5	5 V		50	25	-	ns
			10 V		30	10	-	ns
			15 V		20	5	-	ns
t <sub>h</sub>	hold time	DS to CP; see Fig. 4	5 V		40	20	-	ns
			10 V		20	10	-	ns
			15 V		15	8	-	ns
		Dn to PL; see Fig. 5	5 V		+15	-10	-	ns
			10 V		15	0	-	ns
			15 V		15	0	-	ns
t <sub>w</sub>	pulse width	CP = LOW; minimum width; see Fig. 4	5 V		70	35	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
		PL = HIGH; minimum width; see Fig. 5	5 V		70	35	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
t <sub>rec</sub>	recovery time	PL input; see Fig. 5	5 V		50	10	-	ns
			10 V		40	5	-	ns
			15 V		35	5	-	ns

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula[1]	Min	Typ	Max	Unit
f <sub>clk(max)</sub>	maximum clock frequency	CP input; see Fig. 4	5 V		6	13	-	MHz
			10 V		15	30	-	MHz
			15 V		20	40	-	MHz

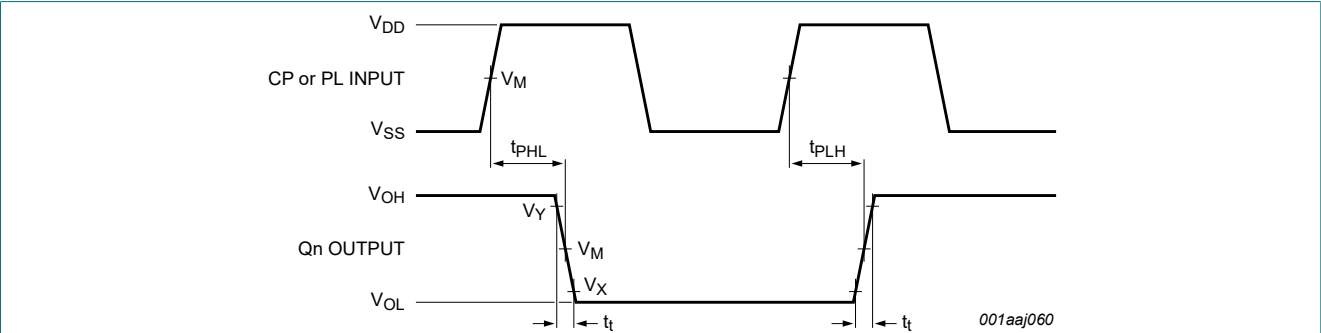
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C<sub>L</sub> in pF).

**Table 8. Dynamic power dissipation P<sub>D</sub>**

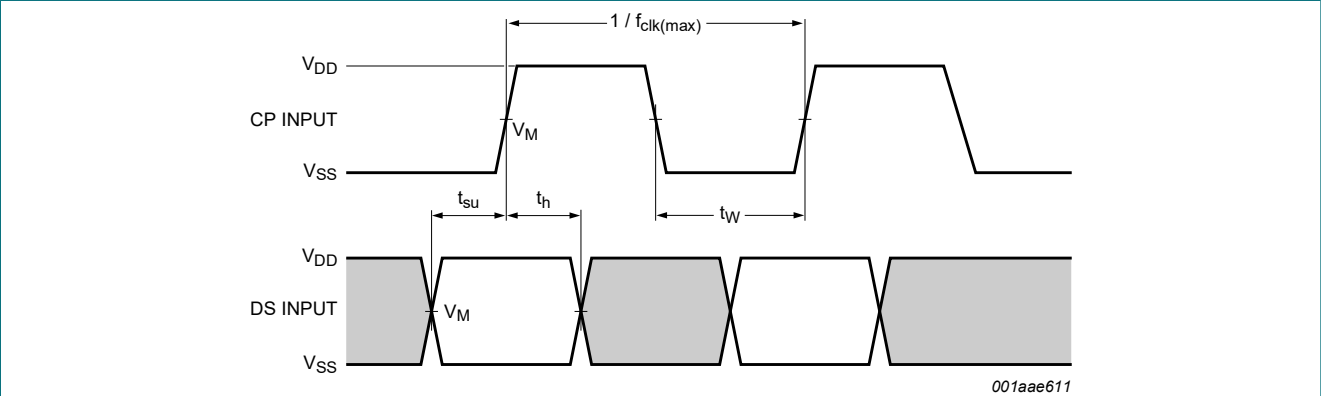
P<sub>D</sub> can be calculated from the formulas shown. V<sub>SS</sub> = 0 V; t<sub>r</sub> = t<sub>f</sub> ≤ 20 ns; T<sub>amb</sub> = 25 °C.

Symbol	Parameter	V <sub>DD</sub>	Typical formula for P <sub>D</sub> (μW)	where:
P <sub>D</sub>	dynamic power dissipation	5 V	$P_D = 900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f <sub>i</sub> = input frequency in MHz f <sub>o</sub> = output frequency in MHz C <sub>L</sub> = output load capacitance in pF V <sub>DD</sub> = supply voltage in V Σ(f <sub>o</sub> × C <sub>L</sub> ) = sum of the outputs
		10 V	$P_D = 4300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 12000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

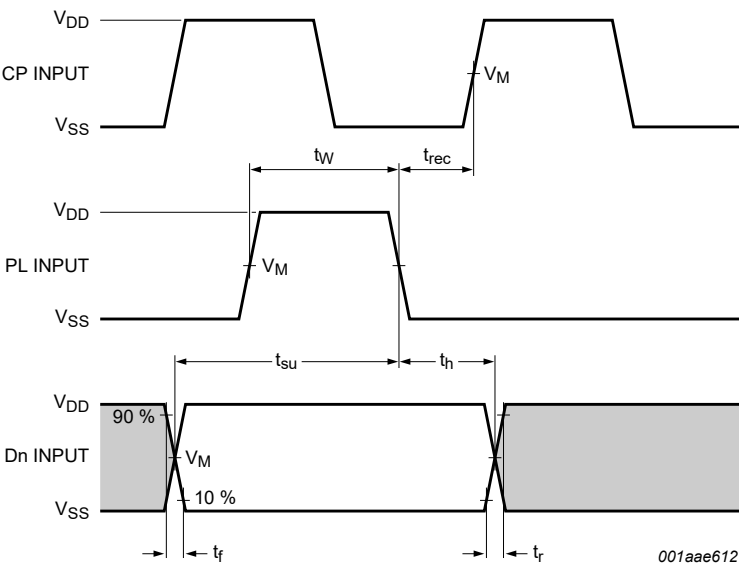
### 10.1. Waveforms and test circuit



**Fig. 3. Waveforms showing propagation delays for CP and PL inputs to Qn output and Qn transition times**



**Fig. 4. Waveforms showing minimum clock pulse width, set-up time, and hold time for CP and DS**

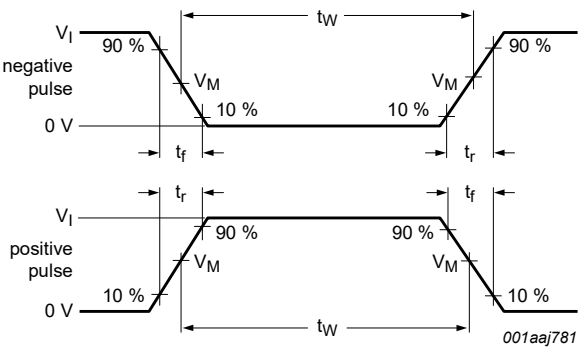


Set-up times and hold times are shown as positive values but may be specified as negative values. Measurement points are given in [Table 9](#).

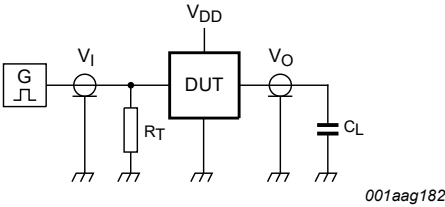
**Fig. 5. Waveforms showing minimum pulse width and recovery time for PL; set-up and hold times for Dn to PL**

**Table 9. Measurement points**

Supply voltage	Input	Output		
$V_{DD}$	$V_M$	$V_M$	$V_X$	$V_Y$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_{DD}$	$0.9V_{DD}$



a. Input waveform



b. Test circuit

Test data is given in [Table 10](#).

Definitions test circuit:

$C_L$  = load capacitance including jig and probe capacitance;

$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

**Fig. 6. Test circuit for measuring switching times**



Table 10. Test data

Supply voltage	Input		Load
V <sub>DD</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>
5 V to 15 V	V <sub>SS</sub> or V <sub>DD</sub>	≤ 20 ns	50 pF

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

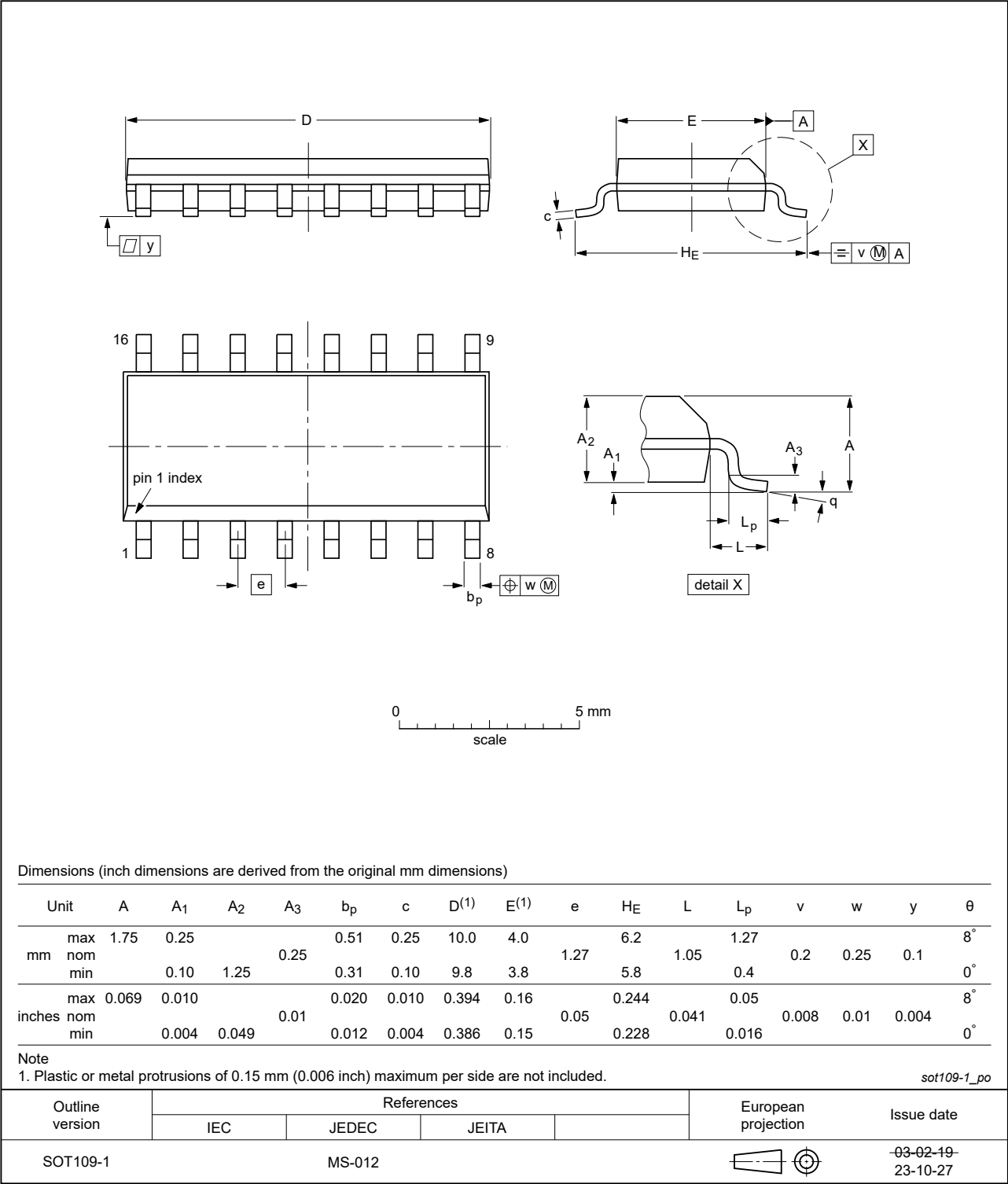


Fig. 7. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

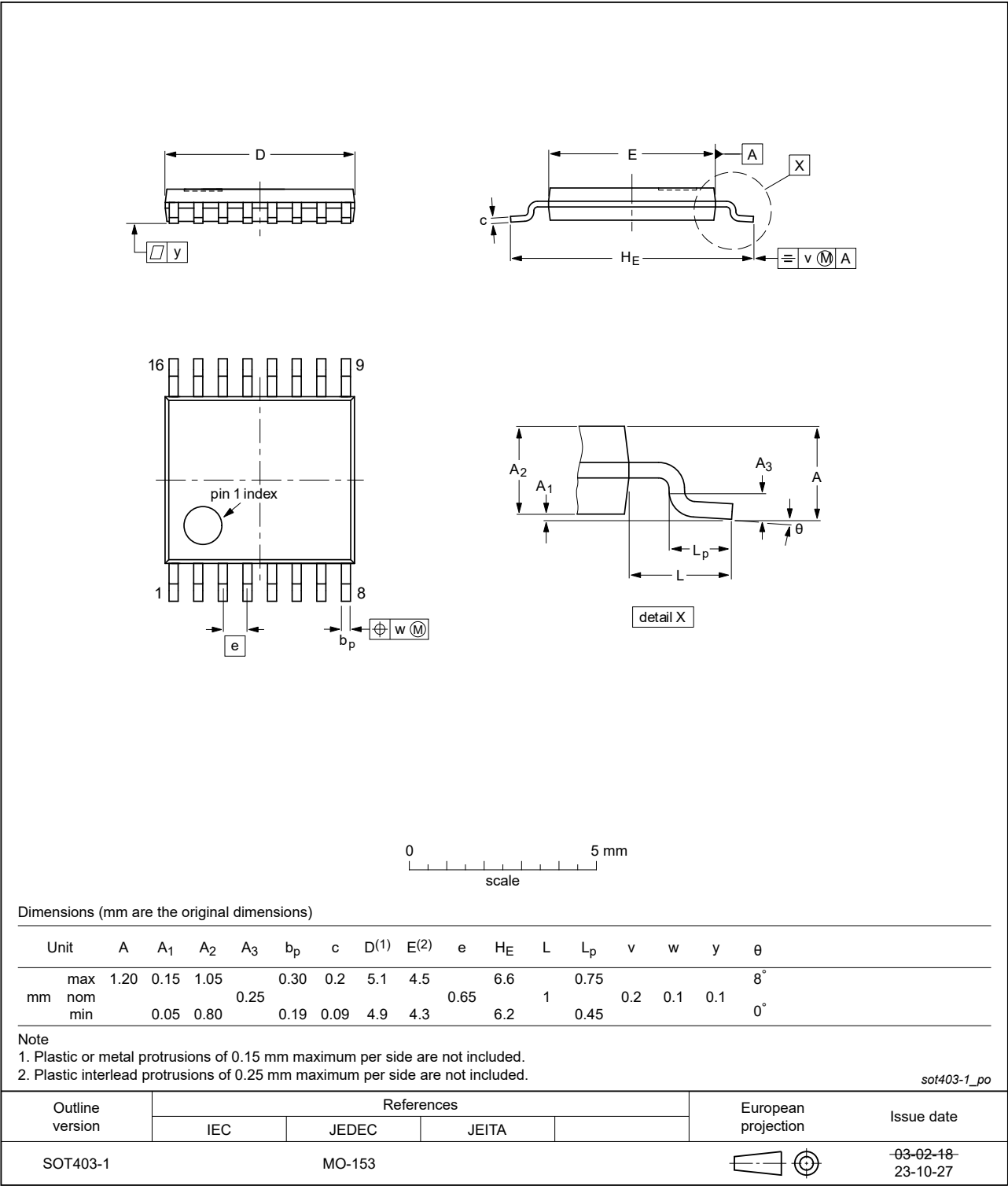


Fig. 8. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4021B v.12	20240808	Product data sheet	-	HEF4021B v.11
Modifications:	<ul style="list-style-type: none"><li>Section 2: ESD specification updated according to the latest JEDEC standard.</li><li>Fig. 7, Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153</li></ul>			
HEF4021B v.11	20211201	Product data sheet	-	HEF4021B v.10
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li>Section 2 updated.</li><li>Table 4: Derating values for P<sub>tot</sub> total power dissipation updated.</li></ul>			
HEF4021B v.10	20160321	Product data sheet	-	HEF4021B v.9
Modifications:	<ul style="list-style-type: none"><li>Type number HEF4021BP (SOT38-4) removed.</li></ul>			
HEF4021B v.9	20130830	Product data sheet	-	HEF4021B v.8
Modifications:	<ul style="list-style-type: none"><li>Added type number HEF4021BTT.</li></ul>			
HEF4021B v.8	20111118	Product data sheet	-	HEF4021B v.7
Modifications:	<ul style="list-style-type: none"><li>Legal pages updated.</li><li>Changes in Section 1 and Section 2.</li><li>Section "Applications" removed.</li></ul>			
HEF4021B v.7	20111010	Product data sheet	-	HEF4021B v.6
HEF4021B v.6	20091127	Product data sheet	-	HEF4021B v.5
HEF4021B v.5	20090707	Product data sheet	-	HEF4021B v.4
HEF4021B v.4	20081110	Product data sheet	-	HEF4021B_CNV v.3
HEF4021B_CNV v.3	19950101	Product specification	-	HEF4021B_CNV v.2
HEF4021B_CNV v.2	19950101	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Ordering information..... 1

4. Functional diagram..... 2

5. Pinning information..... 3

5.1. Pinning..... 3

5.2. Pin description..... 3

6. Functional description..... 4

7. Limiting values..... 4

8. Recommended operating conditions..... 5

9. Static characteristics..... 5

10. Dynamic characteristics..... 6

10.1. Waveforms and test circuit..... 7

11. Package outline..... 10

12. Abbreviations..... 12

13. Revision history..... 12

14. Legal information..... 13

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