

74ALVC74

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 8 — 5 February 2024

Product data sheet

1. General description

The 74ALVC74 is a dual positive edge triggered D-type flip-flop with individual data (D), clock (CP), set ($\overline{SD}$) and reset ($\overline{RD}$) inputs, and complementary Q and $\overline{Q}$ outputs. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output.

Schmitt trigger action on all inputs makes the device tolerant of slow rise and fall times.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

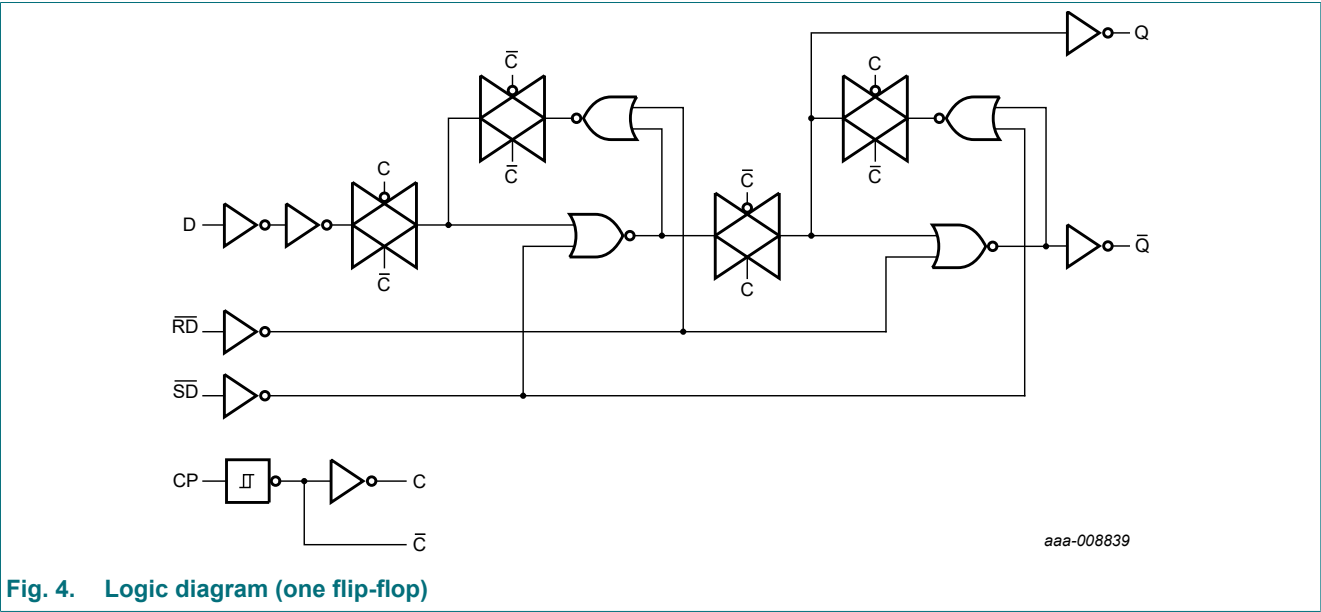
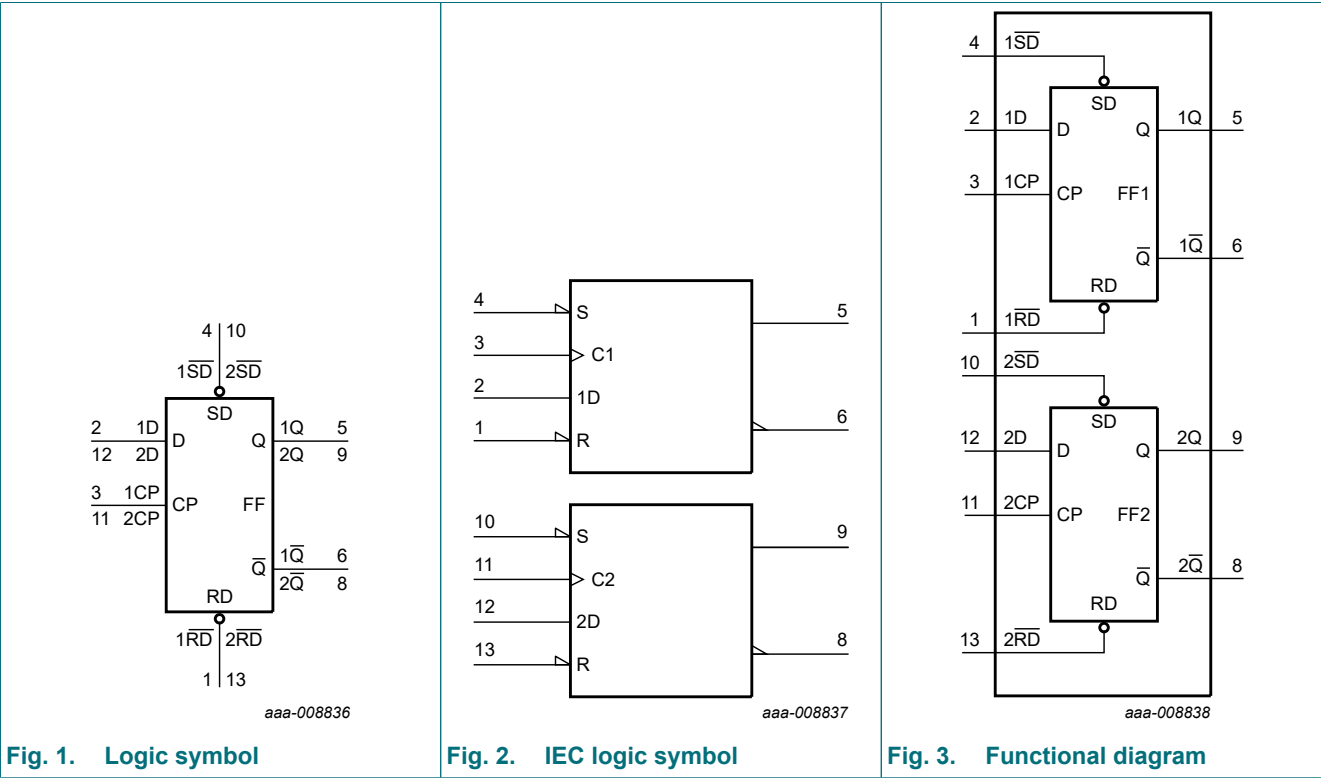
- Wide supply voltage range from 1.65 V to 3.6 V
- CMOS low power dissipation
- Overvoltage tolerant inputs to 3.6 V
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD78 Class II.A
- Complies with JEDEC standard:
 - JESD8-7 (1.65 to 1.95 V)
 - JESD8-5 (2.3 to 2.7 V)
 - JESD8C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

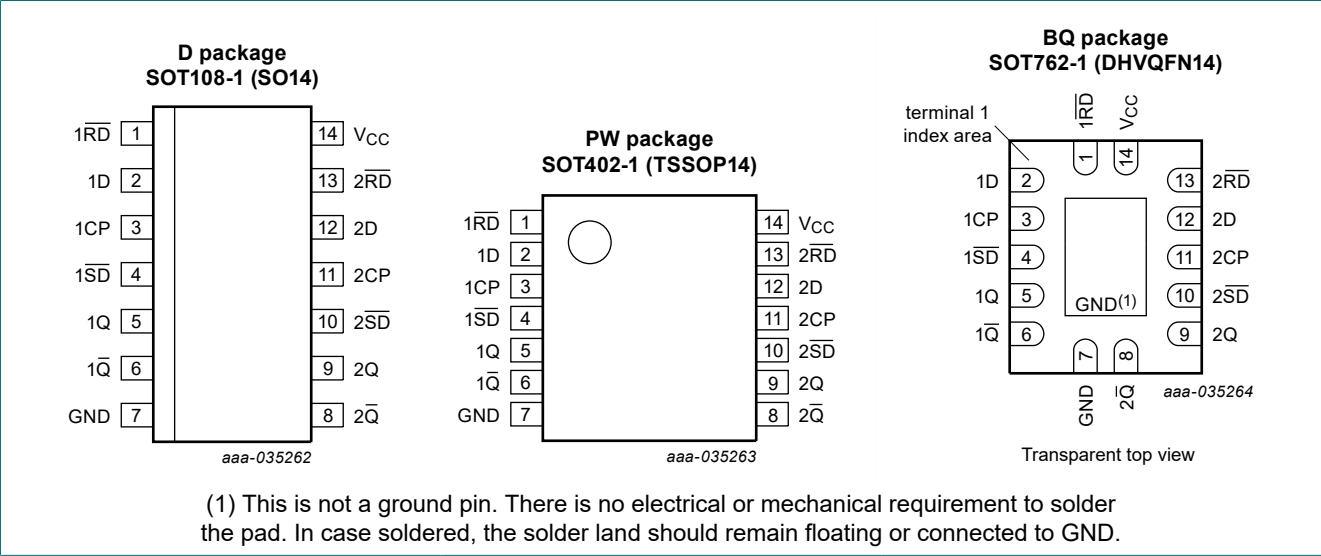
Type number	Package			
	Temperature range	Name	Description	Version
74ALVC74D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ALVC74PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ALVC74BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1RD	1	asynchronous reset-direct input (active-LOW)
1D	2	data input
1CP	3	clock input (LOW-to-HIGH), edge-triggered
1SD	4	asynchronous set-direct input (active-LOW)
1Q	5	true flip-flop output
1Q	6	complement flip-flop output
GND	7	ground (0 V)
2Q	8	complement flip-flop output
2Q	9	true flip-flop output
2SD	10	asynchronous set-direct input (active-LOW)
2CP	11	clock input (LOW-to-HIGH), edge-triggered
2D	12	data input
2RD	13	asynchronous reset-direct input (active-LOW)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition;
nQ_{n+1} = state after the next LOW-to-HIGH CP transition.

Input				Output			
nSD	nRD	nCP	nD	nQ	nQ	nQ _{n+1}	nQ _{n+1}
L	H	X	X	H	L	-	-
H	L	X	X	L	H	-	-
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	[1]	-0.5	+4.6	V
V _O	output voltage	[1]	-0.5	V _{CC} + 0.5	V
		Power-down mode; V _{CC} = 0 V	[1]	-0.5	+4.6
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		1.65	3.6	V
V _I	input voltage		0	3.6	V
V _O	output voltage	V _{CC} = 1.65 to 3.6 V	0	V _{CC}	V
		Power-down mode; V _{CC} = 0 V	0	3.6	V
T _{amb}	ambient temperature	in free air	-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		V _{CC} = 1.65 V to 3.6 V; I _O = -100 µA	V _{CC} - 0.2	-	-	V _{CC} - 0.2	-	V
		V _{CC} = 1.65 V; I _O = -6 mA	1.25	1.51	-	1.25	-	V
		V _{CC} = 2.3 V; I _O = -12 mA	1.8	2.10	-	1.8	-	V
		V _{CC} = 2.3 V; I _O = -18 mA	1.7	2.01	-	1.7	-	V
		V _{CC} = 2.7 V; I _O = -12 mA	2.2	2.53	-	2.2	-	V
		V _{CC} = 3.0 V; I _O = -18 mA	2.4	2.76	-	2.4	-	V
		V _{CC} = 3.0 V; I _O = -24 mA	2.2	2.68	-	2.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		V _{CC} = 1.65 V to 3.6 V; I _O = 100 µA	-	-	0.2	-	0.2	V
		V _{CC} = 1.65 V; I _O = 6 mA	-	0.11	0.3	-	0.3	V
		V _{CC} = 2.3 V; I _O = 12 mA	-	0.17	0.4	-	0.4	V
		V _{CC} = 2.3 V; I _O = 18 mA	-	0.25	0.6	-	0.6	V
		V _{CC} = 2.7 V; I _O = 12 mA	-	0.16	0.4	-	0.4	V
		V _{CC} = 3.0 V; I _O = 18 mA	-	0.23	0.4	-	0.45	V
		V _{CC} = 3.0 V; I _O = 24 mA	-	0.30	0.55	-	0.55	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	±0.1	±5	-	±20	µA
I _{OFF}	power-off leakage current	V _{CC} = GND; V _I or V _O = 3.6 V	-	±0.1	±10	-	±80	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.2	10	-	80	µA
ΔI _{CC}	additional supply current	V _{CC} = 3.0 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	750	-	750	µA
C _I	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V): for test circuit, see Fig. 7.

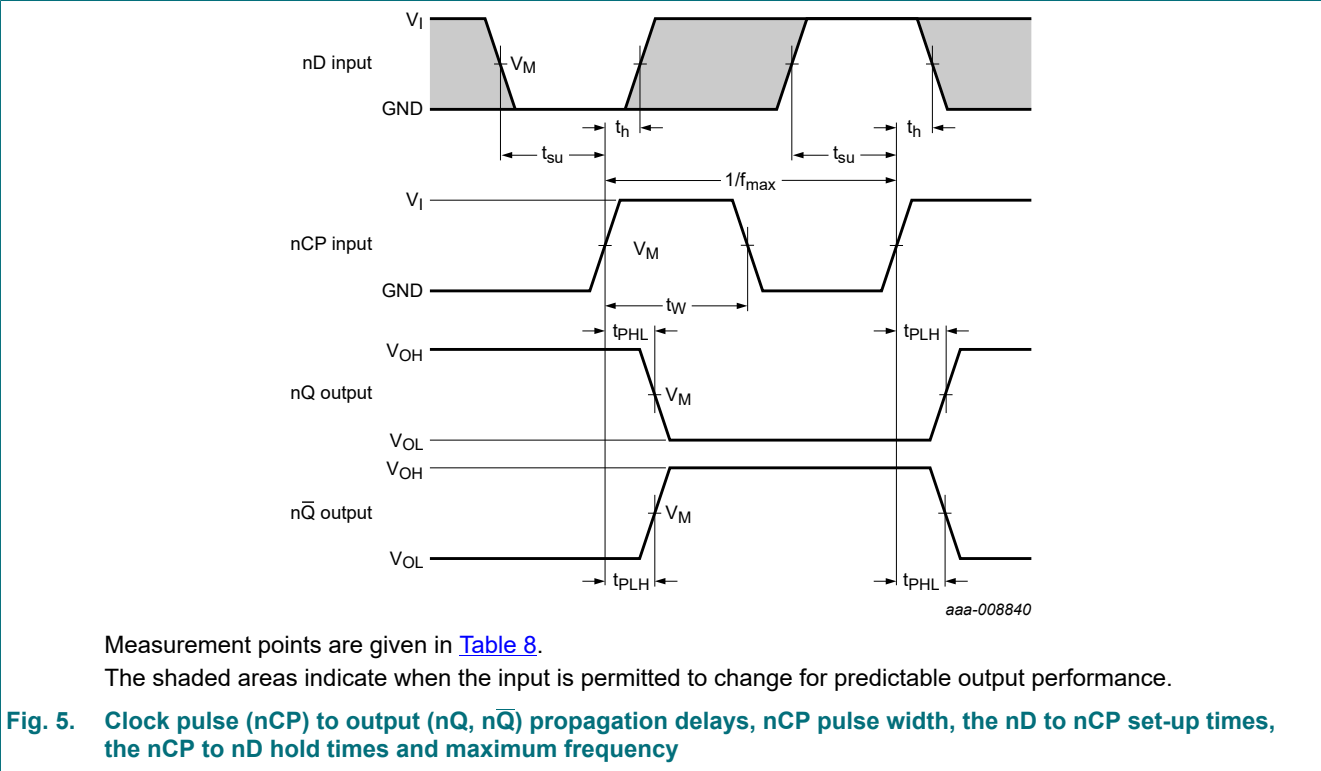
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nCP to nQ, nQ̄; see Fig. 5 [2]						
		V _{CC} = 1.65 to 1.95 V	1.0	3.7	6.2	1.0	7.1	ns
		V _{CC} = 2.3 to 2.7 V	1.0	2.6	4.2	1.0	4.8	ns
		V _{CC} = 2.7 V	1.0	2.8	4.2	1.0	4.8	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.7	3.8	1.0	4.4	ns
		nSD̄ to nQ, nQ̄; see Fig. 6						
		V _{CC} = 1.65 to 1.95 V	1.0	3.4	5.4	1.0	6.2	ns
		V _{CC} = 2.3 to 2.7 V	1.0	2.4	3.8	1.0	4.4	ns
		V _{CC} = 2.7 V	1.0	3.2	4.2	1.0	4.8	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.3	3.5	1.0	4.0	ns
		nRD̄ to nQ, nQ̄; see Fig. 6						
		V _{CC} = 1.65 to 1.95 V	1.0	3.5	5.4	1.0	6.2	ns
		V _{CC} = 2.3 to 2.7 V	1.0	2.5	3.8	1.0	4.4	ns
		V _{CC} = 2.7 V	1.0	3.1	4.2	1.0	4.8	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.3	3.5	1.0	4.0	ns
t _w	pulse width	nCP; HIGH or LOW; see Fig. 5						
		V _{CC} = 1.65 to 1.95 V	2.5	0.9	-	2.5	-	ns
		V _{CC} = 2.3 to 2.7 V	2.5	0.6	-	2.5	-	ns
		V _{CC} = 2.7 V	2.5	1.3	-	2.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	2.5	1.3	-	2.5	-	ns
		nSD̄ or nRD̄; LOW; see Fig. 6						
		V _{CC} = 1.65 to 1.95 V	2.5	0.9	-	2.5	-	ns
		V _{CC} = 2.3 to 2.7 V	2.5	0.6	-	2.5	-	ns
		V _{CC} = 2.7 V	2.5	1.0	-	2.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	2.5	0.7	-	2.5	-	ns
t _{rec}	recovery time	nRD̄ to nCP; see Fig. 6						
		V _{CC} = 1.65 to 1.95 V	0.7	-0.1	-	0.7	-	ns
		V _{CC} = 2.3 to 2.7 V	0.7	-0.1	-	0.7	-	ns
		V _{CC} = 2.7 V	0.7	-0.1	-	0.7	-	ns
		V _{CC} = 3.0 V to 3.6 V	0.7	-0.1	-	0.7	-	ns
t _{su}	set-up time	nD to nCP; see Fig. 5						
		V _{CC} = 1.65 to 1.95 V	1.2	0.6	-	1.2	-	ns
		V _{CC} = 2.3 to 2.7 V	1.2	0.8	-	1.2	-	ns
		V _{CC} = 2.7 V	0.9	0.5	-	0.9	-	ns
		V _{CC} = 3.0 V to 3.6 V	0.8	0.4	-	0.8	-	ns

Dual D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _h	hold time	nD to nCP; see Fig. 5						
		V _{CC} = 1.65 to 1.95 V	0.6	-0.4	-	0.6	-	ns
		V _{CC} = 2.3 to 2.7 V	0.6	-0.3	-	0.6	-	ns
		V _{CC} = 2.7 V	0.7	-0.4	-	0.7	-	ns
		V _{CC} = 3.0 V to 3.6 V	0.8	-0.1	-	0.8	-	ns
f _{max}	maximum frequency	nCP; see Fig. 5						
		V _{CC} = 1.65 to 1.95 V	150	275	-	150	-	MHz
		V _{CC} = 2.3 to 2.7 V	200	325	-	200	-	MHz
		V _{CC} = 2.7 V	250	375	-	250	-	MHz
		V _{CC} = 3.0 V to 3.6 V	300	425	-	300	-	MHz
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} ; V _{CC} = 3.3 V [3]	-	35	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C.
Typical values are measured at V_{CC} = 1.8 V for V_{CC} = 1.65 V to 1.95 V.
Typical values are measured at V_{CC} = 2.5 V for V_{CC} = 2.3 V to 2.7 V.
Typical values are measured at V_{CC} = 3.3 V for V_{CC} = 3.0 V to 3.6 V
- [2] t_{pd} is the same as t_{PHL} and t_{PLH}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$, where:
f_i = input frequency in MHz; f_o = output frequency in MHz;
N = total load switching outputs; C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



Dual D-type flip-flop with set and reset; positive-edge trigger

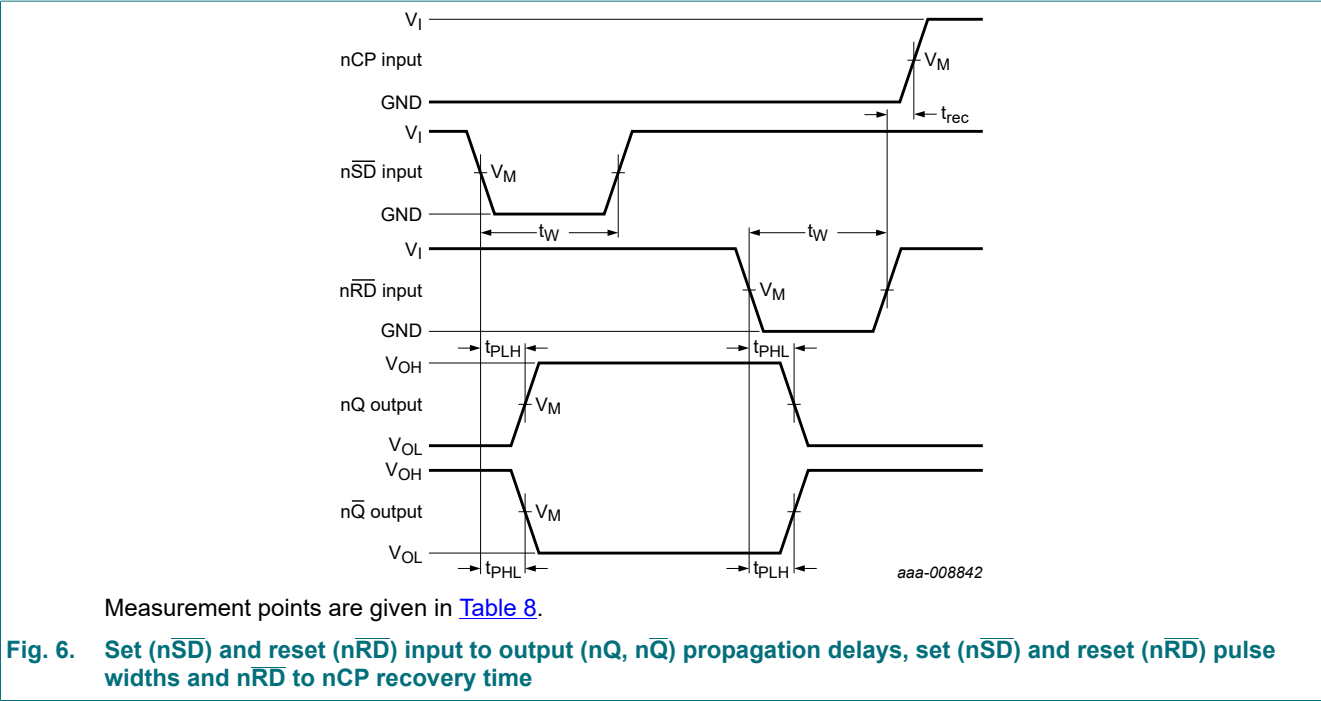


Table 8. Measurement points

Supply voltage	Input		Output
V_{CC}	V_I	V_M	V_M
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V

Dual D-type flip-flop with set and reset; positive-edge trigger

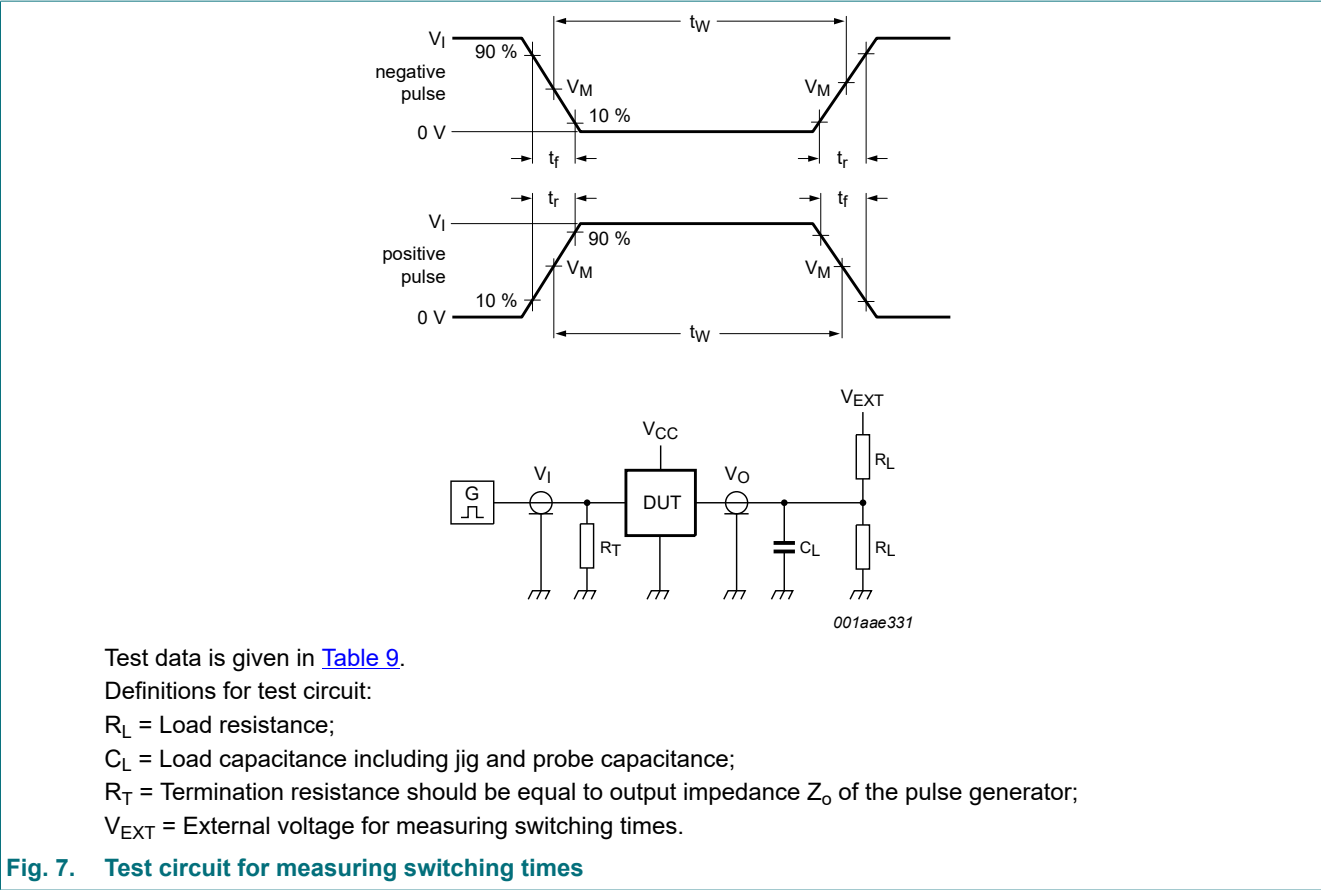


Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

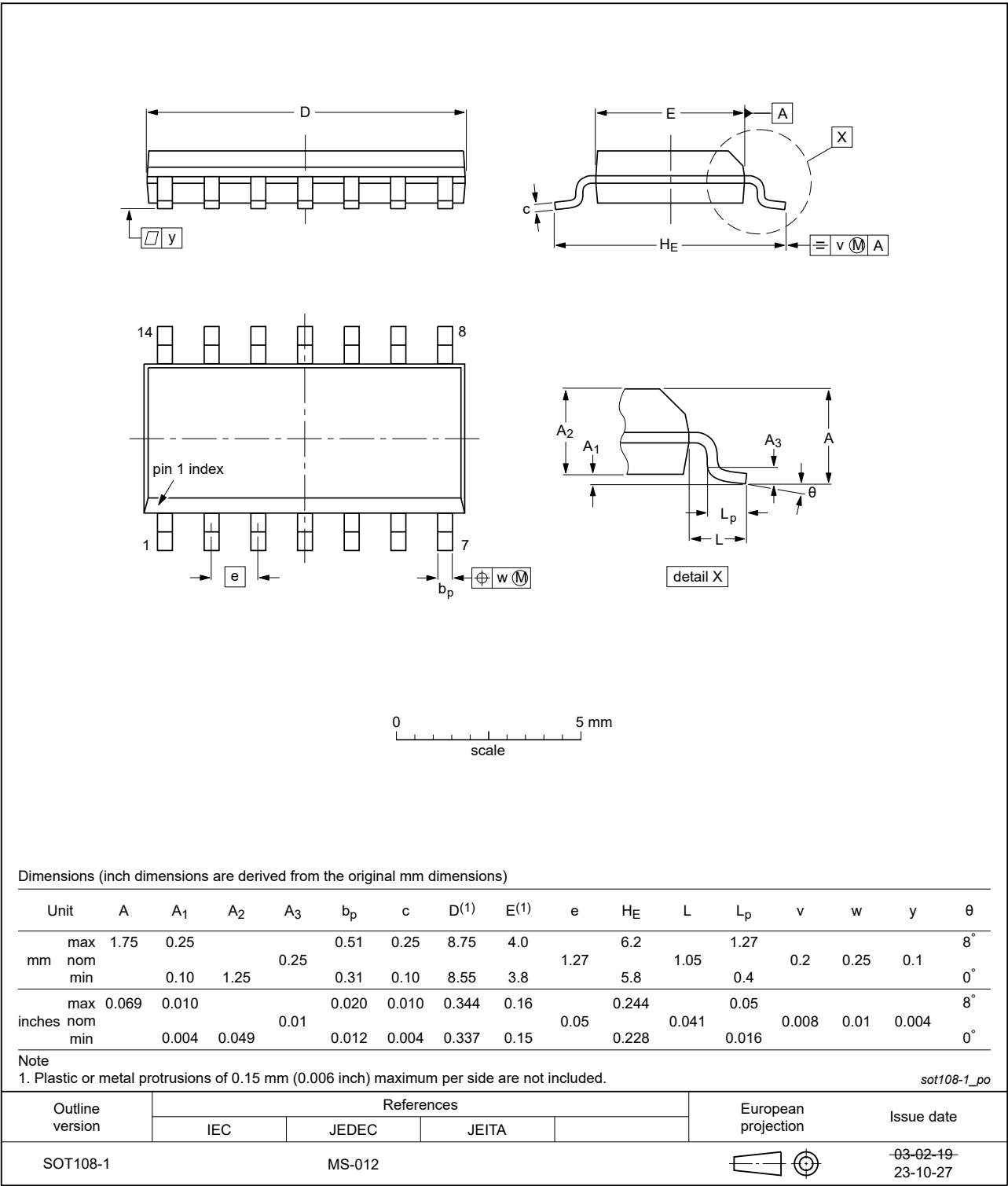


Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

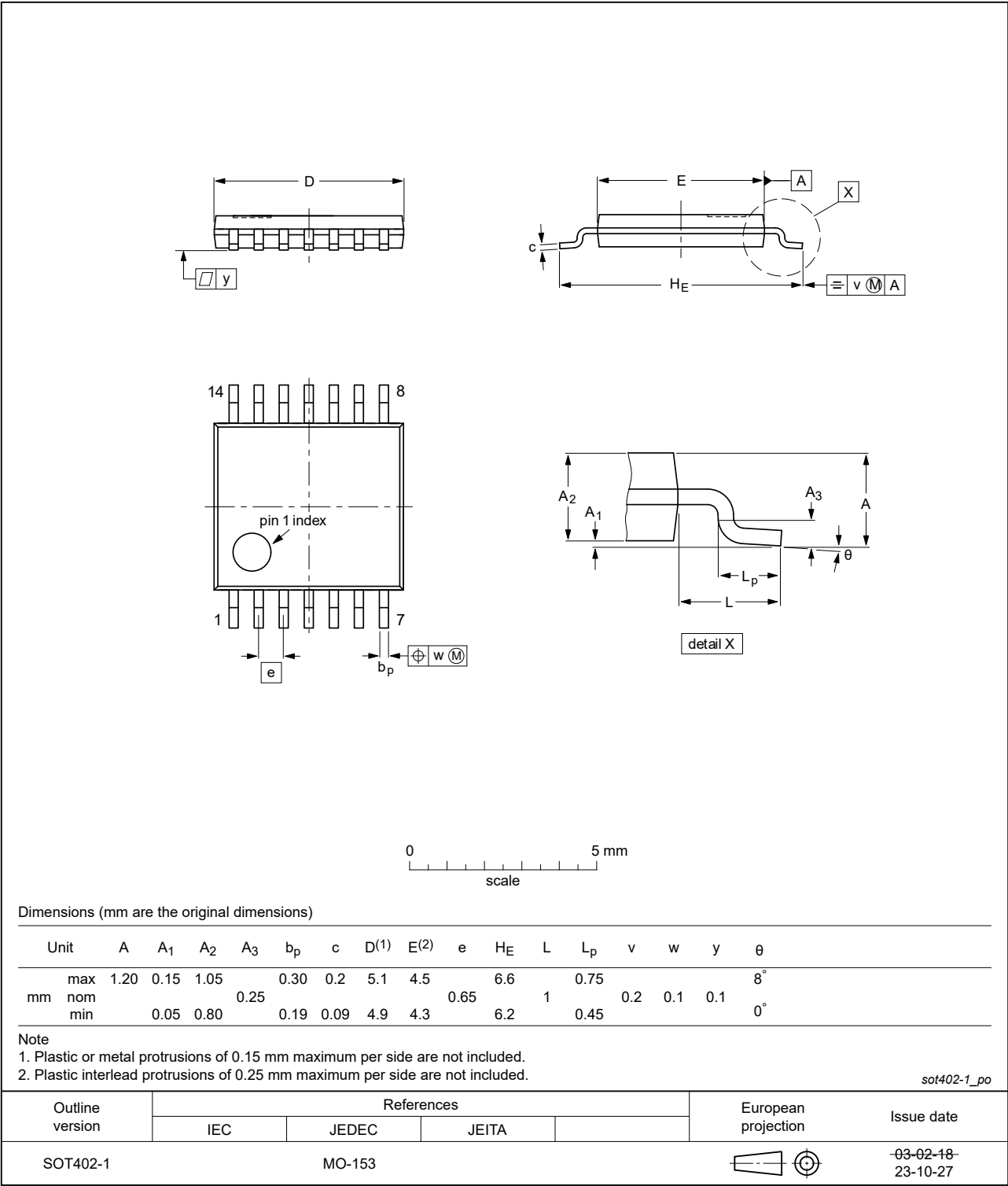


Fig. 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

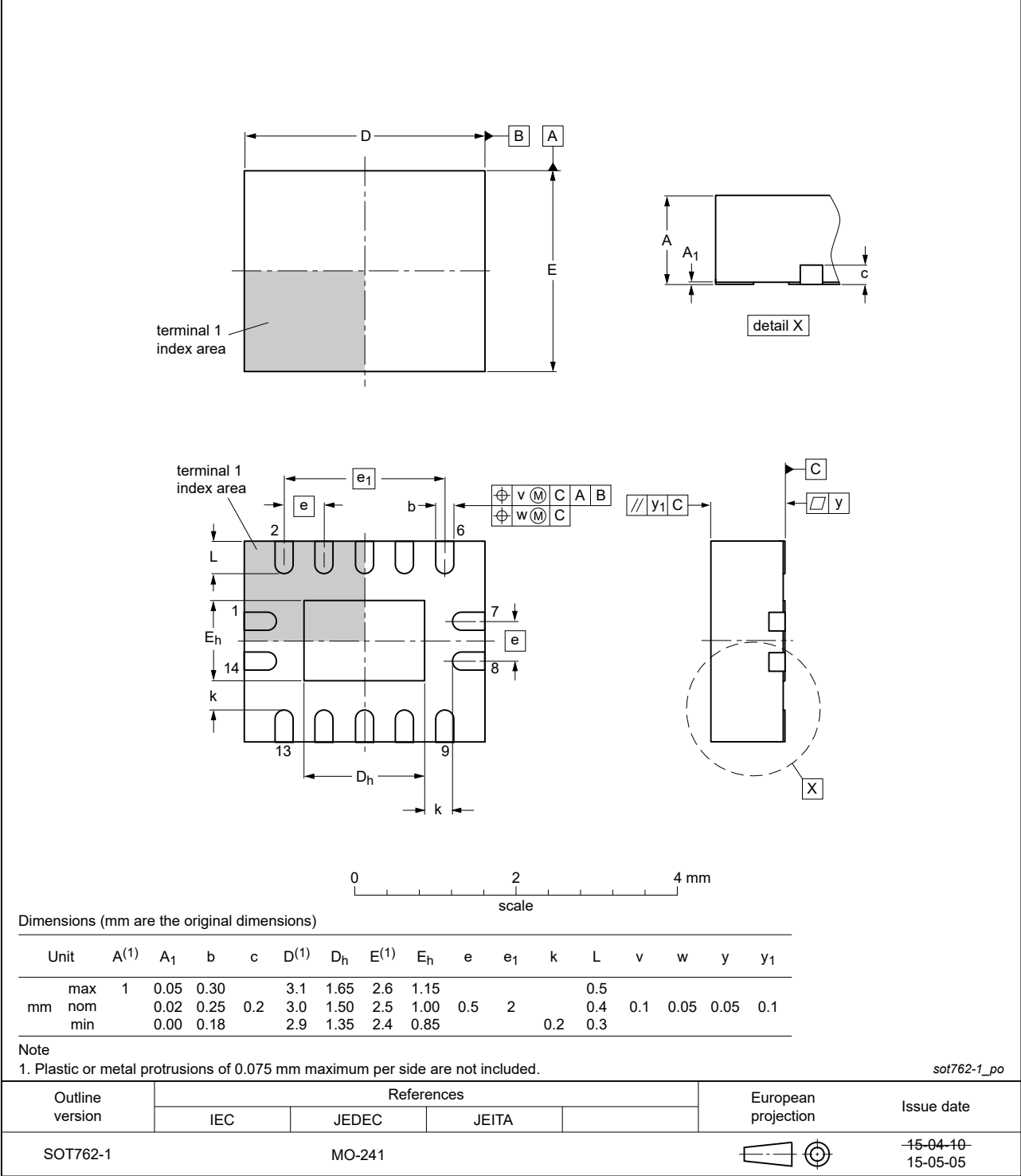


Fig. 10. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC74 v.8	20240205	Product data sheet	-	74ALVC74 v.7
Modifications:	Fig. 8, Fig. 9: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74ALVC74 v.7	20230707	Product data sheet	-	74ALVC74 v.6
Modifications:	Section 1 updated. Section 2: updated; ESD specification updated according to the latest JEDEC standard. - Specifications for -40 °C to +125 °C added.			
74ALVC74 v.6	20210727	Product data sheet	-	74ALVC74 v.5
Modifications:	Section 10: Minimum set-up time (t_{su(min)}) at V_{CC} = 2.7 V changed to 1.1 ns. (errata)			
74ALVC74 v.5	20210430	Product data sheet	-	74ALVC74 v.4
Modifications:	Section 2: Reference to JESD36 removed. Section 7: Derating values for P_{tot} total power dissipation have been updated.			
74ALVC74 v.4	20170816	Product data sheet	-	74ALVC74 v.3
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate.			
74ALVC74 v.3	20030526	Product specification	-	74ALVC74 v.2
74ALVC74 v.2	20030124	Product specification	-	74ALVC74 v.1
74ALVC74 v.1	20021115	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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