74AHC2G126; 74AHCT2G126

Dual buffer/line driver; 3-state

Rev. 9 — 1 September 2023 Product data sheet

1. General description

The 74AHC2G126; 74AHCT2G126 is a dual buffer/line driver with 3-state outputs controlled by the output enable inputs (nOE). Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

2. Features and benefits

- Symmetrical output impedance
- Wide supply voltage range from 2.0 to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- Input levels:
  - For 74AHC2G126: CMOS level
  - For 74AHCT2G126: TTL level
- High noise immunity
- CMOS low power dissipation
- Balanced propagation delays
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC2G126DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74AHC2G126DC 74AHCT2G126DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

4. Marking

Table 2. Marking codes

Type number	Marking[1]
74AHC2G126DP	A26
74AHC2G126DC	A26
74AHCT2G126DC	C26

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

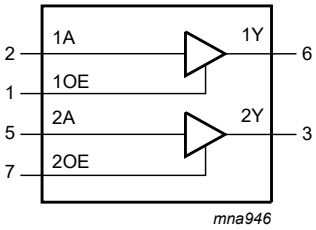


Fig. 1. Logic symbol

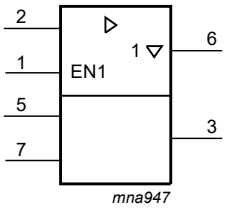


Fig. 2. IEC logic symbol

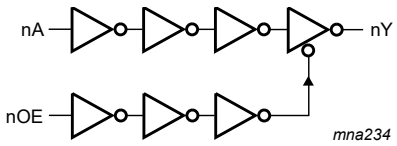
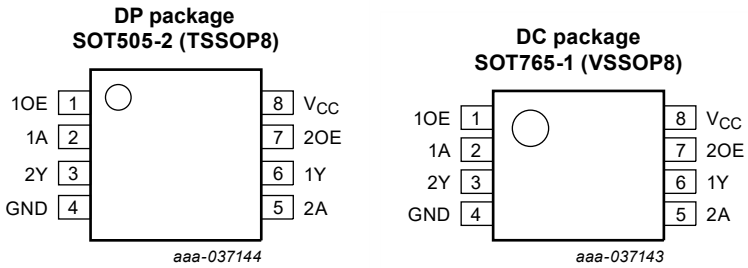


Fig. 3. Logic diagram (one buffer)

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 7	output enable input (active HIGH)
1A, 2A	2, 5	data input
GND	4	ground (0 V)
1Y, 2Y	6, 3	data output
V_{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	**nA**	**nY**
H	L	L
H	H	H
L	X	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
V_I	input voltage			-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V	[1]	-20	-	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	[1]	-	±20	mA
I_O	output current	-0.5 V < V_O < V_{CC} + 0.5 V		-	±25	mA
I_{CC}	supply current			-	75	mA
I_{GND}	ground current			-75	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C.
For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC2G126			74AHCT2G126			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V_{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC2G126										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -50 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -50 µA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I_O = -50 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_O = -8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I_{OZ}	OFF-state output current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	0.25	-	2.5	-	10	µA
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
C_I	input capacitance		-	1.5	10	-	10	-	10	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHCT2G126										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I_{OZ}	OFF-state output current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	0.25	-	2.5	-	10	µA
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
ΔI_{CC}	additional supply current	per input pin; V_I = 3.4 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	1.5	10	-	10	-	10	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

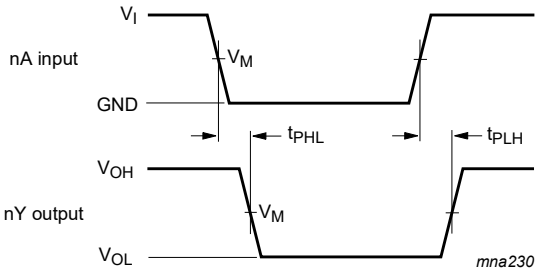
GND = 0 V; for test circuit see Fig. 6.

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
74AHC2G126											
t_{pd}	propagation delay	nA to nY; see Fig. 4	[1]								
		V_{CC} = 3.0 V to 3.6 V	[2]								
		C_L = 15 pF		-	4.7	8.0	1.0	9.5	1.0	11.5	ns
		C_L = 50 pF		-	6.6	11.5	1.0	13.0	1.0	14.5	ns
		V_{CC} = 4.5 V to 5.5 V	[3]								
		C_L = 15 pF		-	3.4	5.5	1.0	6.5	1.0	7.0	ns
		C_L = 50 pF		-	4.8	7.5	1.0	8.5	1.0	9.5	ns
t_{en}	enable time	nOE to nY; see Fig. 5	[1]								
		V_{CC} = 3.0 V to 3.6 V	[2]								
		C_L = 15 pF		-	5.0	8.0	1.0	9.5	1.0	11.5	ns
		C_L = 50 pF		-	6.9	11.5	1.0	13.0	1.0	14.5	ns
		V_{CC} = 4.5 V to 5.5 V	[3]								
		C_L = 15 pF		-	3.6	5.1	1.0	6.0	1.0	6.5	ns
		C_L = 50 pF		-	4.9	7.5	1.0	9.0	1.0	9.5	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{dis}	disable time	nOE to nY; see Fig. 5 [1]								
		V_{CC} = 3.0 V to 3.6 V [2]								
		C_L = 15 pF	-	6.0	9.7	1.0	11.5	1.0	12.5	ns
		C_L = 50 pF	-	8.3	13.2	1.0	15.0	1.0	16.5	ns
		V_{CC} = 4.5 V to 5.5 V [3]								
		C_L = 15 pF	-	4.1	6.8	1.0	8.0	1.0	8.5	ns
		C_L = 50 pF	-	5.7	8.8	1.0	10.0	1.0	11.0	ns
C_{PD}	power dissipation capacitance	per buffer; C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC} [4]	-	10	-	-	-	-	-	pF
74AHCT2G126										
t_{pd}	propagation delay	nA to nY; see Fig. 4 [1]								
		V_{CC} = 4.5 V to 5.5 V [3]								
		C_L = 15 pF	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
		C_L = 50 pF	-	4.8	7.5	1.0	8.5	1.0	9.5	ns
t_{en}	enable time	nOE to nY; see Fig. 5 [1]								
		V_{CC} = 4.5 V to 5.5 V [3]								
		C_L = 15 pF	-	3.9	5.1	1.0	6.0	1.0	6.5	ns
		C_L = 50 pF	-	5.1	7.5	1.0	9.0	1.0	9.5	ns
t_{dis}	disable time	nOE to nY; see Fig. 5 [1]								
		V_{CC} = 4.5 V to 5.5 V [3]								
		C_L = 15 pF	-	4.5	6.8	1.0	8.0	1.0	8.5	ns
		C_L = 50 pF	-	6.1	8.8	1.0	10.0	1.0	11.0	ns
C_{PD}	power dissipation capacitance	per buffer; C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC} [4]	-	10	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[2] Typical values are measured at V_{CC} = 3.3 V.
[3] Typical values are measured at V_{CC} = 5.0 V.
[4] C_{PD} is used to determine the dynamic power dissipation P_D (µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts.

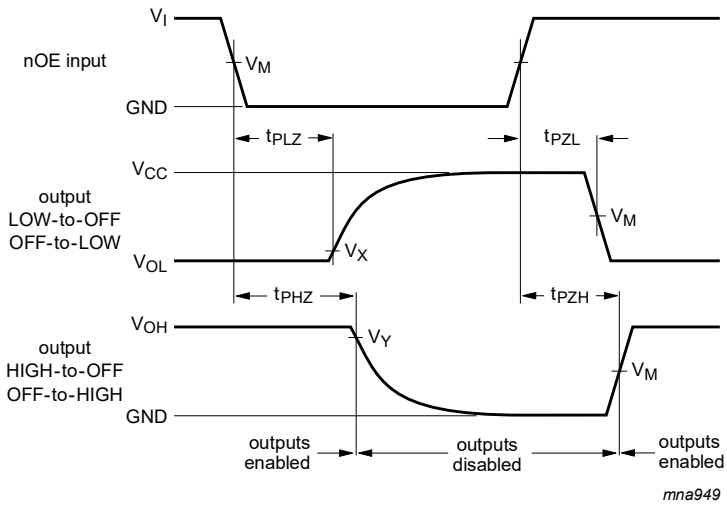
11.1. Waveforms and test circuit



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. Input (nA) to output (nY) propagation delays



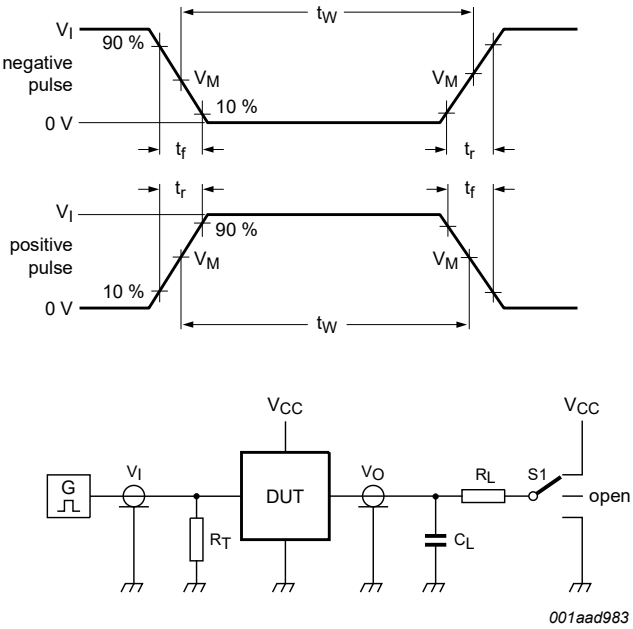
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Enable and disable times

Table 9. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74AHC2G126	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V
74AHCT2G126	1.5 V	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

S1 = Test selection switch.

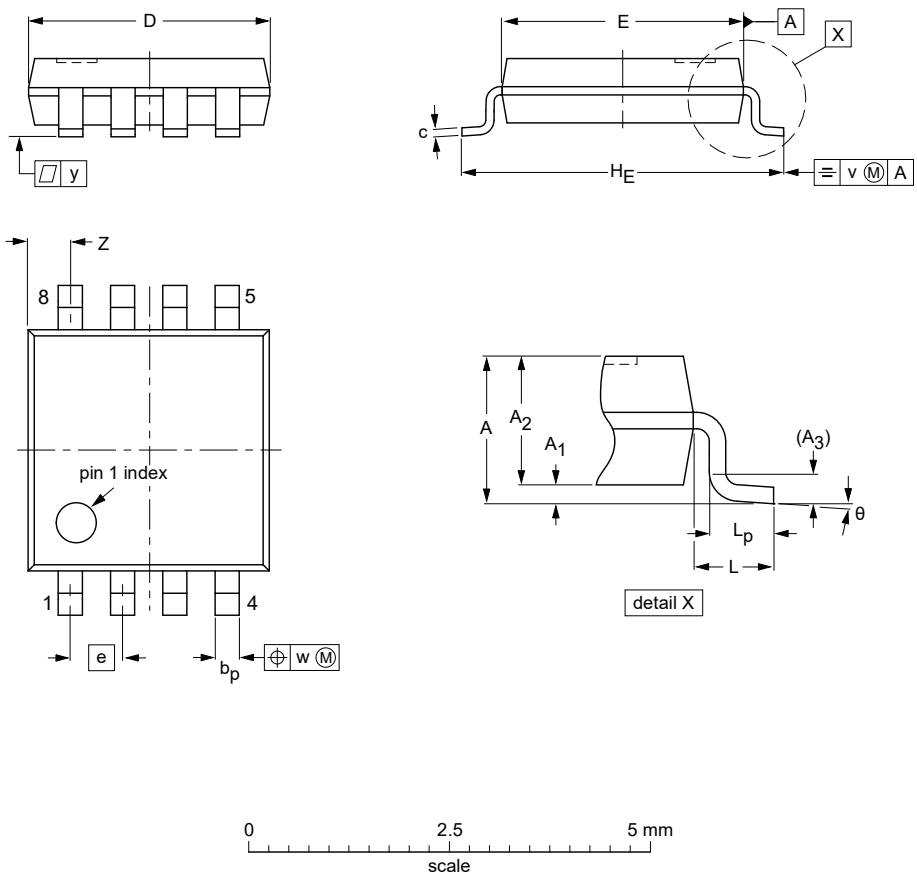
Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC2G126	V_{CC}	≤ 3 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74AHCT2G126	3 V	≤ 3 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

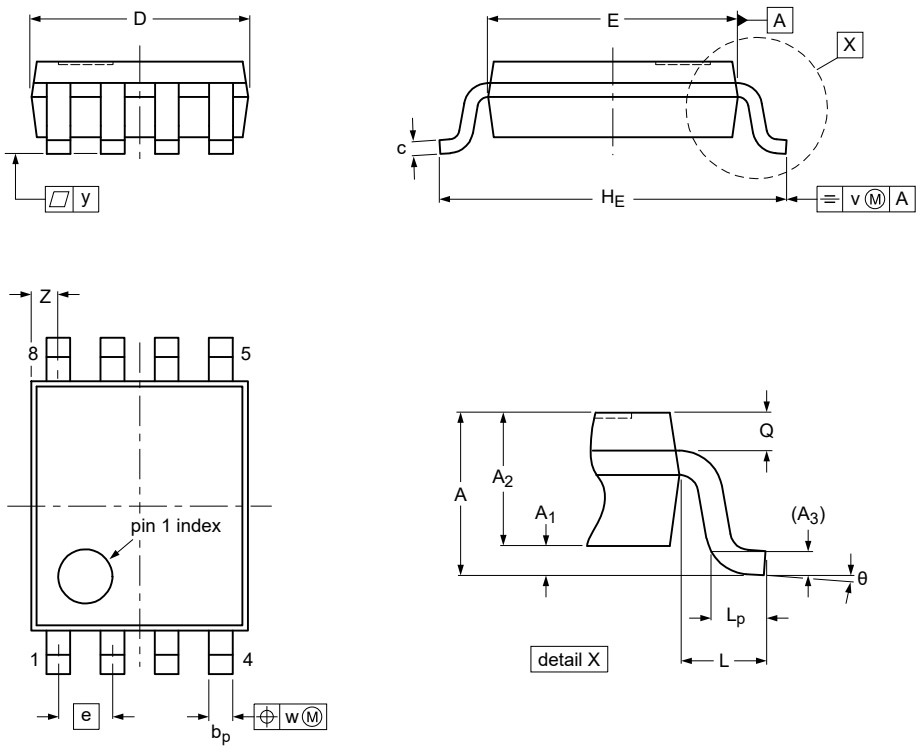
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig. 7. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit		A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	max	1	0.15	0.85	0.12	0.27	0.23	2.1	2.4	0.5	3.2	0.4	0.40	0.21	0.2	0.08	0.1	0.4	8°
	nom																		
	min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig. 8. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT2G126 v.9	20230901	Product data sheet	-	74AHC_AHCT2G126 v.8
Modifications:	• Section 1 and Section 2 updated. • Section 2: ESD specification updated according to the latest JEDEC standard. • Section 8: Derating values for P_{tot} total power dissipation updated.			
74AHC_AHCT2G126 v.8	20181119	Product data sheet	-	74AHC_AHCT2G126 v.7
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74AHCT2G126DP (SOT505-2/TSSOP8), 74AHC2G126GD and 74AHCT2G126GD (SOT996-2/XSON8) removed.			
74AHC_AHCT2G126 v.7	20130506	Product data sheet	-	74AHC_AHCT2G126 v.6
Modifications:	• For type number 74AHC2G126GD and 74AHCT2G126GD XSON8U has changed to XSON8.			
74AHC_AHCT2G126 v.6	20111108	Product data sheet	-	74AHC_AHCT2G126 v.5
Modifications:	• Legal pages updated.			
74AHC_AHCT2G126 v.5	20110324	Product data sheet	-	74AHC_AHCT2G126 v.4
74AHC_AHCT2G126 v.4	20090427	Product data sheet	-	74AHC_AHCT2G126 v.3
74AHC_AHCT2G126 v.3	20090115	Product data sheet	-	74AHC_AHCT2G126 v.2
74AHC_AHCT2G126 v.2	20040921	Product data sheet	-	74AHC_AHCT2G126 v.1
74AHC_AHCT2G126 v.1	20040113	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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