



PUSB3FR4

ESD protection for ultra high-speed interfaces

12 July 2018

Product data sheet

1. General description

The device is designed to protect high-speed interfaces such as SuperSpeed USB 3.2 at 10 Gbps, High-Definition Multimedia Interface (HDMI), DisplayPort, external Serial Advanced Technology Attachment (eSATA) and Low Voltage Differential Signaling (LVDS) interfaces against ElectroStatic Discharge (ESD).

The device includes four high-level ESD protection diode structures. They protect sensitive transmitters and receivers for ultra high-speed signal lines. The device is encapsulated in a leadless small DFN2510A-10 (SOT1176-1) plastic package.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of only 0.29 pF. These diodes utilize a snap-back structure in order to provide protection to downstream components from ESD voltages up to ± 15 kV contact exceeding IEC 61000-4-2, level 4.

2. Features and benefits

- System-level ESD protection for USB 2.0 and SuperSpeed USB 3.2 at 10 Gbps, HDMI, DisplayPort, eSATA and LVDS
- Line capacitance of only 0.29 pF for each channel
- Outstanding system protection: extremely deep snap-back combined with dynamic resistance of only 0.27 Ω
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ± 15 kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Design-friendly 'pass-through' signal routing

3. Applications

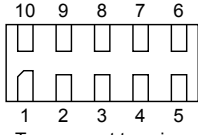
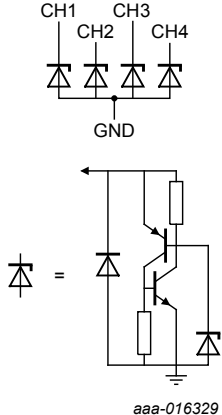
The device is designed for high-speed receiver and transmitter port protection:

- Smartphones, tablet computers, Mobile Internet Devices (MID) and portable devices
- TVs and monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles

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4. Pinning information

Table 1. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|--------------------------|---|---|
| 1 | CH1 | channel 1 ESD protection |  <p>Transparent top view</p> <p>DFN2510A-10 (SOT1176-1)</p> |  <p>aaa-016329</p> |
| 2 | CH2 | channel 2 ESD protection | | |
| 3 | GND | ground | | |
| 4 | CH3 | channel 3 ESD protection | | |
| 5 | CH4 | channel 4 ESD protection | | |
| 6 | n.c. | not connected | | |
| 7 | n.c. | no connection | | |
| 8 | GND | ground | | |
| 9 | n.c. | not connected | | |
| 10 | n.c. | not connected | | |

5. Ordering information

Table 2. Ordering information

| Type number | Package | | |
|-------------|-------------|---|-----------|
| | Name | Description | Version |
| PUSB3FR4 | DFN2510A-10 | plastic, leadless extremely thin small outline package; 10 terminals; 0.5 mm pitch; 2.5 mm x 1 mm x 0.5 mm body | SOT1176-1 |

6. Marking

Table 3. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PUSB3FR4 | FR |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-----------|---------------------------------|---|-----|------|-----|------|
| V_I | input voltage | | | -0.5 | 3.3 | V |
| I_{PPM} | rated peak pulse current | $t_p = 8/20 \mu s$ | | - | 7 | A |
| V_{ESD} | electrostatic discharge voltage | IEC 61000-4-2, level 4; contact discharge | [1] | -15 | 15 | kV |
| | | IEC 61000-4-2, level 4; air discharge | [1] | -15 | 15 | kV |
| T_{stg} | storage temperature | | | -55 | 125 | °C |
| T_{amb} | ambient temperature | | | -40 | 85 | °C |

[1] All pins to ground.

8. Characteristics

Table 5. Characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-------------------|-----------------------------|---|-----|-----|------|------|----------|
| V_{BR} | breakdown voltage | $I_I = 1 \text{ mA}$; $T_{amb} = 25 \text{ °C}$ | | 5.5 | 9 | - | V |
| I_{LR} | reverse leakage current | per channel; $V_I = 1.5 \text{ V}$; $T_{amb} = 25 \text{ °C}$ | | - | 1 | 100 | nA |
| V_F | forward voltage | $I_I = 1 \text{ mA}$; $T_{amb} = 25 \text{ °C}$ | | - | 0.7 | - | V |
| C_{line} | line capacitance | $f = 1 \text{ MHz}$; $V_I = 1.5 \text{ V}$; $T_{amb} = 25 \text{ °C}$ | [1] | - | 0.29 | 0.34 | pF |
| ΔC_{line} | line capacitance difference | $f = 1 \text{ MHz}$; $V_I = 1.5 \text{ V}$; $T_{amb} = 25 \text{ °C}$ | [1] | - | 0.02 | 0.05 | pF |
| r_{dyn} | dynamic resistance | TLP; positive transient; $T_{amb} = 25 \text{ °C}$ | [2] | - | 0.27 | - | Ω |
| | | TLP; negative transient; ; $T_{amb} = 25 \text{ °C}$ | [2] | - | 0.27 | - | Ω |
| V_{sbck} | snapback voltage | $I_I = 1 \text{ A}$; TLP 10/100 ns; $T_{amb} = 25 \text{ °C}$ | | - | 1.5 | - | V |
| V_{CL} | clamping voltage | $I_{PP} = 5 \text{ A}$; positive transient; $T_{amb} = 25 \text{ °C}$ | [3] | - | 3 | - | V |
| | | $I_{PP} = -5 \text{ A}$; negative transient; $T_{amb} = 25 \text{ °C}$ | [3] | - | -3 | - | V |

[1] The parameter is guaranteed by design.

[2] 100 ns Transmission Line Pulse (TLP), 50 Ω , pulser at 80 ns.

[3] According to IEC 61000-4-5 (8/20 μs current waveform).

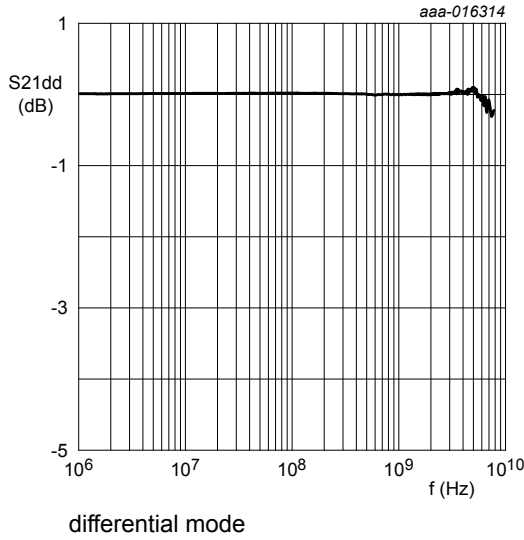
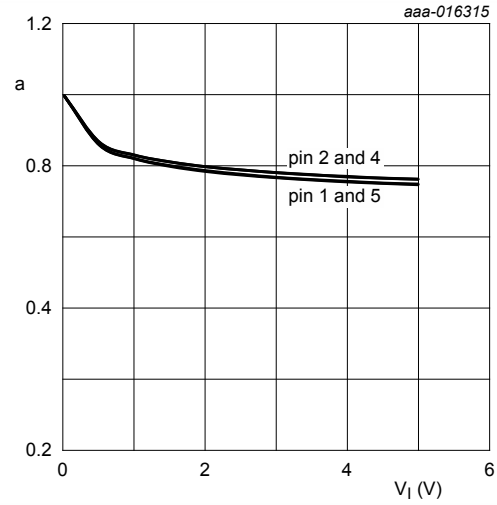
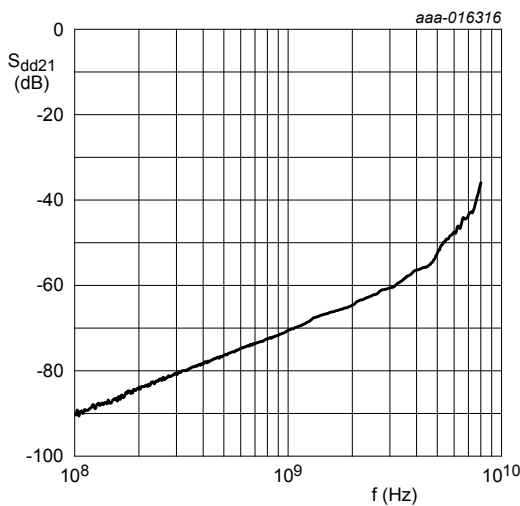


Fig. 1. Insertion loss; typical values



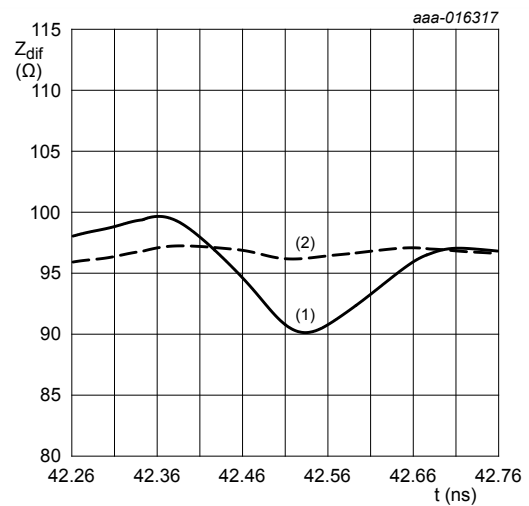
$$a = \frac{C_{line}}{C_{line}(V_I = 0 V)}$$

Fig. 2. Relative capacitance as a function of input voltage; typical values



Sdd21 normalized to 100 Ω;
differential pairs CH1/CH2 versus CH3/CH4

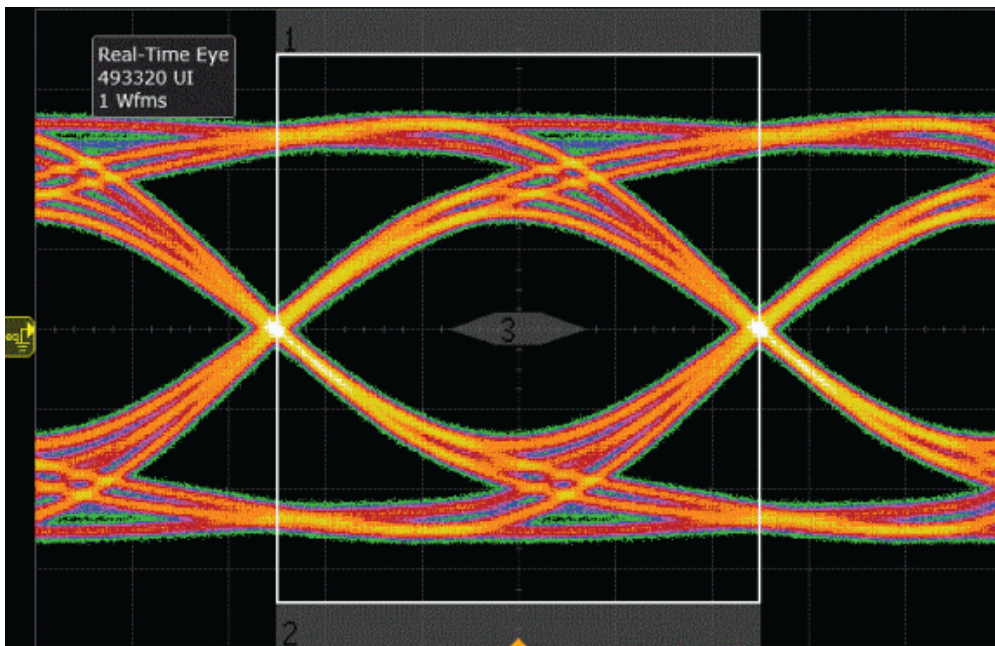
Fig. 3. Mixed-mode differential NEXT crosstalk; typical values



$t_r = 200$ ps; differential pair CH1 + CH2

(1) Device on reference board
(2) Reference board without Device Under Test (DUT)

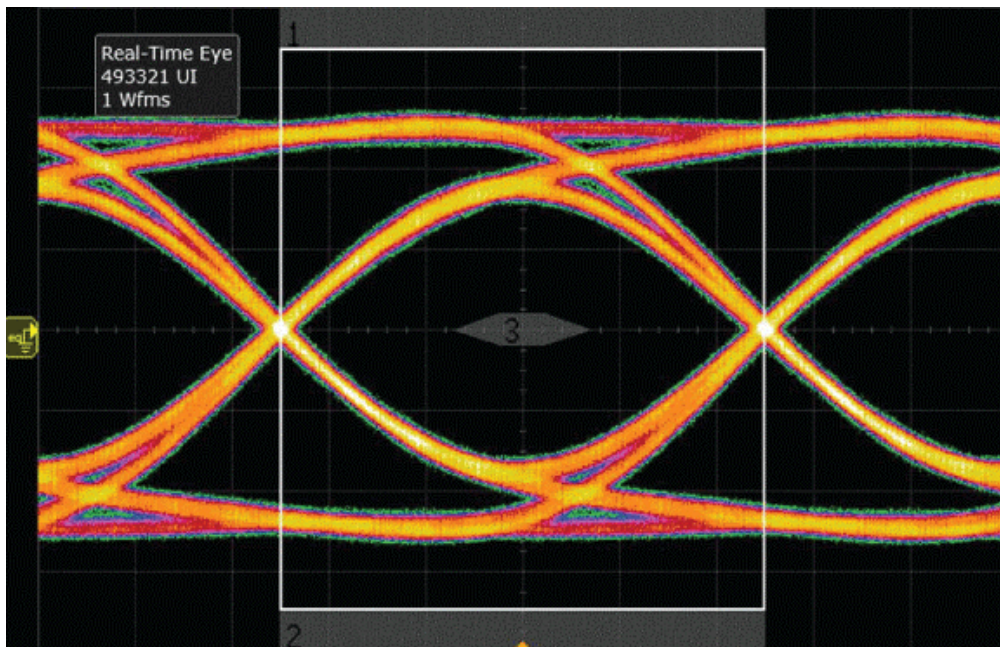
Fig. 4. Differential Time Domain Reflectometer (TDR) plot; typical values



aaa-016318

Data rate: 10 Gbit/s
 Vertical scale: 175 mV/div
 Horizontal scale: 20 ps/div

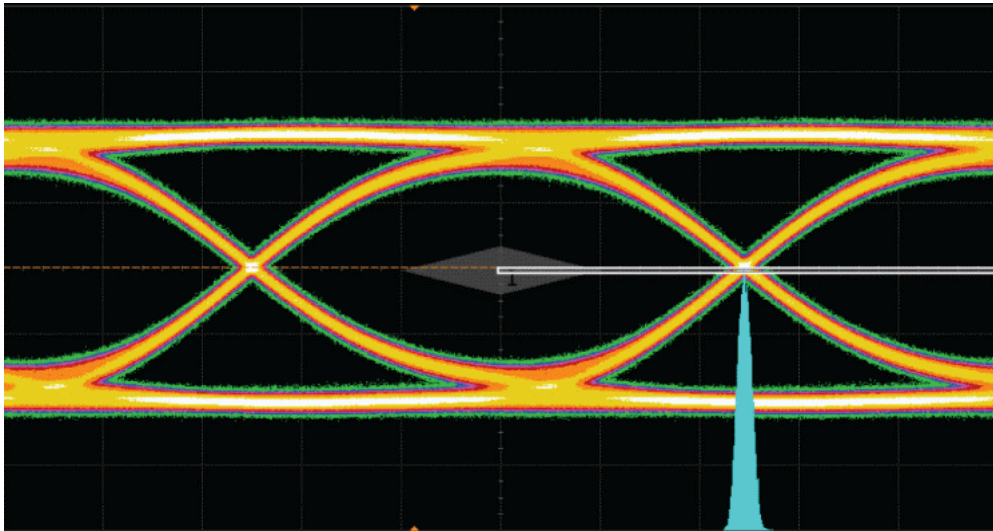
Fig. 5. USB 3.2 eye diagram, PCB with device



aaa-016319

Data rate: 10 Gbit/s
 Vertical scale: 175 mV/div
 Horizontal scale: 20 ps/div

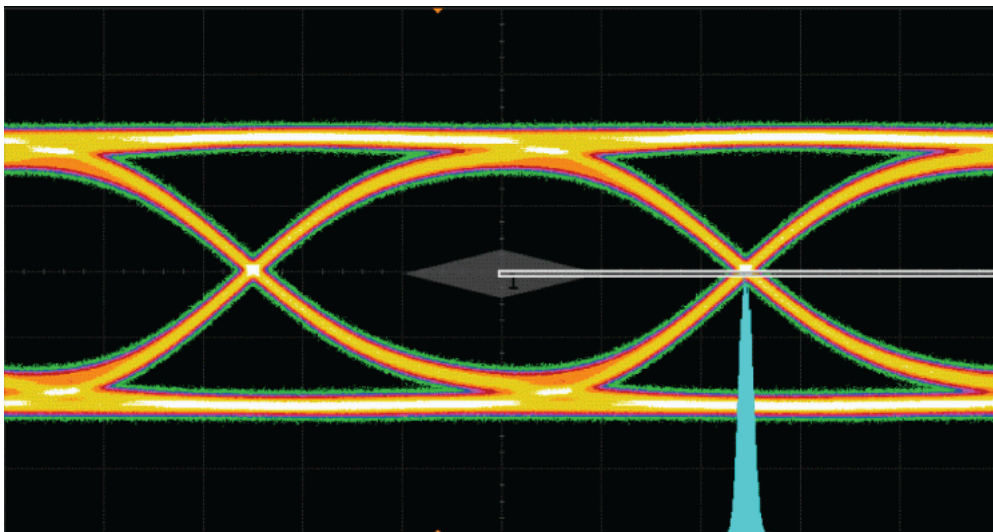
Fig. 6. USB 3.2 eye diagram, PCB without device



aaa-016320

Test frequency: 148.5 MHz
 Differential swing voltage: 812 mV
 Horizontal scale: 34 ps/div

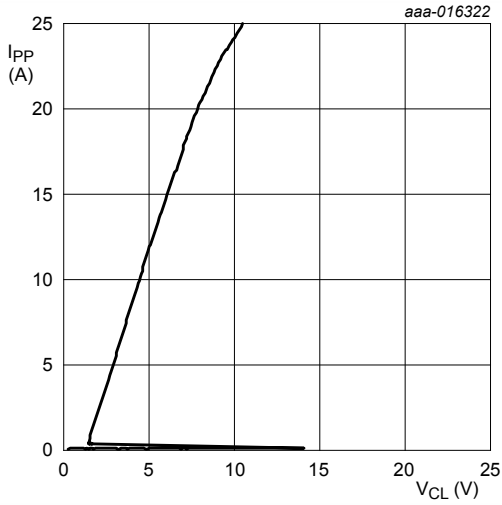
Fig. 7. HDMI 2.0 TP1 eye diagram, PCB with device



aaa-016321

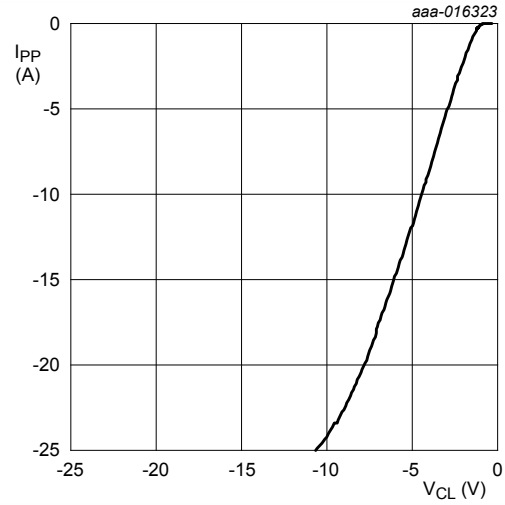
Test frequency: 148.5 MHz
 Differential swing voltage: 812 mV
 Horizontal scale: 34 ps/div

Fig. 8. HDMI 2.0 TP1 eye diagram, PCB without device



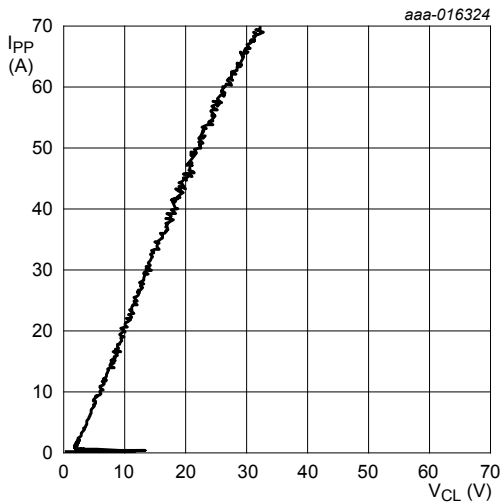
$t_p = 100 \text{ ns}$; Transmission Line Pulse (TLP);
 $t_r = 1 \text{ ns}$

Fig. 9. Dynamic resistance with positive clamping; typical values



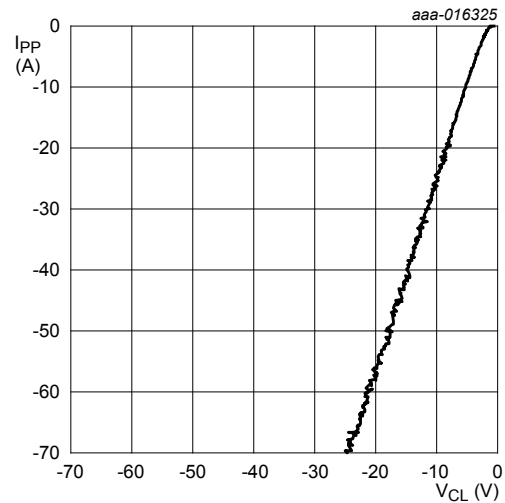
$t_p = 100 \text{ ns}$; Transmission Line Pulse (TLP);
 $t_r = 1 \text{ ns}$

Fig. 10. Dynamic resistance with negative clamping; typical values



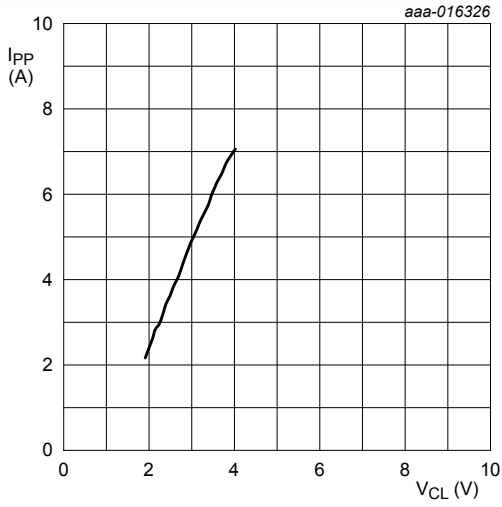
$t_p = 5 \text{ ns}$; Transmission Line Pulse (TLP);
 $t_r = 600 \text{ ps}$

Fig. 11. Dynamic resistance with positive clamping; typical values



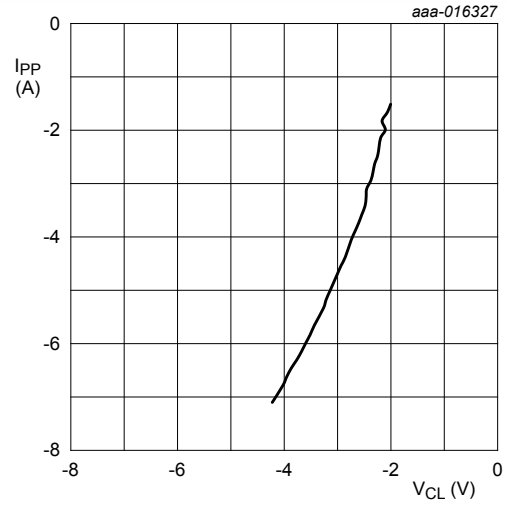
$t_p = 5 \text{ ns}$; Transmission Line Pulse (TLP);
 $t_r = 600 \text{ ps}$

Fig. 12. Dynamic resistance with negative clamping; typical values



IEC 61000-4-5; $t_p = 8/20 \mu s$; positive pulse

Fig. 13. Dynamic resistance with positive clamping; typical values



IEC 61000-4-5; $t_p = 8/20 \mu s$; negative pulse

Fig. 14. Dynamic resistance with negative clamping; typical values

9. Application information

The device is designed to provide high-level ESD protection for high-speed serial data buses such as HDMI, DisplayPort, eSATA and LVDS data lines.



Note: When designing the PCB, give careful consideration to impedance matching and signal coupling. Do not connect the signal lines to unlimited current sources like, for example, a battery.

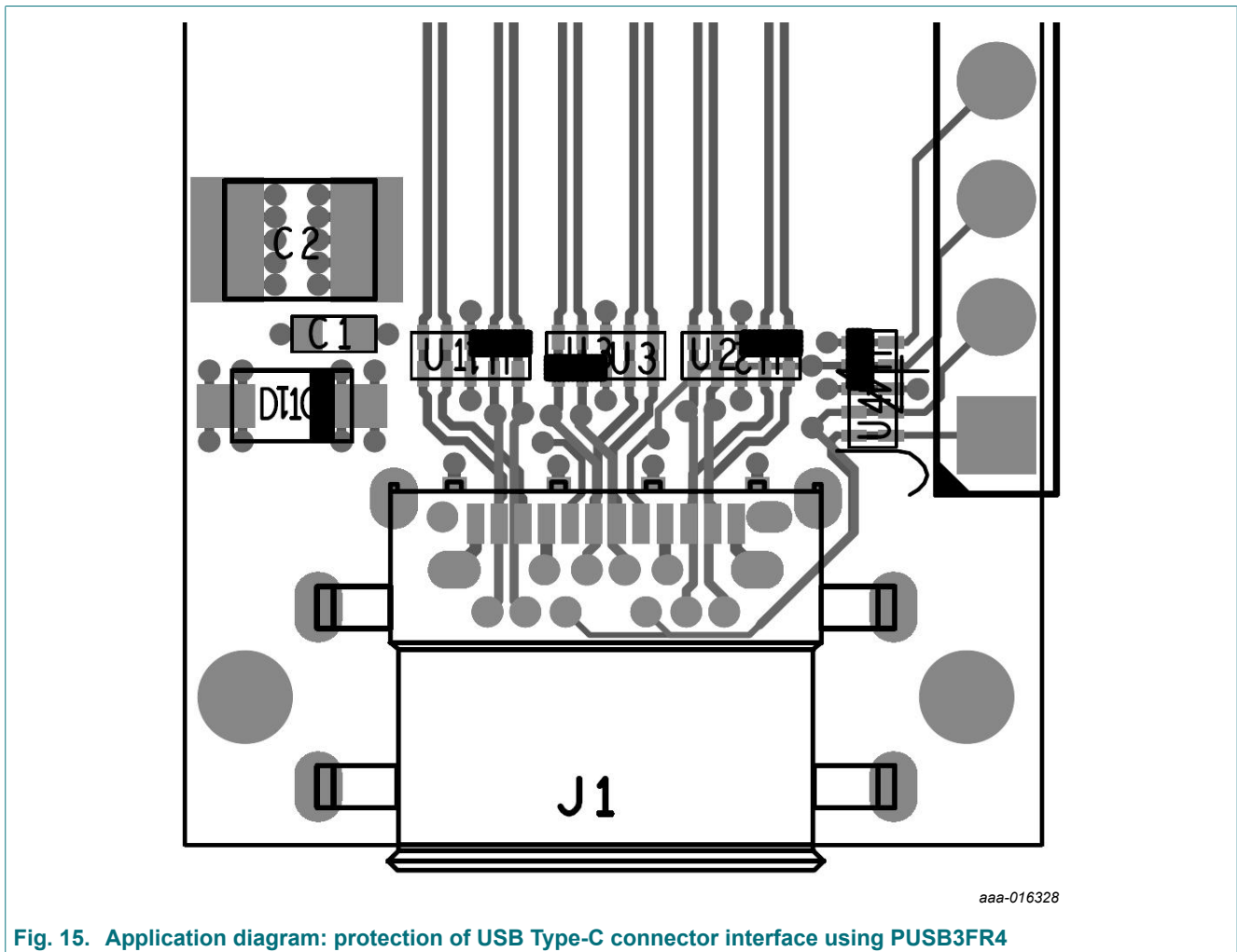


Fig. 15. Application diagram: protection of USB Type-C connector interface using PUSB3FR4

Dynamic resistance

The device uses an advanced clamping structure showing a negative dynamic resistance.

This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

10. Package outline

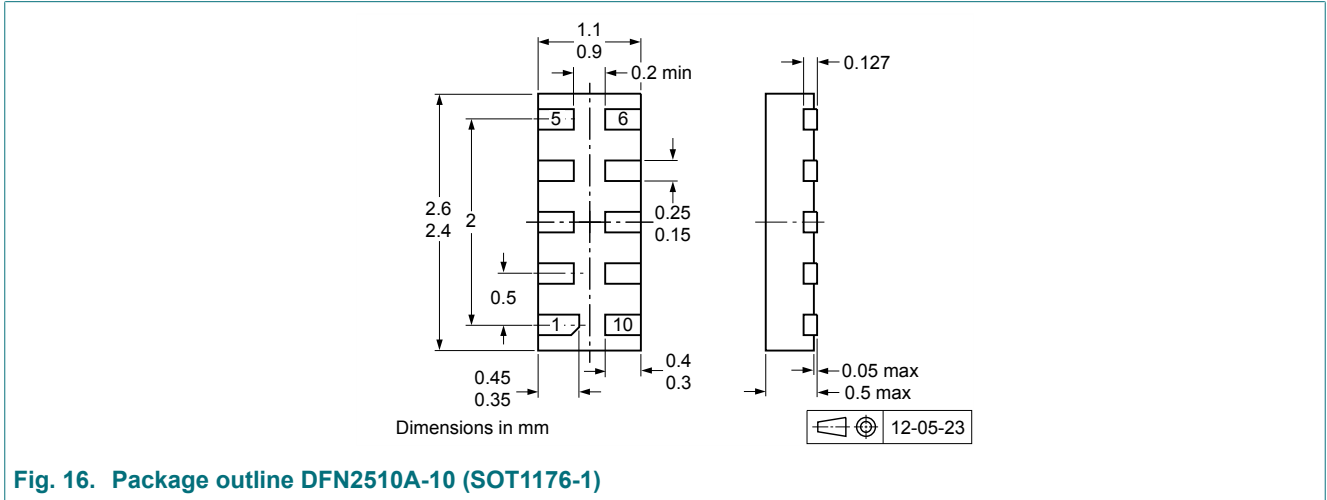


Fig. 16. Package outline DFN2510A-10 (SOT1176-1)

11. Soldering

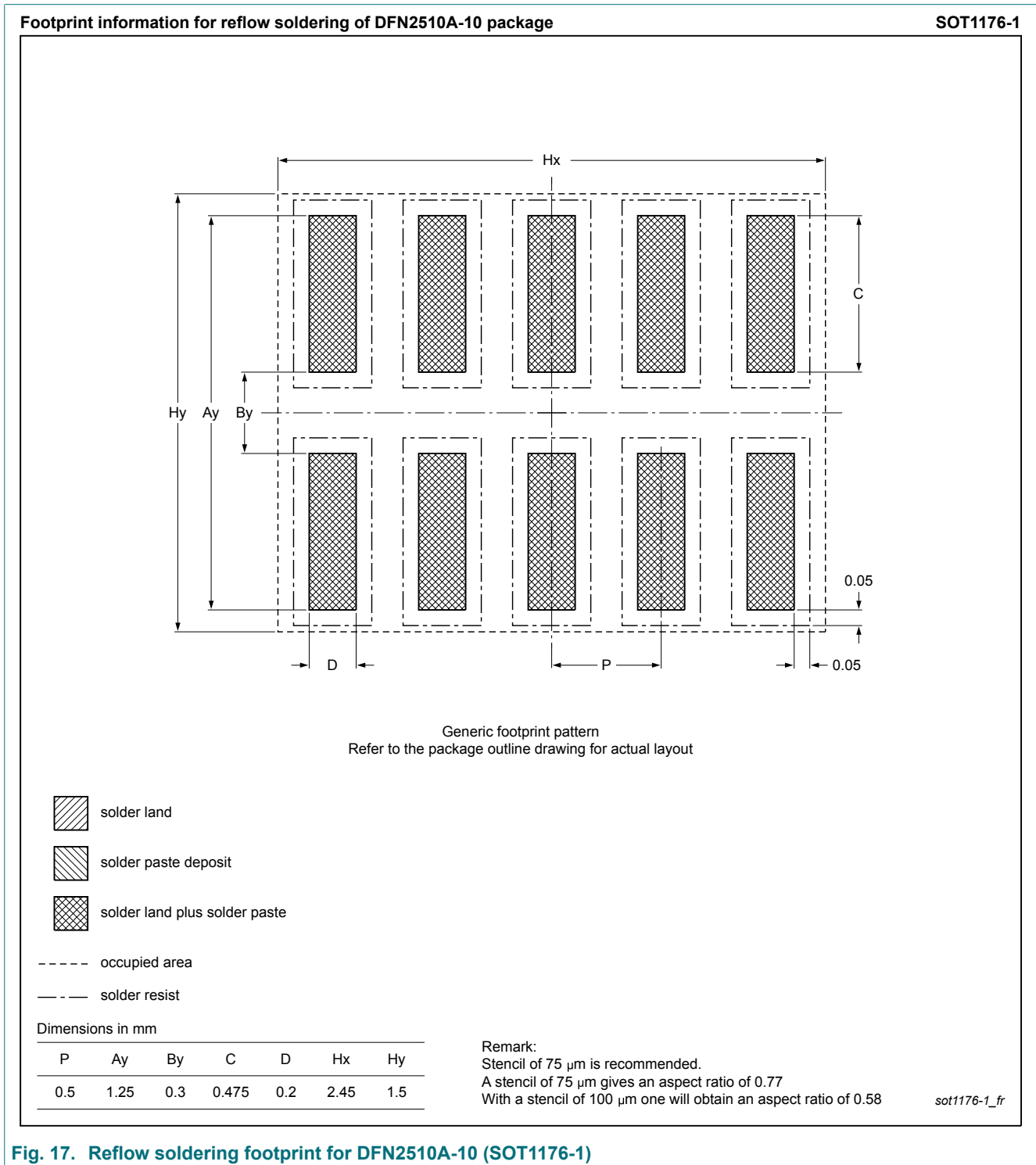


Fig. 17. Reflow soldering footprint for DFN2510A-10 (SOT1176-1)

12. Revision history

Table 6. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|--------------------|---------------|--------------|
| PUSB3FR4 v.2 | 20180711 | Product data sheet | - | PUSB3FR4 v.1 |
| Modifications: | <ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.• Legal texts have been adapted to the new company name where appropriate.• Conditions clarified to reflect the used standard• Figures 9 to 12 were updated | | | |
| PUSB3FR4 v.1 | 20150126 | Product data sheet | - | - |

13. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 12 July 2018

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