



# PDTA115EU

PNP resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$

5 March 2024

Product data sheet

## 1. General description

PNP Resistor-Equipped Transistor (RET) in a very small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package.

NPN complement: PDTC115EU

## 2. Features and benefits

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

## 3. Applications

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	-50	V
I <sub>O</sub>	output current		-	-	-20	mA
R1	bias resistor 1 (input)	T <sub>amb</sub> = 25 °C	70	100	130	k $\Omega$
R2/R1	bias resistor ratio		0.8	1	1.2	

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 SC-70 (SOT323)	 sym003
2	G	GND (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTA115EU	SC-70	plastic, surface-mounted package; 3 leads; 1.3 mm pitch; 2 mm x 1.25 mm x 0.95 mm body	SOT323

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PDTA115EU	%7C

[1] % = placeholder for manufacturing site code

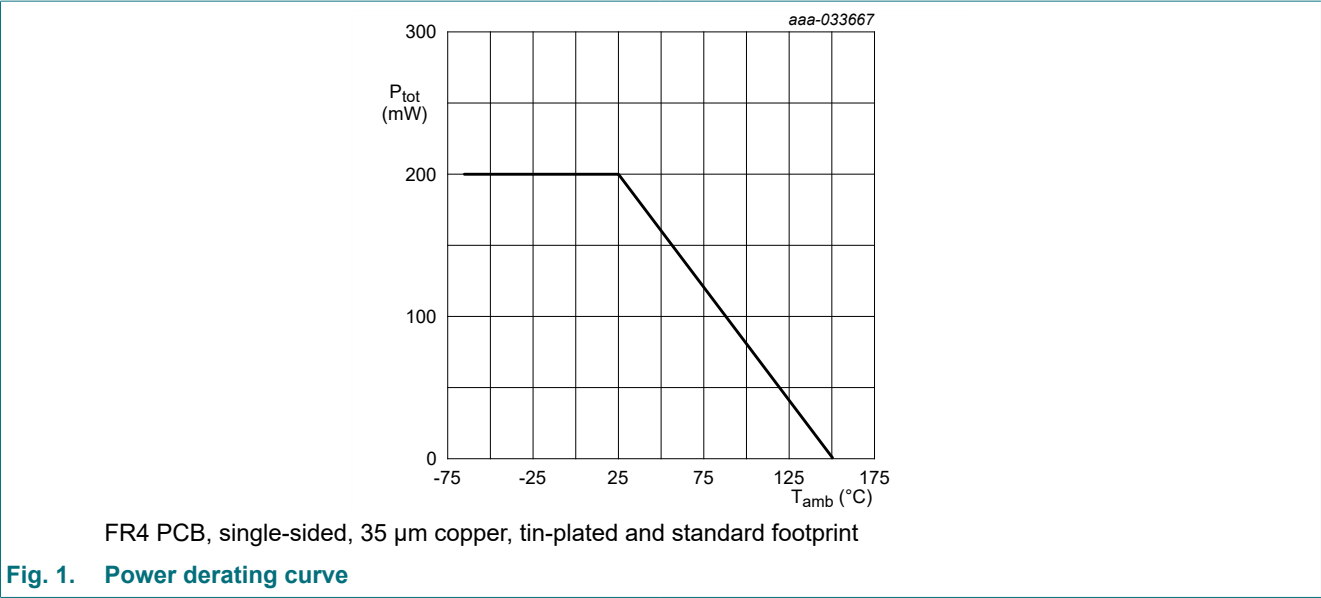
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CBO</sub>	collector-base voltage	open emitter		-	-50	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	-50	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	-10	V
V <sub>I</sub>	input voltage			-40	10	V
I <sub>O</sub>	output current			-	-20	mA
I <sub>CM</sub>	peak collector current			-	-100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	200	mW
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-65	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

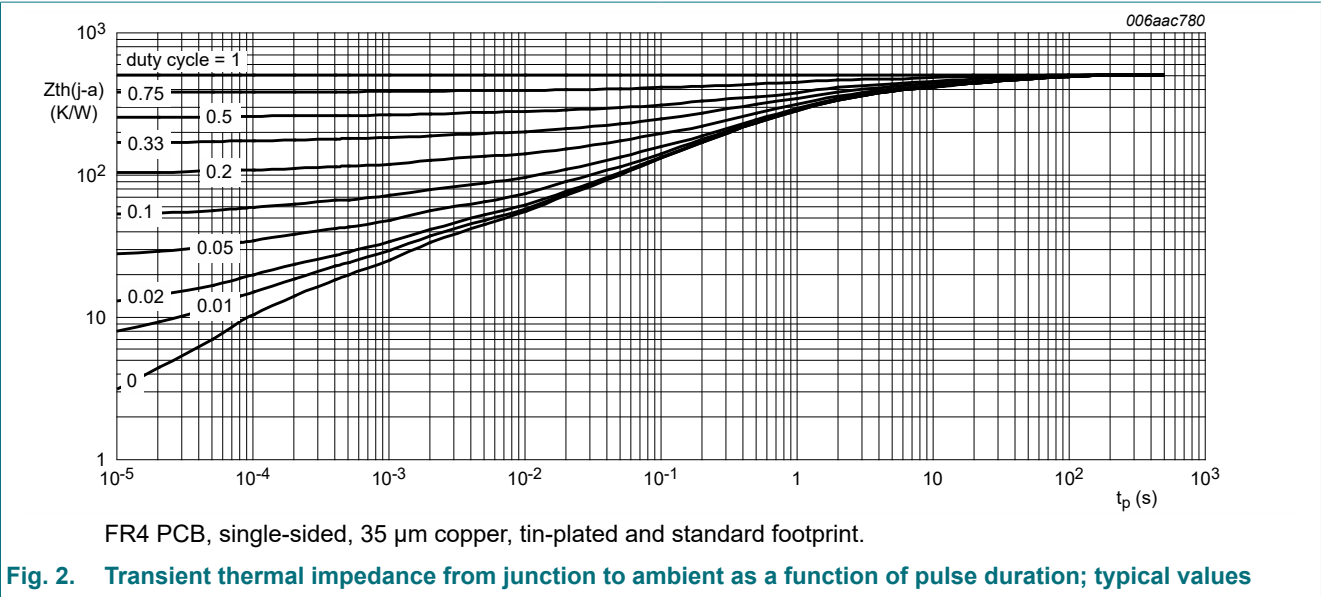


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25\text{ °C}$	[1]	-	-	625	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = -50 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	-100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	-100	nA
		V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	-5	μA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	-50	μA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -5 mA; T <sub>amb</sub> = 25 °C	80	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = -5 mA; I <sub>B</sub> = -0.25 mA; T <sub>amb</sub> = 25 °C	-	-	-150	mV
V <sub>I(off)</sub>	off-state input voltage	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -100 μA; T <sub>amb</sub> = 25 °C	-	-1.2	-0.5	V
V <sub>I(on)</sub>	on-state input voltage	V <sub>CE</sub> = -0.3 V; I <sub>C</sub> = -1 mA; T <sub>amb</sub> = 25 °C	-3	-1.6	-	V
R1	bias resistor 1 (input)	T <sub>amb</sub> = 25 °C	70	100	130	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = -10 V; I <sub>E</sub> = 0 A; i <sub>e</sub> = 0 A; f = 1 MHz; T <sub>amb</sub> = 25 °C	-	-	3	pF

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

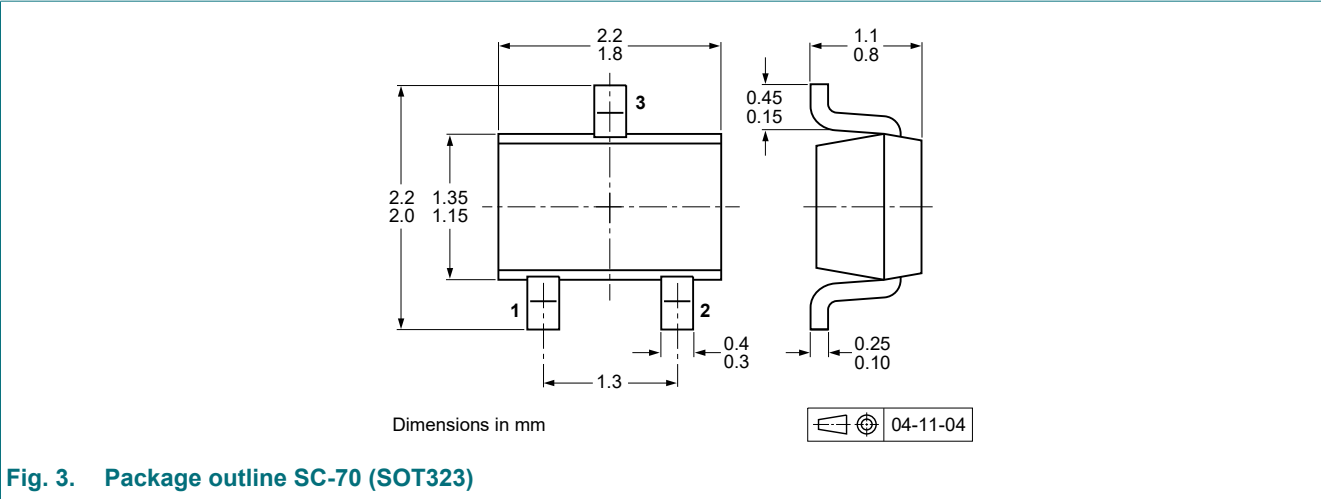


Fig. 3. Package outline SC-70 (SOT323)

13. Soldering

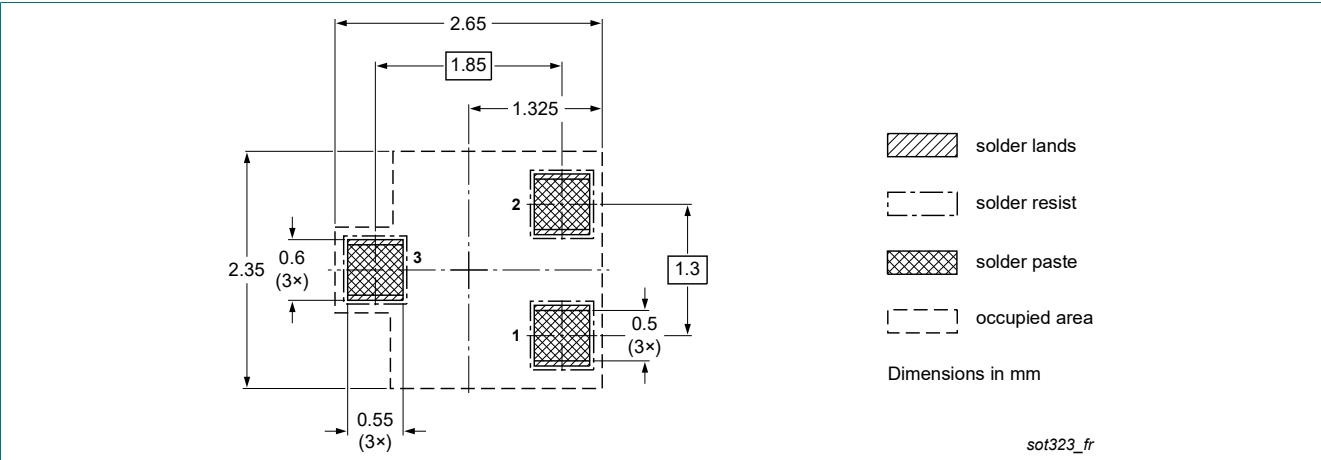


Fig. 4. Reflow soldering footprint for SC-70 (SOT323)

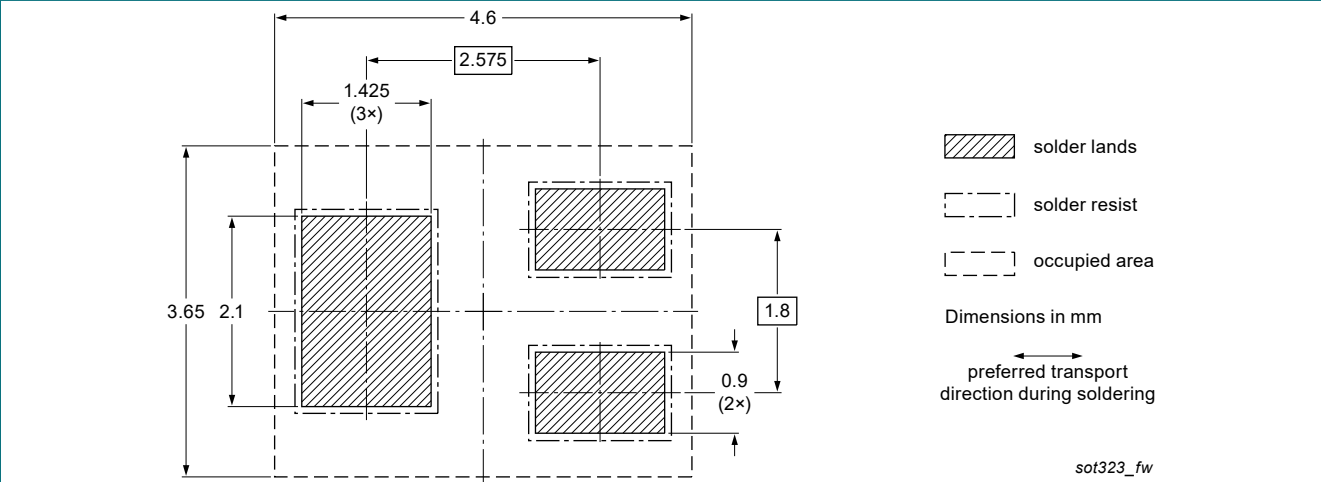


Fig. 5. Wave soldering footprint for SC-70 (SOT323)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTA115EU v.3	20240305	Product data sheet	-	PDTA115E series v.2
Modification:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li>Family data sheet reduced to single type data sheet.</li><li>Packing information removed.</li></ul>			
PDTA115E series v.2	20040730	Product data sheet	-	PDTA115E series v.1
PDTA115E series v.1	20040505	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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