

74HCT4538-Q100

Dual retriggerable precision monostable multivibrator

Rev. 5 — 26 March 2024

Product data sheet

1. General description

The 74HCT4538-Q100 is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has two trigger/retrigger inputs ($n\bar{A}$ and nB), a direct reset input ($n\bar{CD}$), two complementary outputs (nQ and $n\bar{Q}$), and two pins ($nREXT/CEXT$ and $nCEXT$) for connecting the external timing components C_{EXT} and R_{EXT} . Typical pulse width variation over temperature range is $\pm 0.2\%$. The device may be triggered by either the positive or the negative edges of the input pulse. The duration and accuracy of the output pulse are determined by the external timing components C_{EXT} and R_{EXT} . The output pulse width (T_W) is equal to $0.7 \times R_{EXT} \times C_{EXT}$. The linear design techniques guarantee precise control of the output pulse width. A LOW level at $n\bar{CD}$ terminates the output pulse immediately. Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Tolerant of slow trigger rise and fall times
- High noise immunity
- Separate reset inputs
- Triggering from falling or rising edge
- Complies with JEDEC standard no. 7A
- Wide supply voltage range from 4.5 to 5.5 V
- CMOS low power dissipation
- TTL input levels
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HCT4538D-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4538PW-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

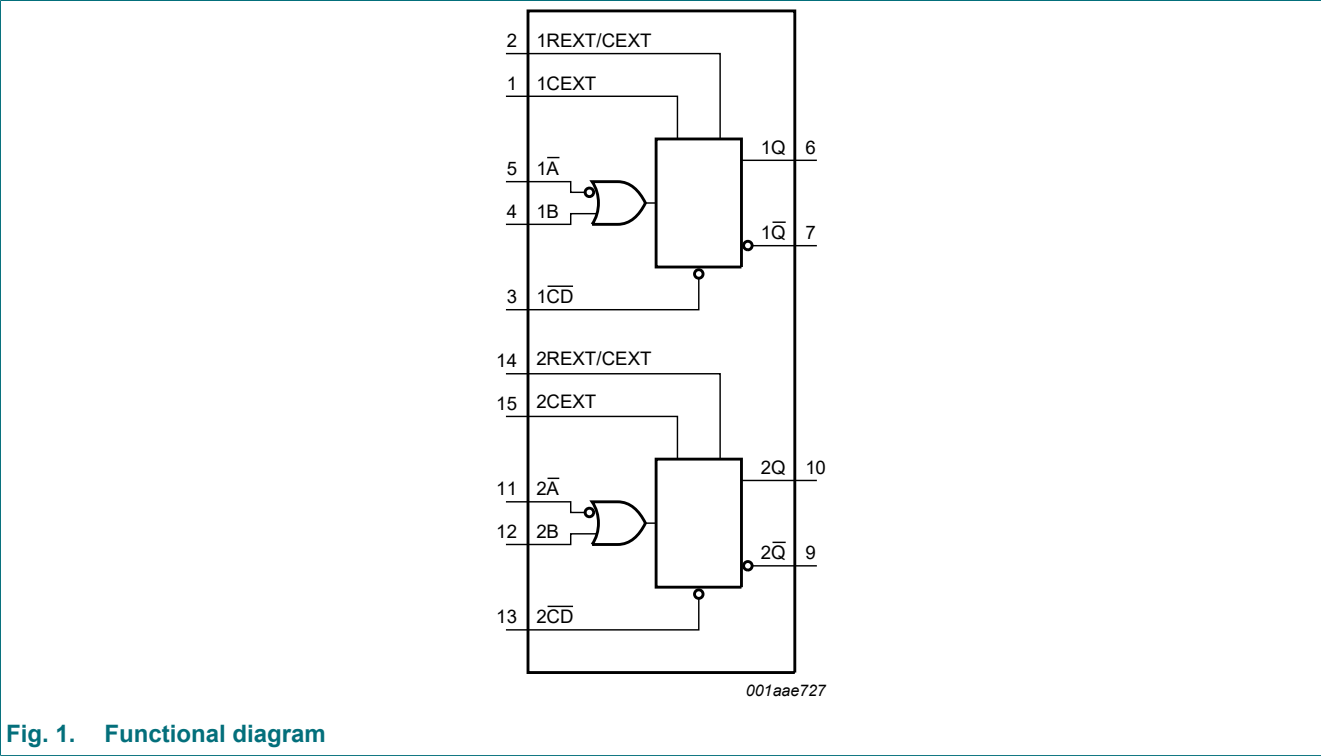


Fig. 1. Functional diagram

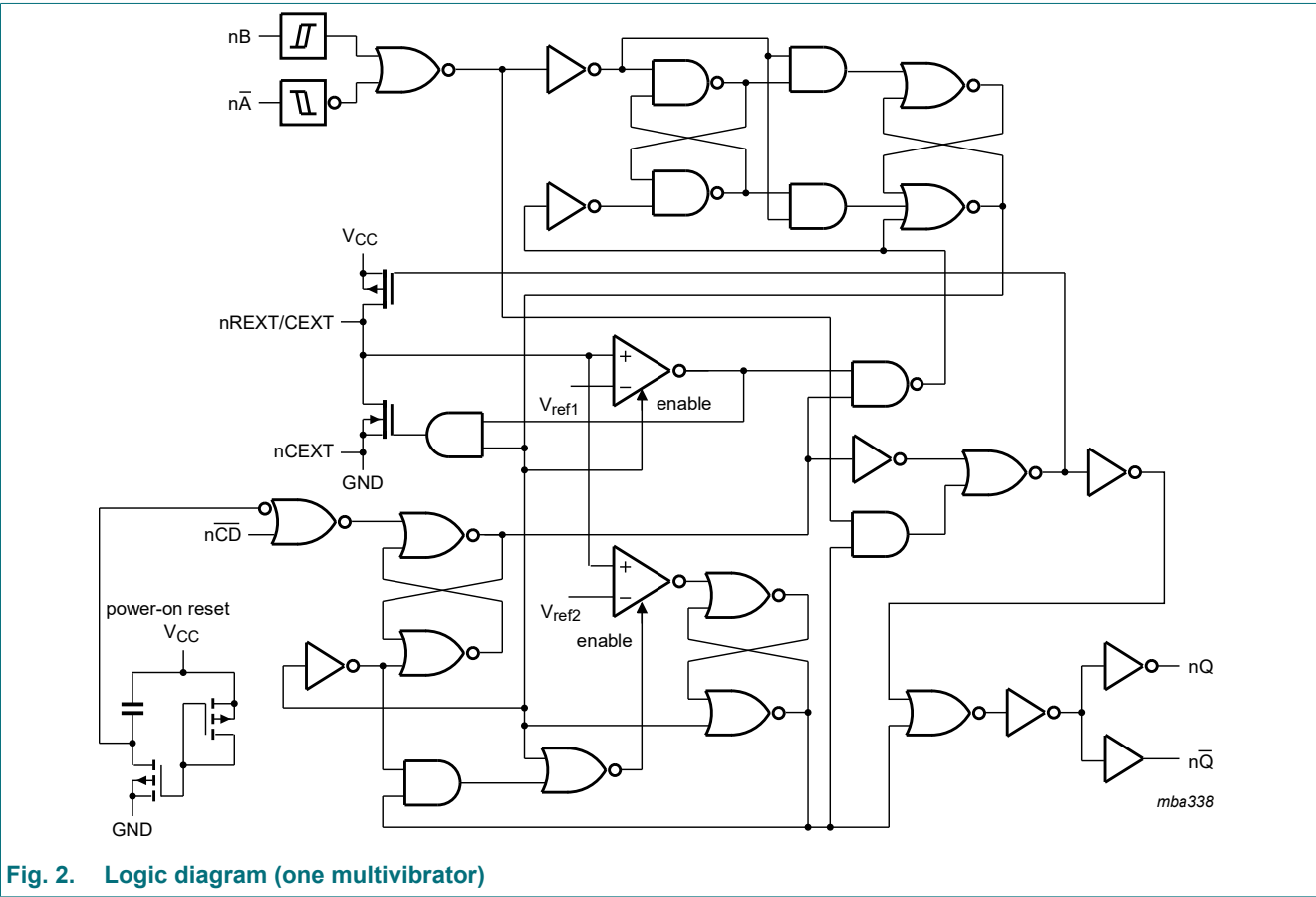


Fig. 2. Logic diagram (one multivibrator)

5. Pinning information

5.1. Pinning

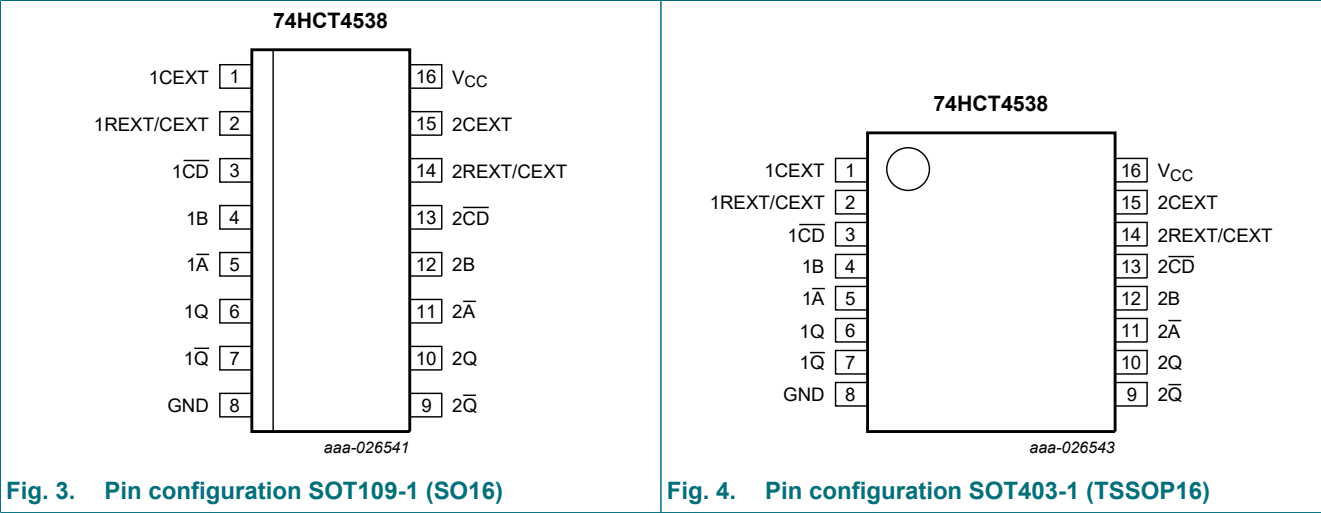


Fig. 3. Pin configuration SOT109-1 (SO16)

Fig. 4. Pin configuration SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1CEXT, 2CEXT	1, 15	external capacitor connection (always connected to ground)
1REXT/CEXT, 2REXT/CEXT	2, 14	external capacitor/resistor connection
1CD, 2CD	3, 13	direct reset input (active LOW)
1B, 2B	4, 12	input (LOW to HIGH triggered)
1A, 2A	5, 11	input (HIGH to LOW triggered)
1Q, 2Q	6, 10	output
1Q, 2Q	7, 9	complementary output (active LOW)
GND	8	ground (0 V)
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;
↑ = positive-going transition; ↓ = negative-going transition;
⌋ = one HIGH level output pulse, with the pulse width determined by C_{EXT} and R_{EXT};
⌋ = one LOW level output pulse, with the pulse width determined by C_{EXT} and R_{EXT}.

Inputs			Outputs	
nA	nB	nCD	nQ	nQ
↓	L	H	⌋	⌋
H	↑	H	⌋	⌋
X	X	L	L	H

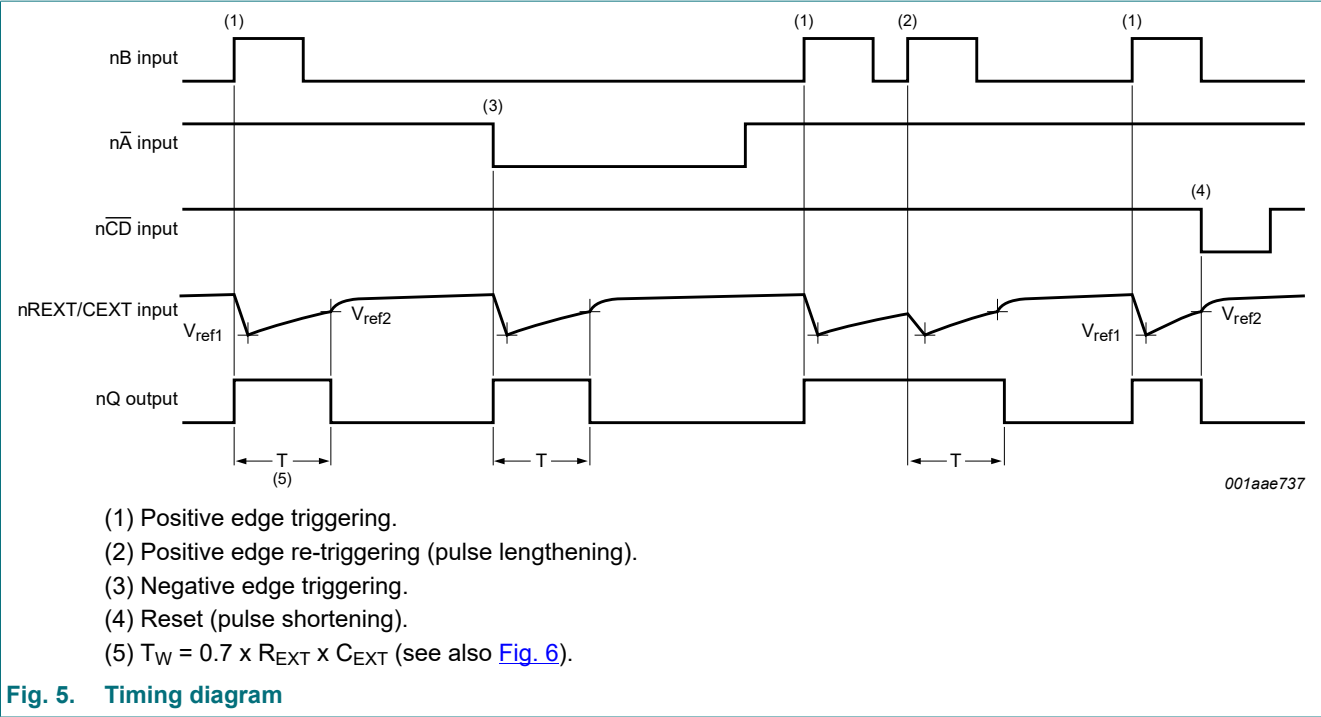


Fig. 5. Timing diagram

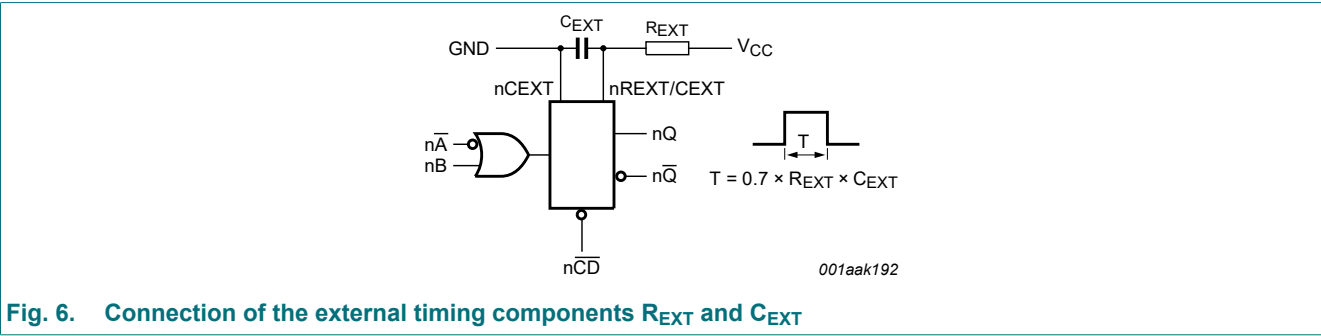


Fig. 6. Connection of the external timing components R_{EXT} and C_{EXT}

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	±20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 4.5 V	-	1.67	139	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	μA
		pin nREXT/CEXT; V _I = 2.0 V or GND; other inputs at V _{CC} or GND; V _{CC} = 5.5 V [1]	-	-	±0.5	-	±5	-	±10	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		pin nA, nB	-	50	180	-	225	-	245	μA
		pin nCD	-	65	234	-	293	-	319	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

[1] This measurement can only be carried out after a trigger pulse is applied.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	LOW to HIGH propagation delay	n $\overline{A}$, nB to nQ; see Fig. 7								
		V _{CC} = 4.5 V	-	35	60	-	75	-	90	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	30	-	-	-	-	-	ns
		n $\overline{CD}$ to n $\overline{Q}$; see Fig. 7								
t _{PHL}	HIGH to LOW propagation delay	n $\overline{A}$, nB to n $\overline{Q}$; see Fig. 7								
		V _{CC} = 4.5 V	-	35	60	-	75	-	90	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	30	-	-	-	-	-	ns
		n $\overline{CD}$ to nQ; see Fig. 7								
t _t	transition time	nQ and n $\overline{Q}$; see Fig. 7 [1]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	21	ns
t _W	pulse width	n $\overline{A}$ LOW; see Fig. 8								
		V _{CC} = 4.5 V	20	11	-	25	-	30	-	ns
		nB HIGH; see Fig. 8								
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		n $\overline{CD}$ LOW; see Fig. 8								
		V _{CC} = 4.5 V	20	11	-	25	-	30	-	ns
		nQ and n $\overline{Q}$ HIGH or LOW; see Fig. 8								
t _{rec}	recovery time	n $\overline{CD}$ to n $\overline{A}$, nB; see Fig. 8								
		V _{CC} = 4.5 V	7	2	-	9	-	11	-	ns
t _{trig}	retrigger time	n $\overline{A}$, nB; see Fig. 8; X = C _{EXT} / (4.5 × V _{CC})								
		V _{CC} = 4.5 V	-	80+X	-	-	-	-	-	ns
R _{EXT}	external timing resistor	V _{CC} = 5.0 V	2	-	1000	-	-	-	-	kΩ
C _{EXT}	external timing capacitor	V _{CC} = 5.0 V	no limits							
C _{PD}	power dissipation capacitance	per multivibrator; V _I = GND to V _{CC} - 1.5 V [2]	-	138	-	-	-	-	-	pF

[1] t_t is the same as t_{THL} and t_{TLH}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) + 0.48 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 0.8 \times V_{CC} \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs; C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

D = duty cycle factor in %; C_{EXT} = external timing capacitance in pF.

10.1. Waveforms and test circuit

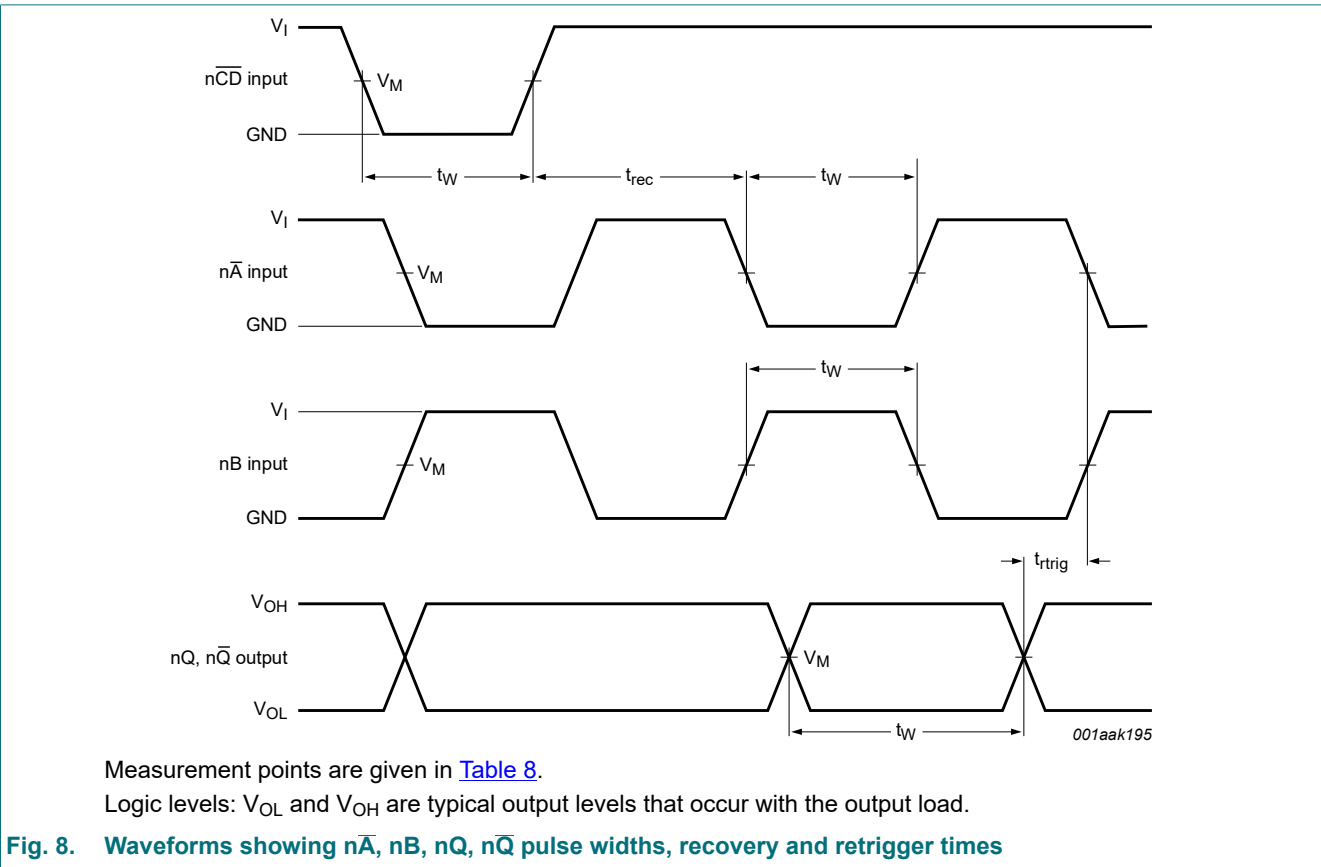
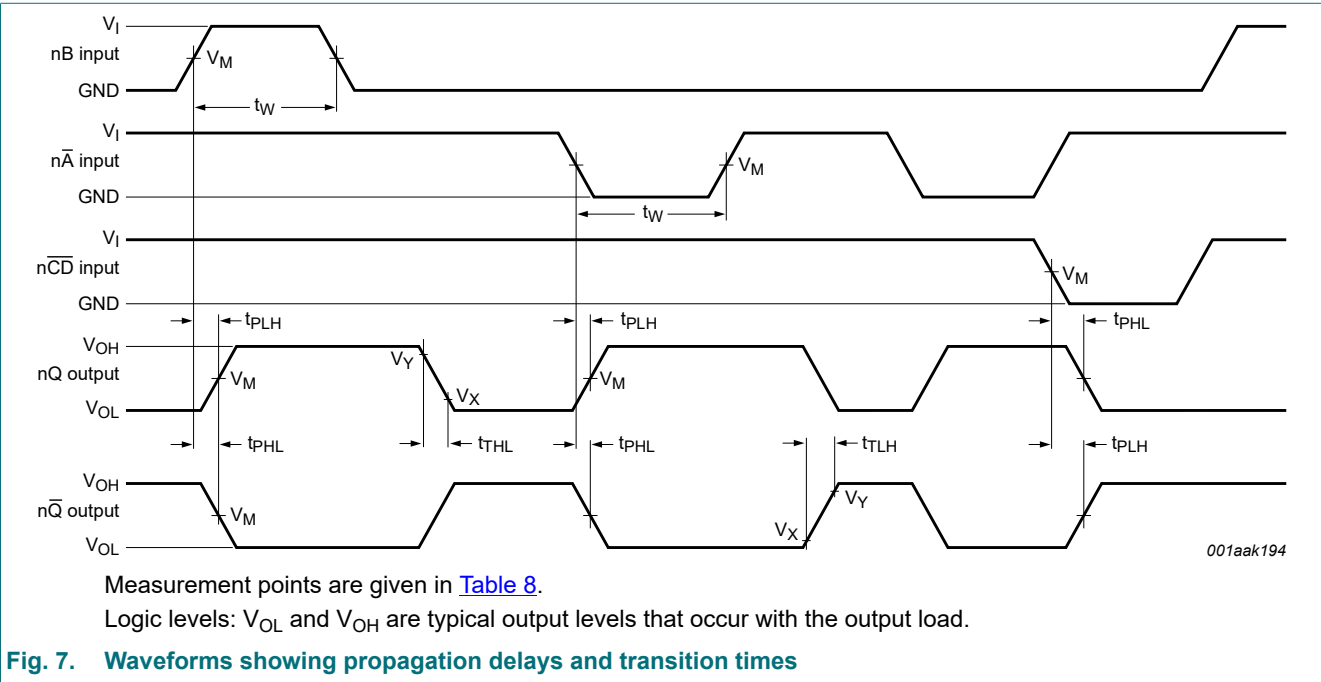


Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$

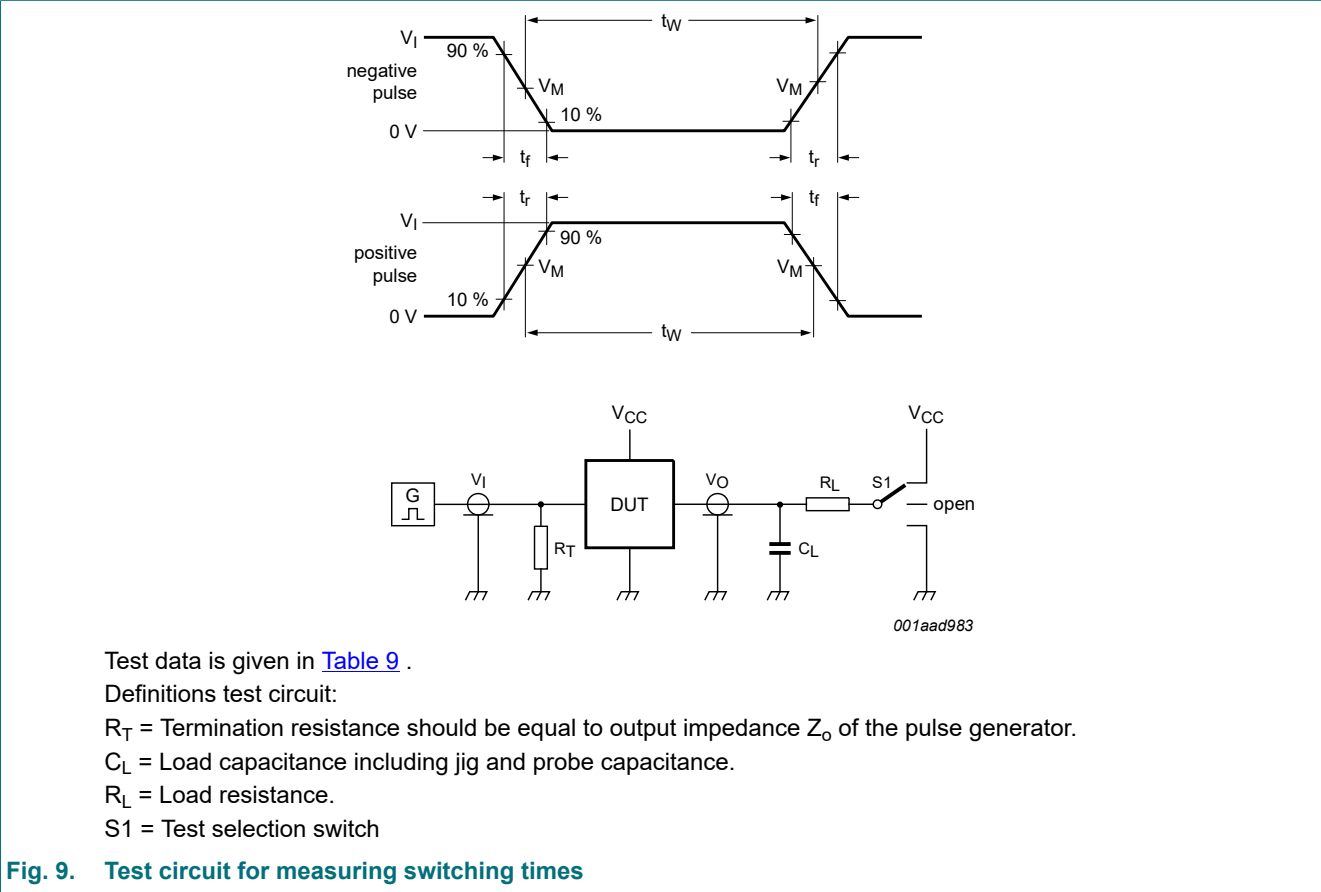


Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
3 V	6 ns	15 pF, 50 pF	1 kΩ	open

11. Application information

11.1. Power-down considerations

A large capacitor (C_{EXT}) may cause problems when powering-down the monostable due to energy stored in this capacitor. When a system containing this device is powered-down or rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Fig. 10

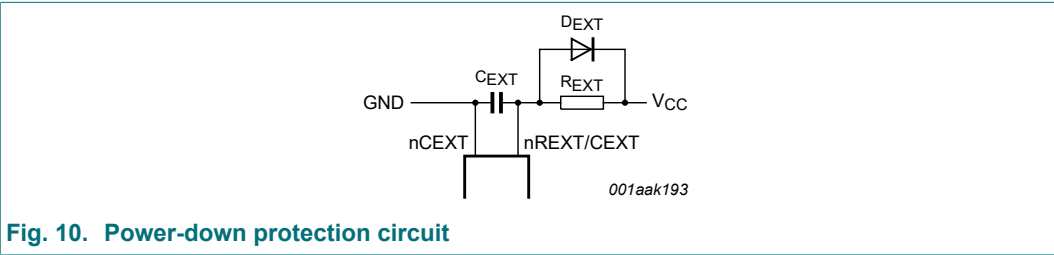


Fig. 10. Power-down protection circuit

11.2. Graphs

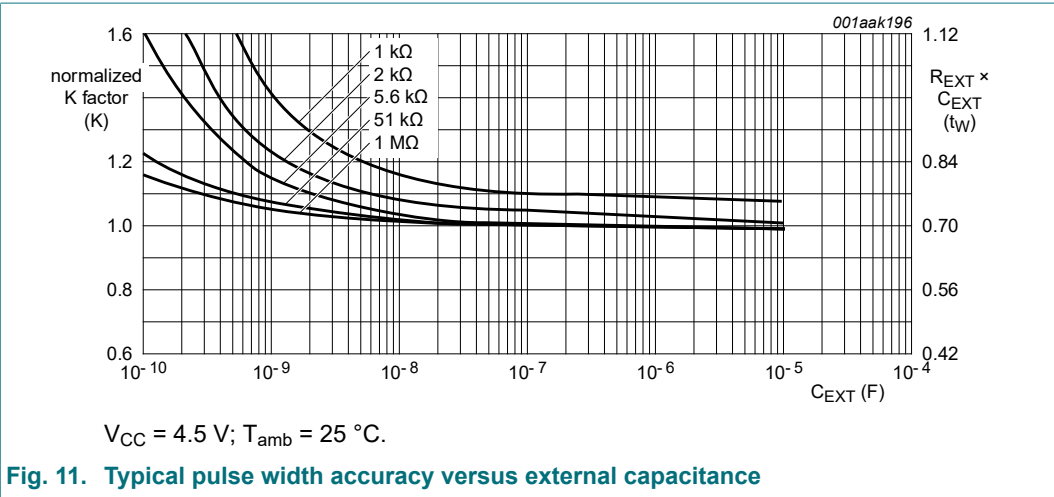


Fig. 11. Typical pulse width accuracy versus external capacitance

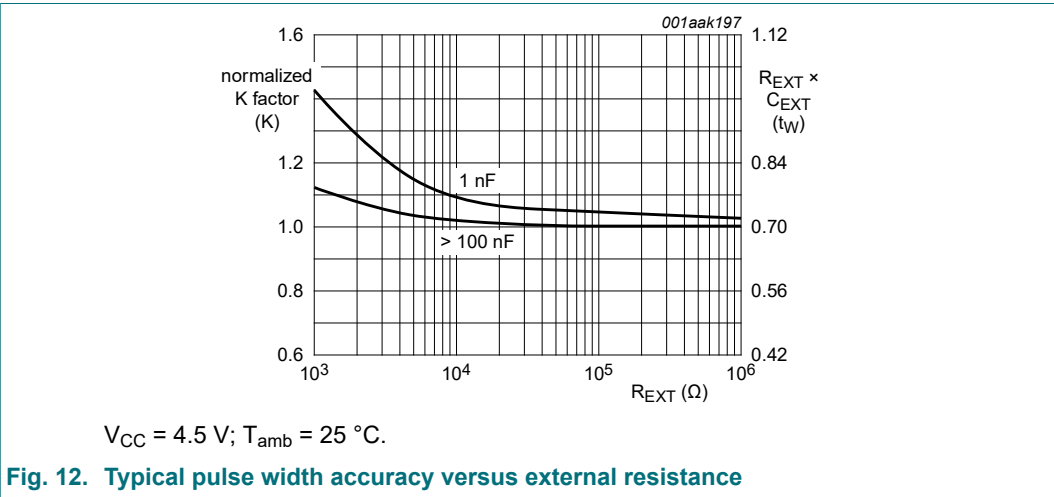


Fig. 12. Typical pulse width accuracy versus external resistance

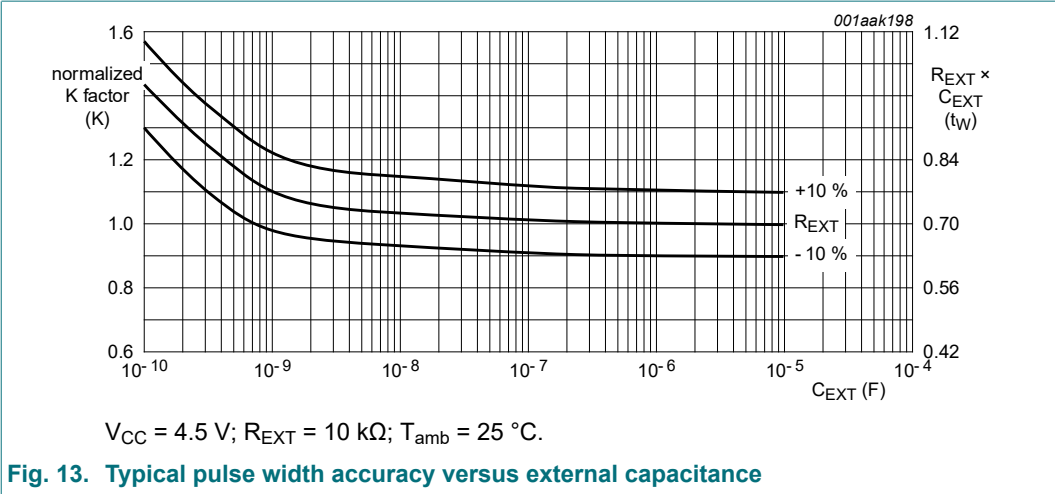


Fig. 13. Typical pulse width accuracy versus external capacitance

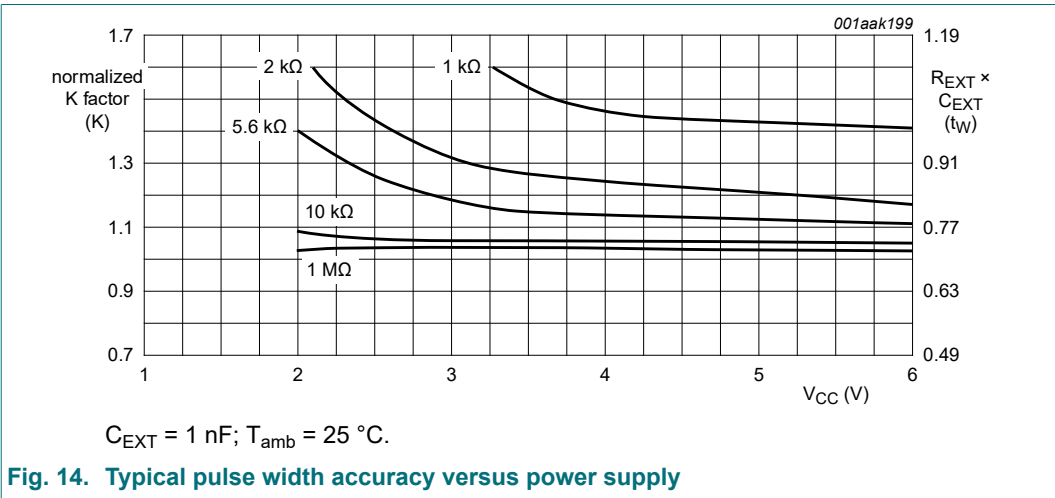


Fig. 14. Typical pulse width accuracy versus power supply

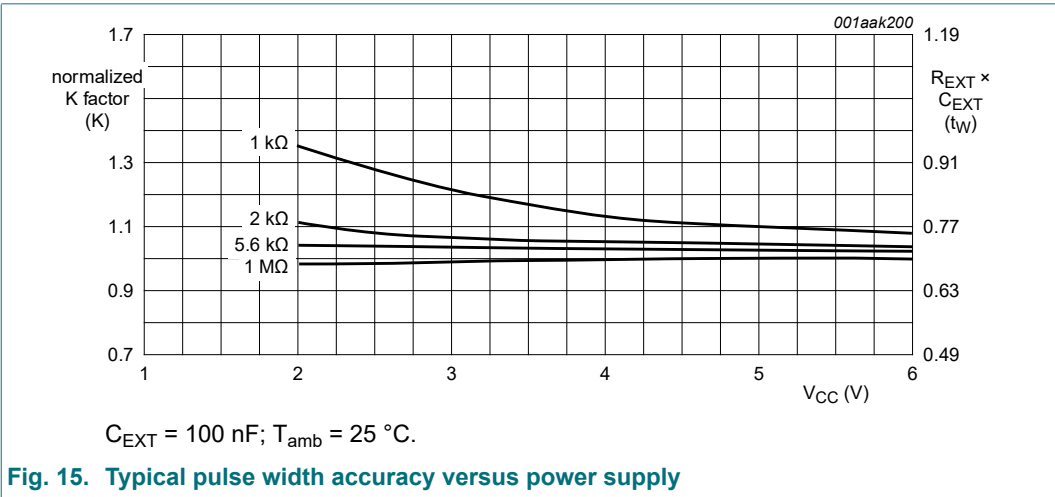


Fig. 15. Typical pulse width accuracy versus power supply

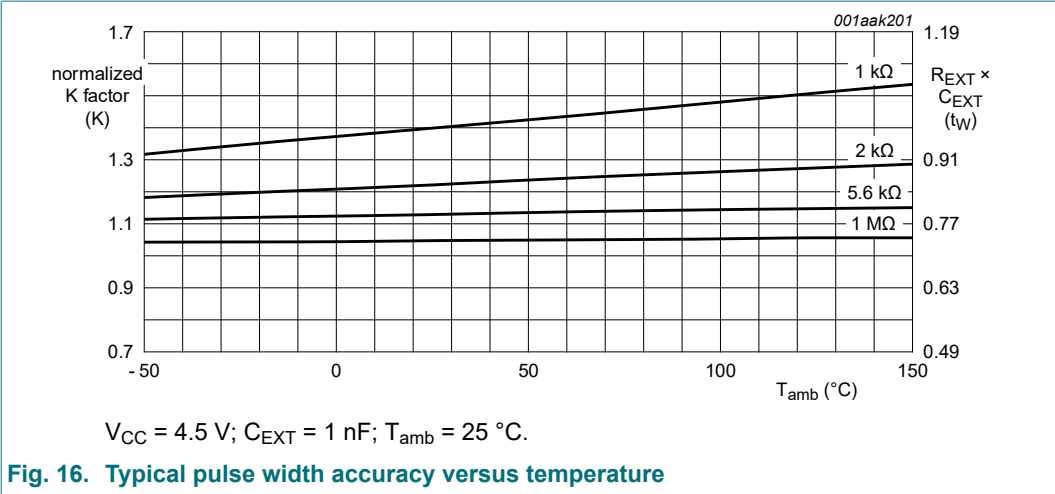


Fig. 16. Typical pulse width accuracy versus temperature

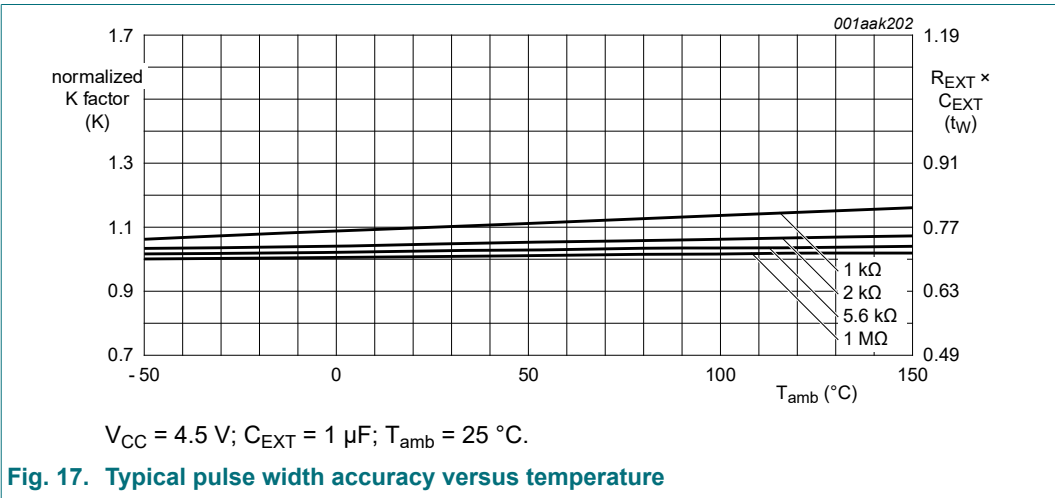


Fig. 17. Typical pulse width accuracy versus temperature

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

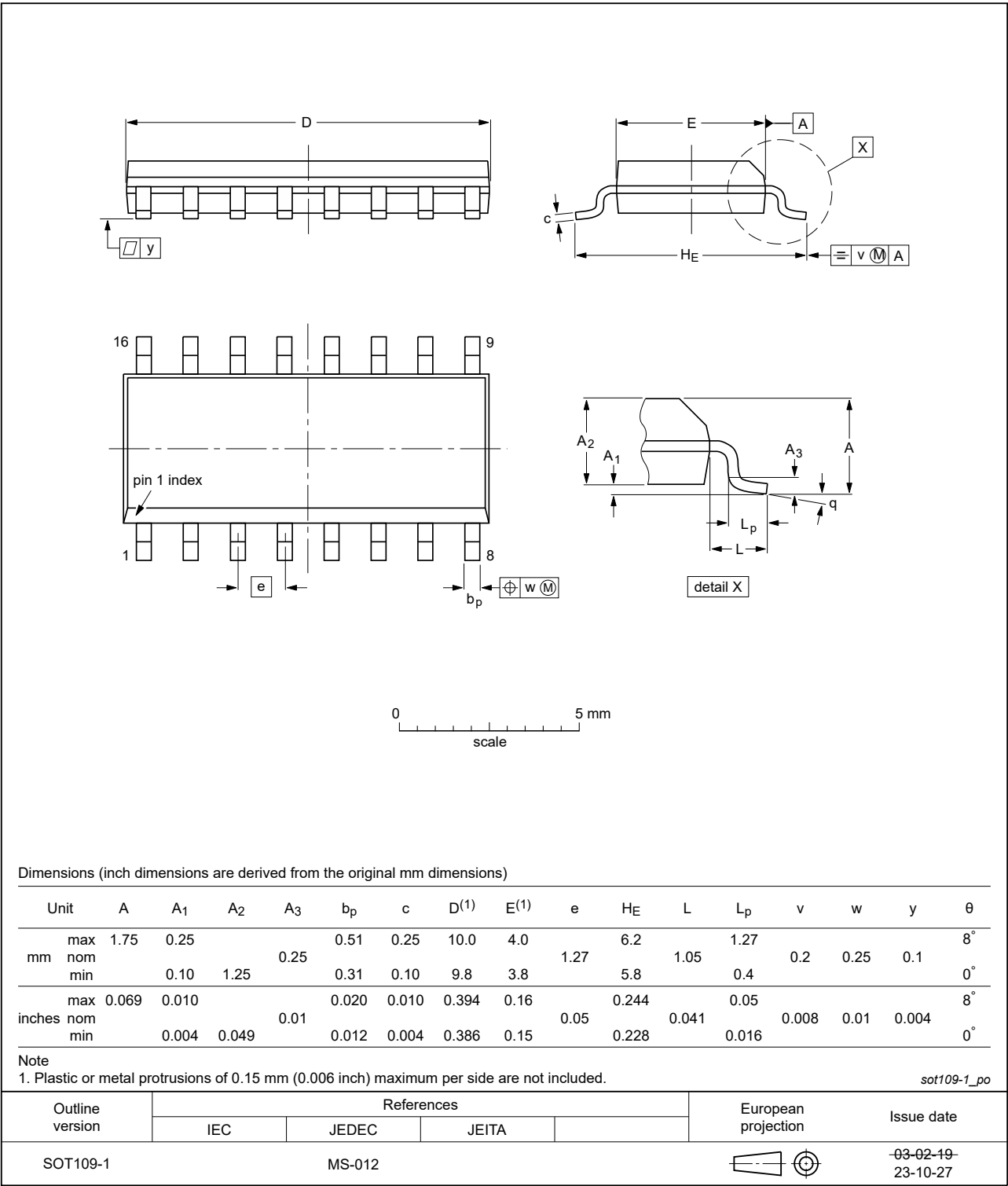


Fig. 18. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

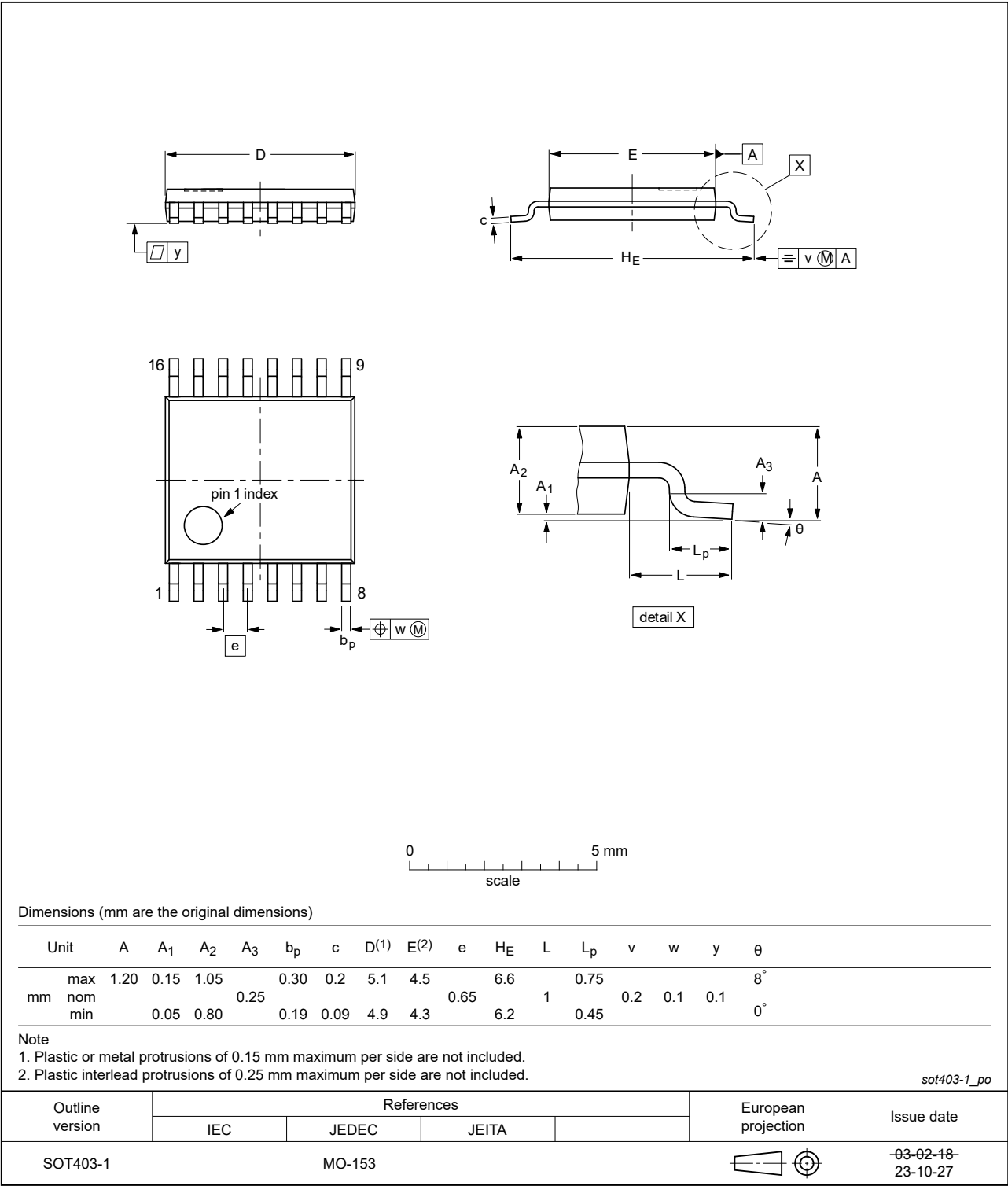


Fig. 19. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCT4538_Q100 v.5	20240326	Product data sheet	-	74HCT4538_Q100 v.4
Modifications:	Fig. 18, Fig. 19: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. Section 2: ESD specification updated according to the latest JEDEC standard.			
74HCT4538_Q100 v.4	20210211	Product data sheet	-	74HCT4538_Q100 v.3
Modifications:	Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation updated.			
74HCT4538_Q100 v.3	20170317	Product data sheet	-	74HC_HCT4538_Q100 v.2
Modifications:	Type numbers 74HC4538D-Q100 and 74HC4538PW-Q100 removed.			
74HC_HCT4538_Q100 v.2	20151223	Product data sheet	-	74HC_HCT4538_Q100 v.1
Modifications:	C_{PD} formula corrected (errata).			
74HC_HCT4538_Q100 v.1	20120802	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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