



PSMN8R0-40HL

N-channel 40 V, 9.4 mOhm, logic level MOSFET in LPAK56D using TrenchMOS technology

30 September 2022

Product data sheet

1. General description

Dual logic level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology.

2. Features and benefits

- Dual MOSFET
- Repetitive avalanche rated
- High reliability LPAK56D package
- Copper-clip, solder die attach
- Qualified to 175 °C

3. Applications

- Brushless DC motor control
- DC-to-DC converters
- High-performance synchronous rectification
- High performance and high efficiency server power supply

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	30	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	53	W
T_j	junction temperature			-55	-	175	°C
Static characteristics FET1 and FET2							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		-	7.66	9.4	mΩ
		$V_{GS} = 5\text{ V}$; $I_D = 10\text{ A}$; $T_j = 175\text{ °C}$; Fig. 11 ; Fig. 12		-	15.4	18.9	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14		-	5.3	-	nC
$Q_{G(tot)}$	total gate charge			-	15.7	-	nC
Avalanche ruggedness FET1 and FET2							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 30\text{ A}$; $V_{sup} \leq 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; Fig. 4	[2] [3]	-	-	84	mJ

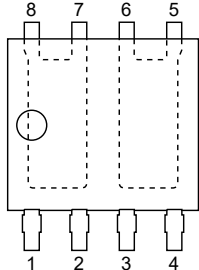
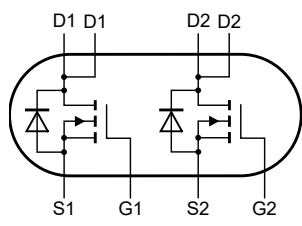
N-channel 40 V, 9.4 mOhm, logic level MOSFET in LFAK56D using TrenchMOS technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode FET1 and FET2						
Q _r	recovered charge	I _S = 10 A; di _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _j = 25 °C	-	12.1	-	nC

- [1] Continuous current is limited by package.
- [2] Refer to application note AN10273 for further information
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFAK56D; Dual LFAK (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN8R0-40HL	LFAK56D; Dual LFAK	plastic, single ended surface mounted package (LFAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN8R0-40HL	8R0L40H

8. Limiting values

Table 5. Limiting values

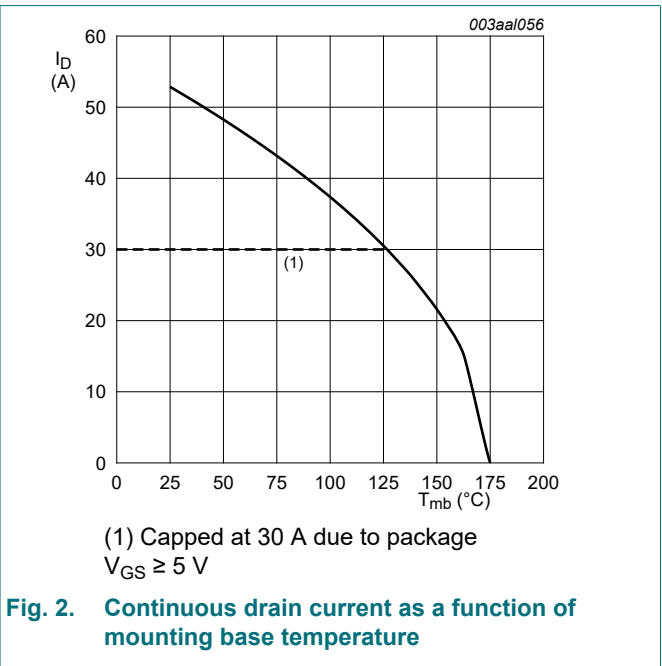
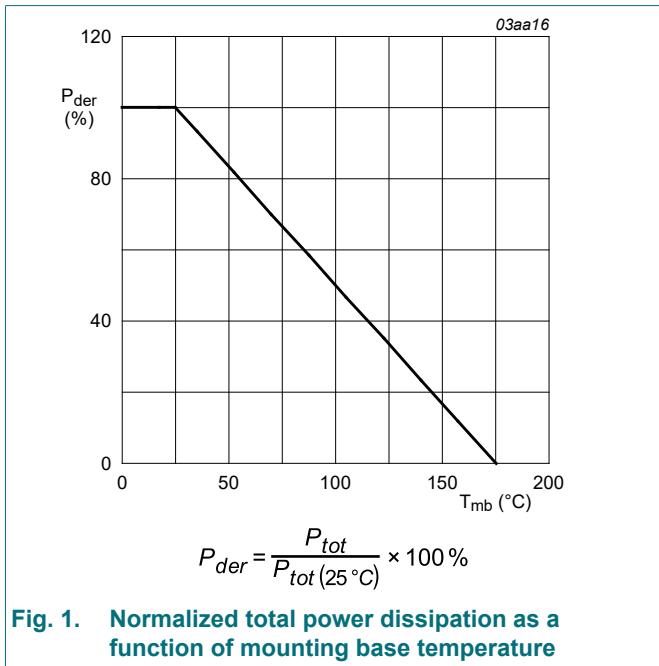
In accordance with the Absolute Maximum Rating System (IEC 60134).

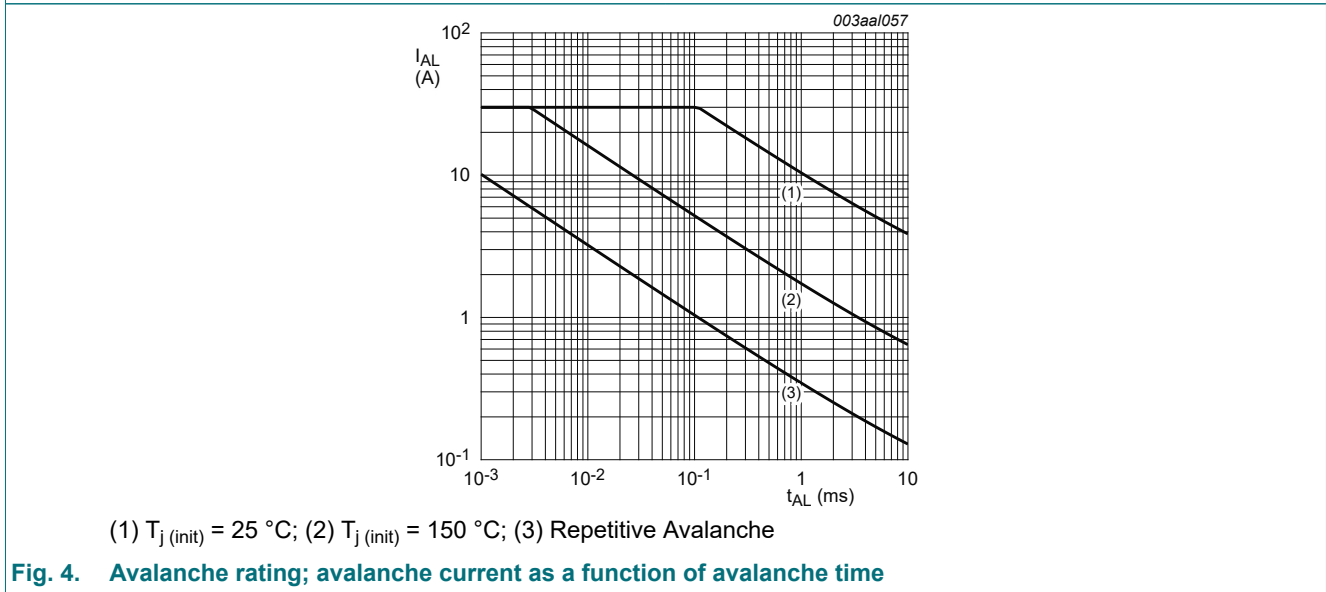
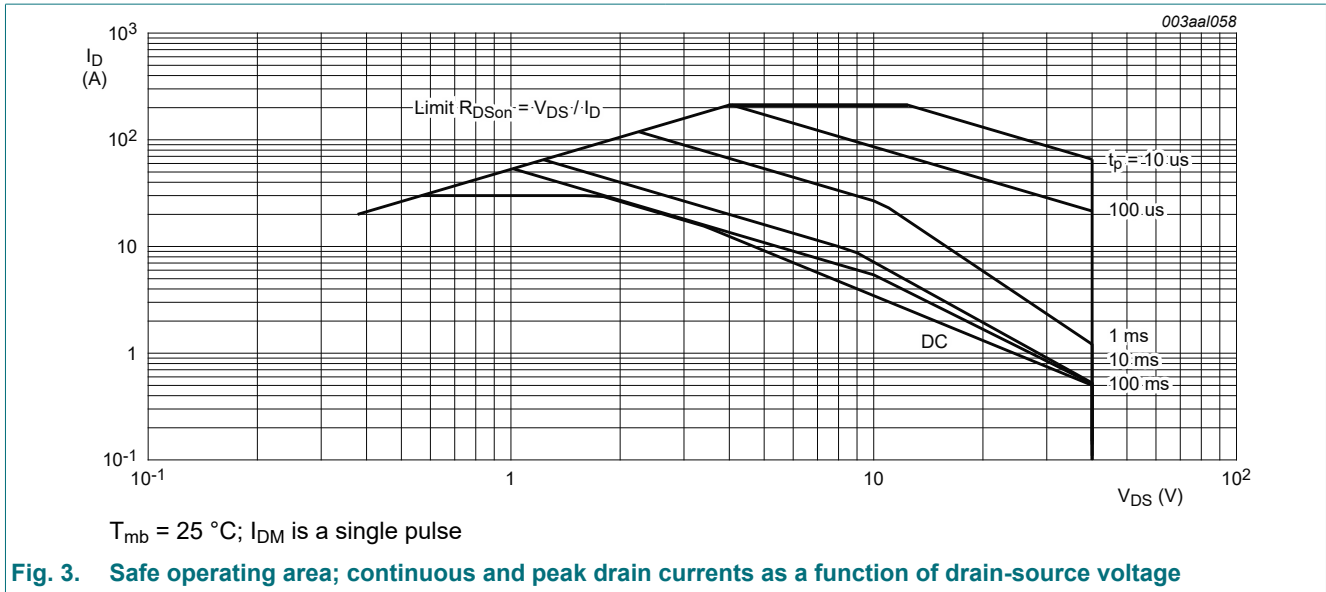
Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	40	V	
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	40	V	
V _{GS}	gate-source voltage	Pulsed; T _j ≤ 175 °C	[1] [2]	-15	15	V
		DC; T _j ≤ 175 °C		-10	10	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	53	W	

N-channel 40 V, 9.4 mOhm, logic level MOSFET in LPAK56D using TrenchMOS technology

Symbol	Parameter	Conditions		Min	Max	Unit
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; Fig. 2	[3]	-	30	A
		V _{GS} = 5 V; T _{mb} = 100 °C; Fig. 2	[3]	-	30	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	211	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I _S	source current	T _{mb} = 25 °C	[3]	-	30	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	211	A
Avalanche ruggedness FET1 and FET2						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 30 A; V _{sup} ≤ 40 V; V _{GS} = 10 V; T _{j(initial)} = 25 °C; Fig. 4	[4] [5]	-	84	mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and/or V_{GS}.
- [3] Continuous current is limited by package.
- [4] Refer to application note AN10273 for further information
- [5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	2.84	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

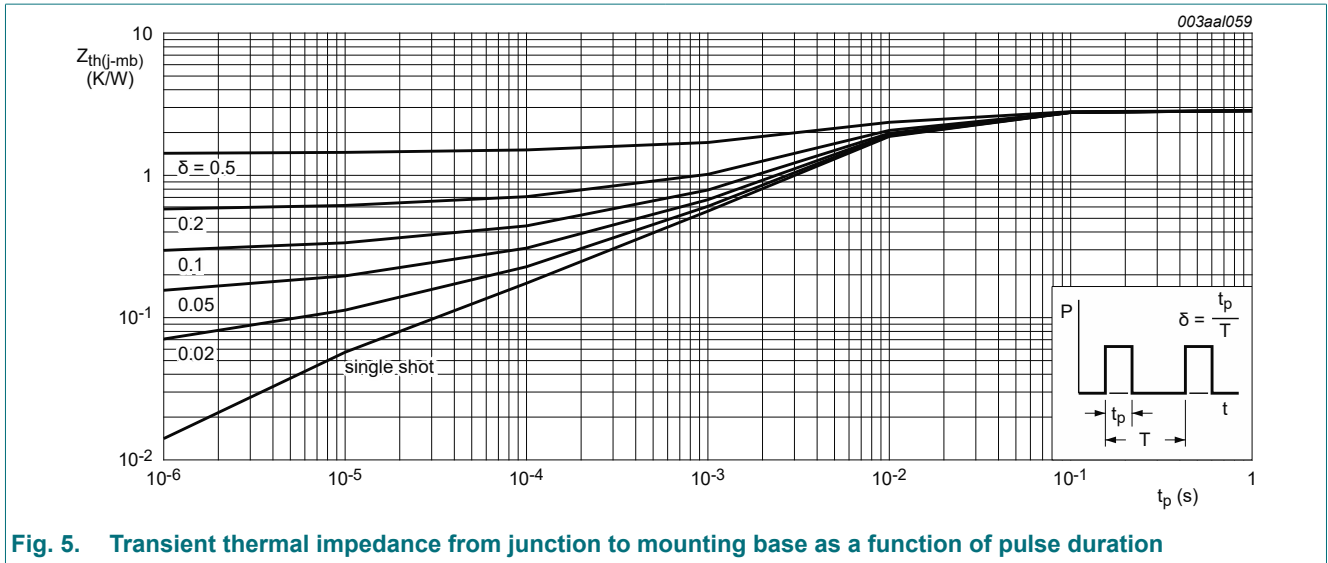


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

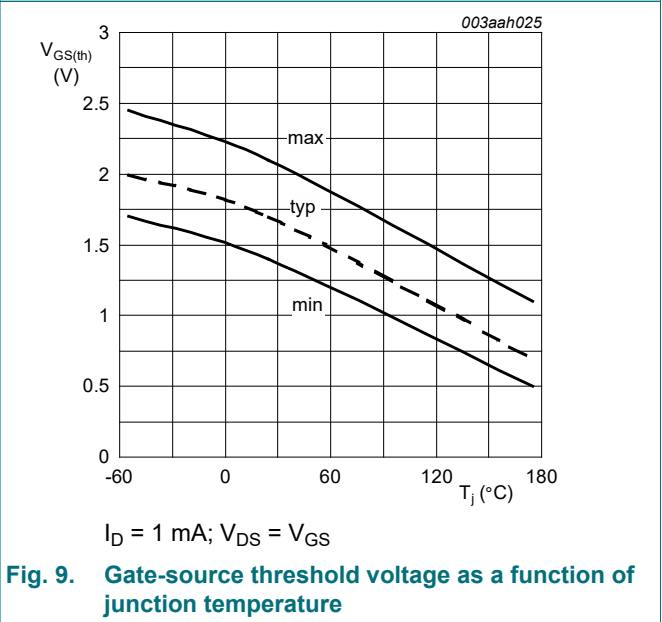
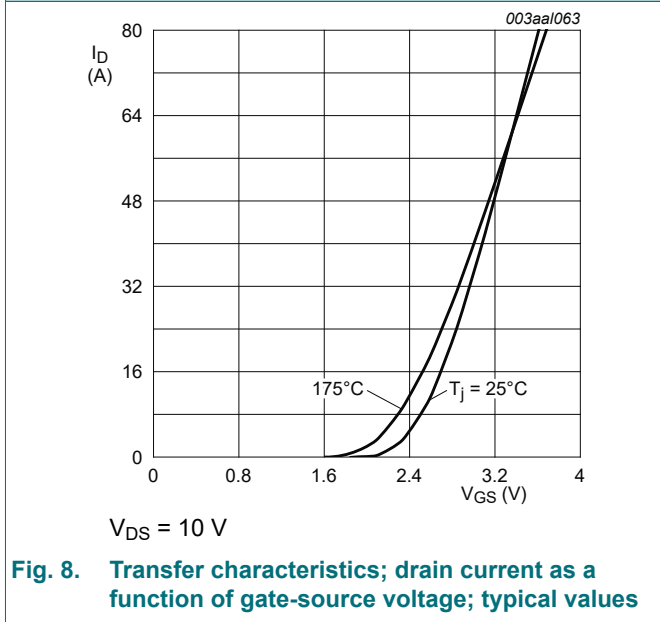
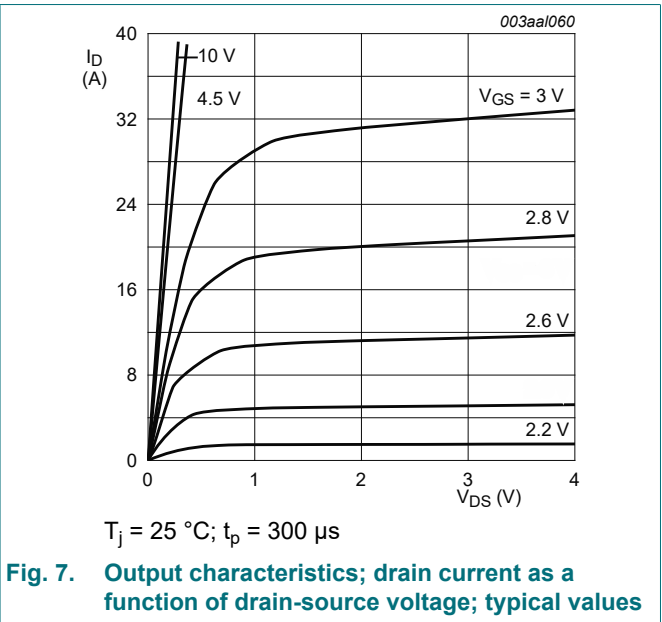
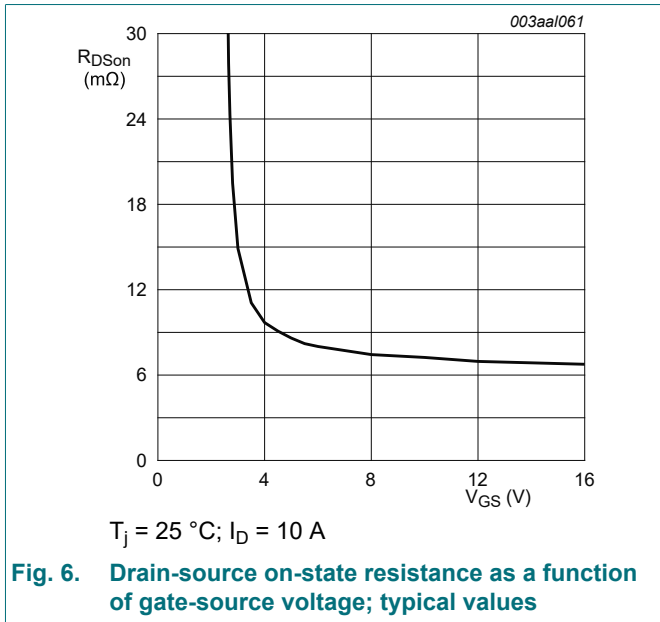
10. Characteristics

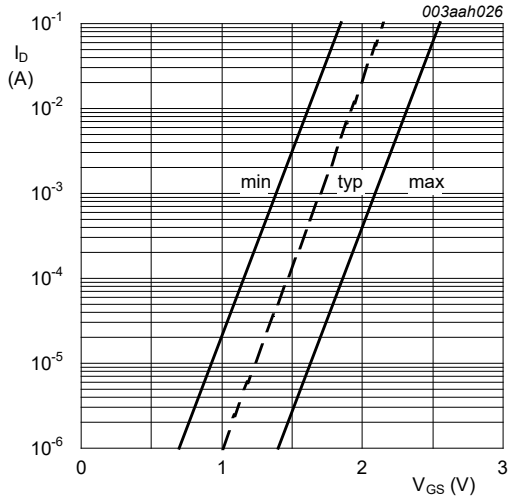
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$; Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$; Fig. 9; Fig. 10	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$; Fig. 9; Fig. 10	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	μA
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA
I_{GSS}	gate leakage current	$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 11	-	7.66	9.4	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 175 \text{ }^\circ C$; Fig. 11; Fig. 12	-	15.4	18.9	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 11	-	6.26	8	m Ω
Dynamic characteristics FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 13; Fig. 14	-	15.7	-	nC
Q_{GS}	gate-source charge		-	3.2	-	nC
Q_{GD}	gate-drain charge		-	5.3	-	nC
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; Fig. 15	-	1583	2110	pF
C_{oss}	output capacitance		-	225	270	pF
C_{rss}	reverse transfer capacitance		-	114	157	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 32 \text{ V}; R_L = 3.3 \text{ } \Omega; V_{GS} = 5 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	10.8	-
t_r	rise time		-	19.8	-	ns

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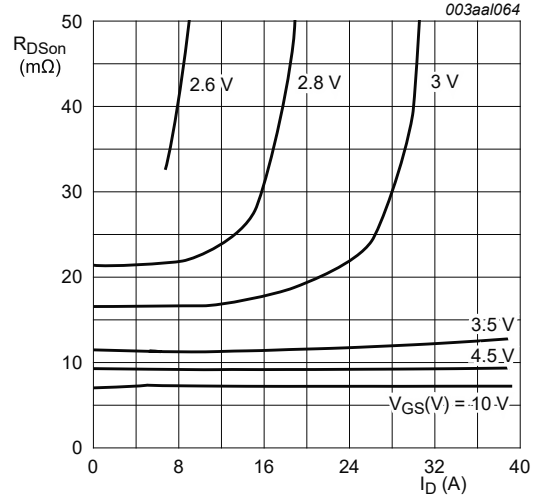
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(off)}$	turn-off delay time		-	20.5	-	ns
t_f	fall time		-	18.2	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 16	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	20.5	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	12.1	-	nC





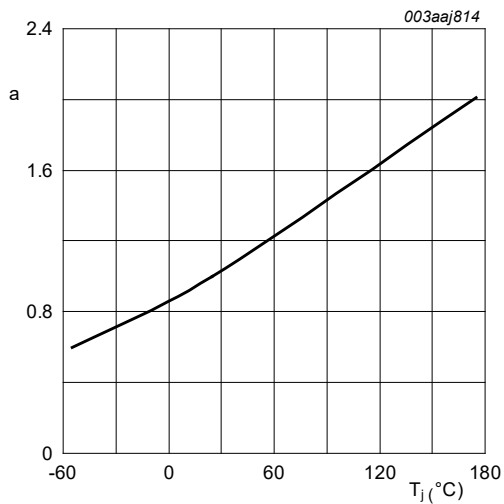
$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$

Fig. 10. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25\text{ °C}; t_p = 300\text{ μs}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ °C})}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

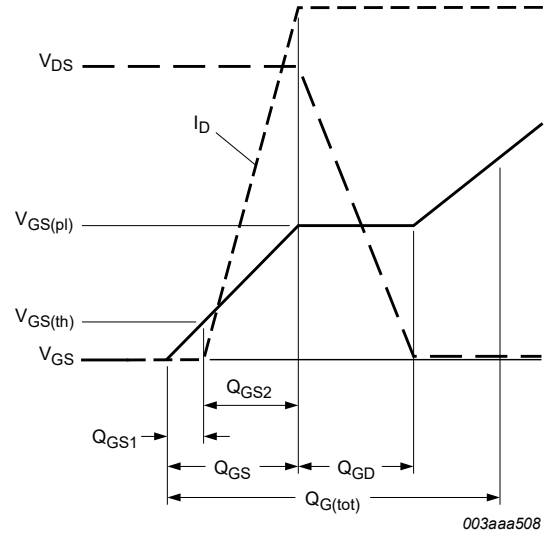


Fig. 13. Gate charge waveform definitions

N-channel 40 V, 9.4 mOhm, logic level MOSFET in LPAK56D using TrenchMOS technology

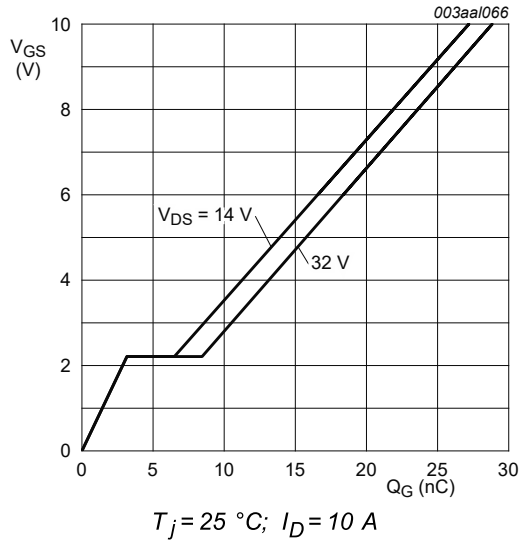


Fig. 14. Gate-source voltage as a function of gate charge; typical values

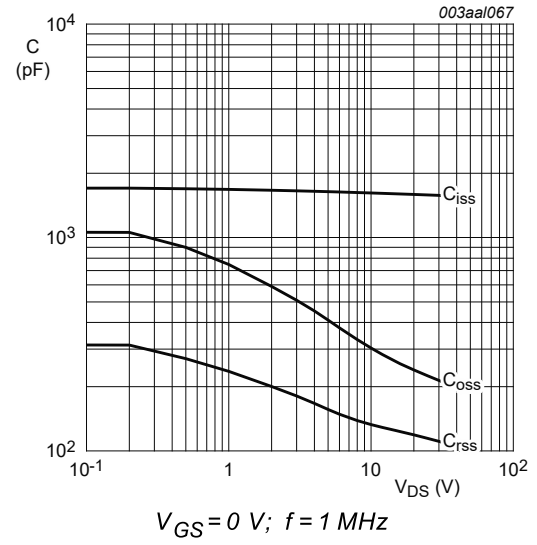


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

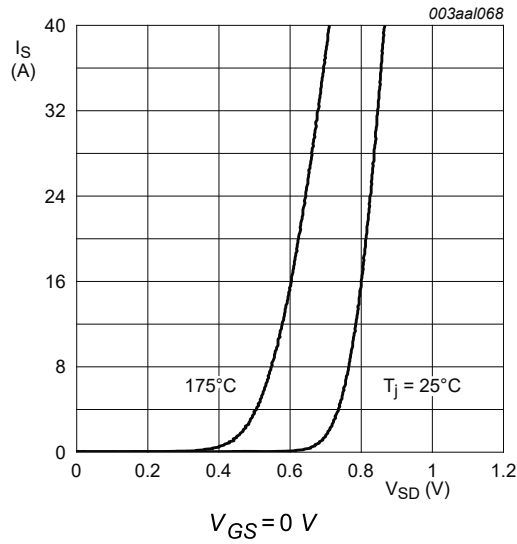


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

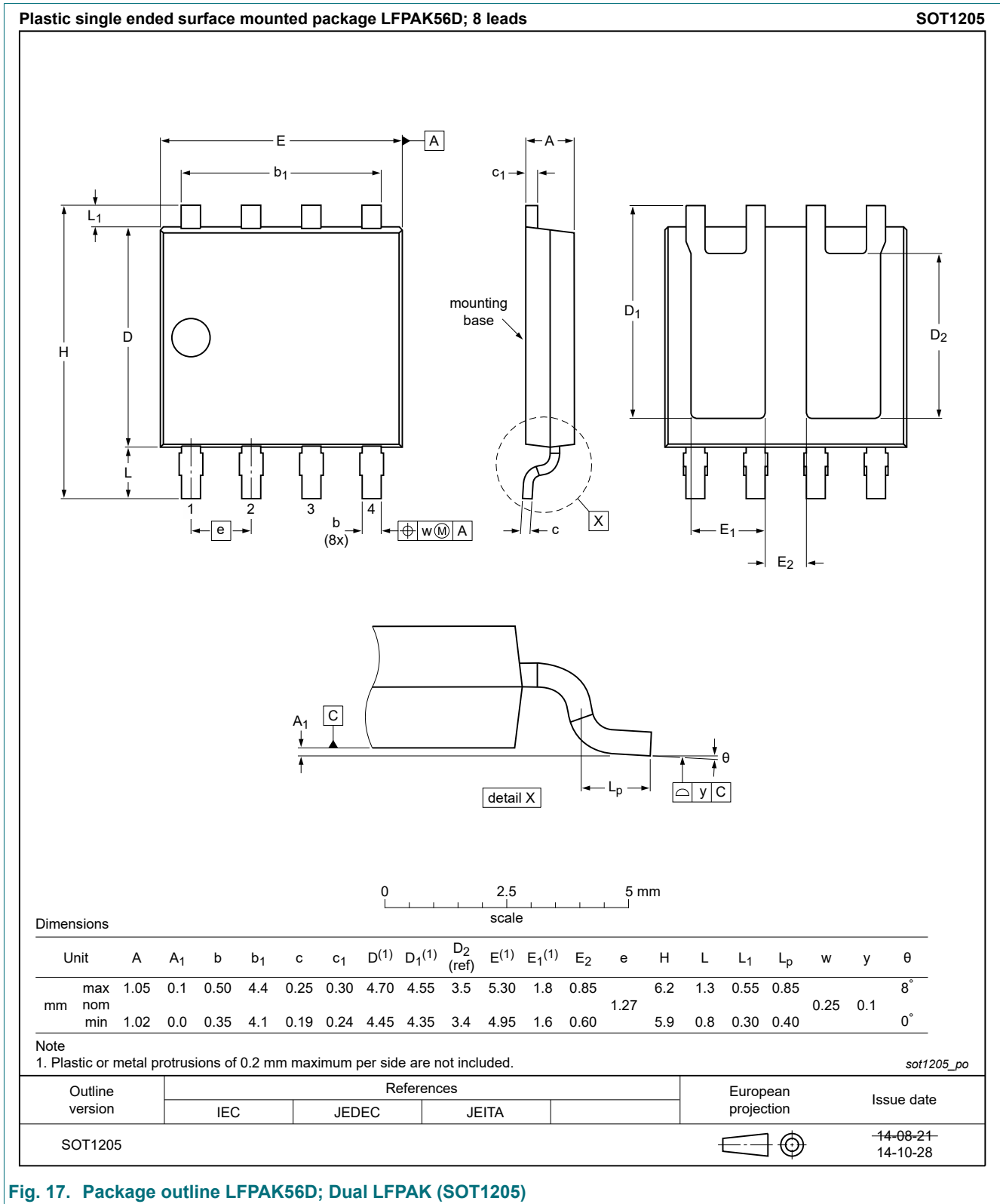


Fig. 17. Package outline LPAK56D; Dual LPAK (SOT1205)

12. Soldering

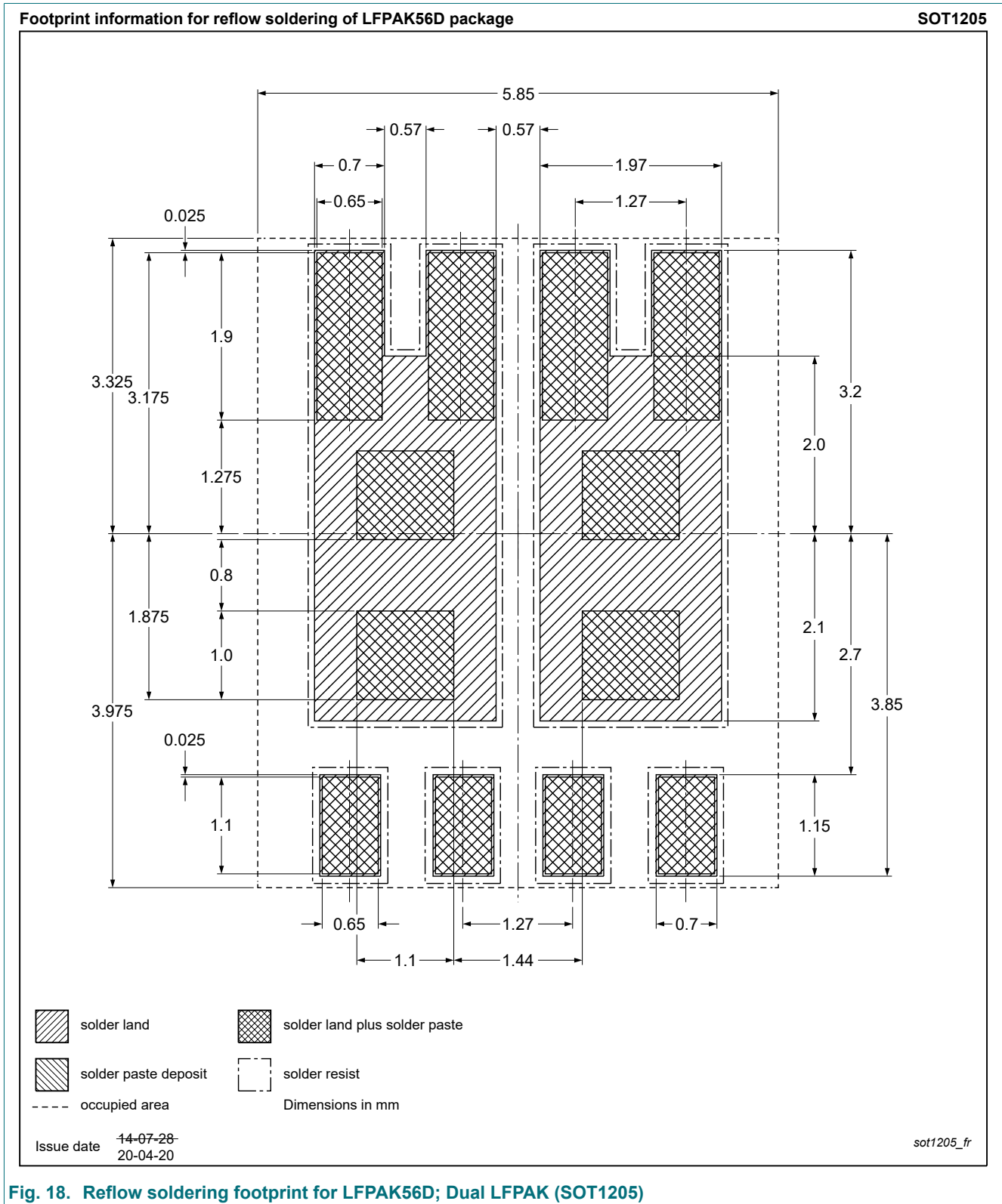


Fig. 18. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Contents

1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	2
9. Thermal characteristics.....	4
10. Characteristics.....	5
11. Package outline.....	9
12. Soldering.....	10
13. Legal information.....	11

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