

PUMH30

NPN/NPN resistor-equipped double transistor; R1 = 2.2 k Ω , R2 = open

12 December 2024

Product data sheet

1. General description

NPN/NPN double Resistor-Equipped Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PUMD30 PNP/PNP complement: PUMB30

2. Features and benefits

- 100 mA output current capability
- Reduces component count
- Built-in bias resistors
- · Reduces pick and place costs
- · Simplifies circuit design
- AEC-Q101 qualified

3. Applications

- Low current peripheral driver
- Cost-saving alternative for BC847BS and BC847BV
- · Control of IC inputs

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | | Min | Тур | Max | Unit |
|------------------|---------------------------|------------|-----|------|-----|------|------|
| Per transistor | | | | | | | |
| V _{CEO} | collector-emitter voltage | open base | | - | - | 50 | V |
| Io | output current | | | - | - | 100 | mA |
| R1 | bias resistor 1 (input) | | [1] | 1.54 | 2.2 | 2.86 | kΩ |

[1] See "Section 11: Test information" for resistor calculation and test conditions.



NPN/NPN resistor-equipped double transistor; R1 = 2.2 k Ω , R2 = open

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|------------------------|--------------------|----------------------|
| 1 | GND1 | GND (emitter) TR1 | | O1 I2 GND2 |
| 2 | I1 | input (base) TR1 | □6 □5 □4 | |
| 3 | O2 | output (collector) TR2 | | R1 TR2 |
| 4 | GND2 | GND (emitter) TR2 | 0 | TR1 |
| 5 | 12 | input (base) TR2 | 1 1 2 3 | R1 |
| 6 | O1 | output (collector) TR1 | TSSOP6 (SOT363) | GND1 I1 O2 sym090 |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | | | |
|-------------|---------|---|---------------|--|--|
| | Name | Description | Version | | |
| PUMH30 | | plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body | <u>SOT363</u> | | |

7. Marking

Table 4. Marking codes

| Type number | Marking code[1] |
|-------------|-----------------|
| PUMH30 | %B1 |

[1] % = placeholder for manufacturing site code

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|------------------|---------------------------|-------------------------------------|-----|-----|-----|------|
| Per transiste | or | | | | | |
| V _{CBO} | collector-base voltage | open emitter | | - | 50 | V |
| V_{CEO} | collector-emitter voltage | open base | | - | 50 | V |
| V_{EBO} | emitter-base voltage | open collector | | - | 5 | V |
| Io | output current | | | - | 100 | mA |
| I _{CM} | peak collector current | t _p ≤ 1 ms; single pulse | | - | 100 | mA |
| P _{tot} | total power dissipation | T _{amb} ≤ 25 °C | [1] | - | 200 | mW |
| Per device | | | | | | |
| P _{tot} | total power dissipation | T _{amb} = 25 °C | [1] | - | 300 | mW |
| Tj | junction temperature | | | - | 150 | °C |
| T _{amb} | ambient temperature | | | -65 | 150 | °C |
| T _{stg} | storage temperature | | | -65 | 150 | °C |

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | | Min | Тур | Max | Unit |
|----------------|---|-------------|-----|-----|-----|-----|------|
| Per transistor | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 625 | K/W |
| Per device | | | • | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 416 | K/W |

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

NPN/NPN resistor-equipped double transistor; R1 = 2.2 k Ω , R2 = open

10. Characteristics

Table 7. Characteristics

 T_{amb} = 25 °C unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Тур | Max | Unit |
|----------------------|--------------------------------------|---|-----|------|-----|------|------|
| Per transist | or | | | | | | |
| V _{(BR)CBO} | collector-base breakdown voltage | $I_C = 100 \ \mu A; I_E = 0 \ A; T_{amb} = 25 \ ^{\circ}C$ | | 50 | - | - | V |
| V _{(BR)CEO} | collector-emitter breakdown voltage | $I_C = 2 \text{ mA}; I_B = 0 \text{ A}; T_{amb} = 25 \text{ °C}$ | | 50 | - | - | V |
| I _{CBO} | collector-base cut-off current | V _{CB} = 50 V; I _E = 0 A; T _{amb} = 25 °C | | - | - | 100 | nA |
| I _{CEO} | collector-emitter cut-off | V _{CE} = 30 V; I _B = 0 A; T _{amb} = 25 °C | | - | - | 100 | nA |
| | current | V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C | | - | - | 5 | μΑ |
| I _{EBO} | emitter-base cut-off current | V _{EB} = 5 V; I _C = 0 A; T _{amb} = 25 °C | | - | - | 100 | nA |
| h _{FE} | DC current gain | V _{CE} = 5 V; I _C = 20 mA; T _{amb} = 25 °C | | 30 | - | - | |
| V _{CEsat} | collector-emitter saturation voltage | $I_C = 10 \text{ mA}; I_B = 0.5 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$ | | - | - | 150 | mV |
| R1 | bias resistor 1 (input) | | [1] | 1.54 | 2.2 | 2.86 | kΩ |
| C _c | collector capacitance | $V_{CB} = 10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A}; f = 1 \text{ MHz}; $ $T_{amb} = 25 \text{ °C}$ | | - | - | 2.5 | pF |

[1] See "Section 11: Test information" for resistor calculation and test conditions.

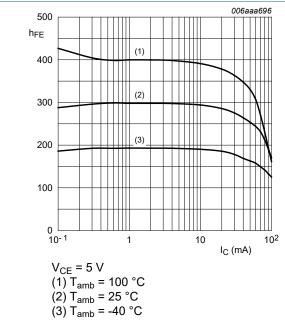


Fig. 1. DC current gain as a function of collector current; typical values

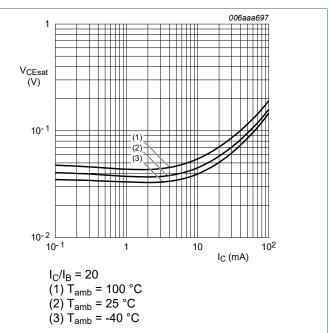


Fig. 2. Collector-emitter saturation voltage as a function of collector current; typical values

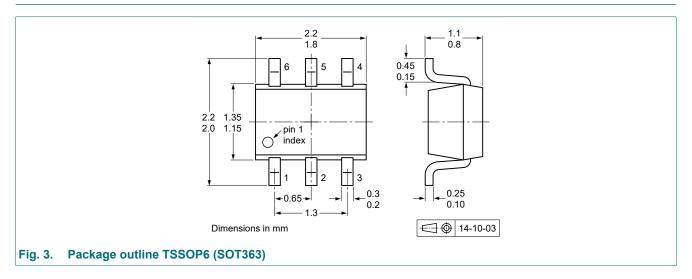
NPN/NPN resistor-equipped double transistor; R1 = 2.2 k Ω , R2 = open

11. Test information

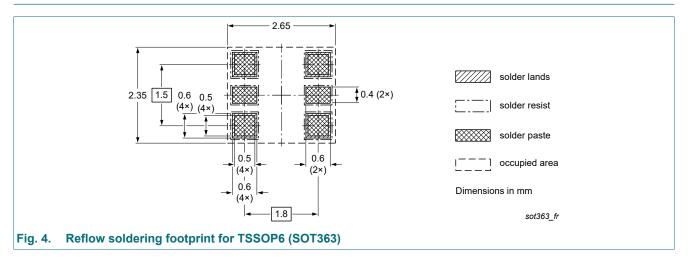
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101* - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

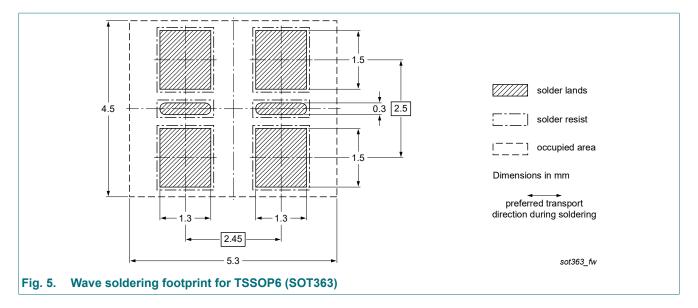
12. Package outline



13. Soldering



NPN/NPN resistor-equipped double transistor; R1 = 2.2 k Ω , R2 = open



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14. Revision history

Table 8. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes | | | |
|-----------------|--|--------------------|---------------|-----------------|--|--|--|
| PUMH30 v.2 | 20241212 | Product data sheet | - | PEMH30_PUMH30_1 | | | |
| Modification: | Family data sheet reduced to single type data sheet. The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Packing information is removed. | | | | | | |
| PEMH30_PUMH30_1 | 20060328 | Product data sheet | - | - | | | |

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15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|-----------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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NPN/NPN resistor-equipped double transistor; R1 = 2.2 k Ω , R2 = open

Contents

| 1. | General description | . 1 |
|-----|-------------------------|-----|
| 2. | Features and benefits | . 1 |
| 3. | Applications | . 1 |
| 4. | Quick reference data | . 1 |
| 5. | Pinning information | . 2 |
| 6. | Ordering information | . 2 |
| 7. | Marking | . 2 |
| 8. | Limiting values | . 3 |
| 9. | Thermal characteristics | . 3 |
| 10. | Characteristics | . 4 |
| 11. | Test information | . 5 |
| 12. | Package outline | . 5 |
| 13. | Soldering | . 5 |
| 14. | Revision history | .7 |
| 15. | Legal information | .8 |
| | | |

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