



BUK4D122-20P

20 V, P-channel Trench MOSFET

27 March 2023

Product data sheet

1. General Description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Extended temperature range $T_j = 175\text{ °C}$
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Tin-plated 100% solderable side pads for optical solder inspection
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- Trench MOSFET technology
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

4. Quick reference data

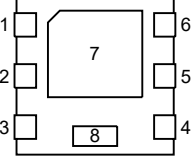
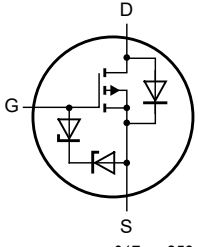
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
V_{GS}	gate-source voltage		-12	-	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-3.2	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -3.2\text{ A}; T_j = 25\text{ °C}$	-	100	122	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view DFN2020MD-6 (SOT1220)</p>	 <p>017aaa259</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK4D122-20P	DFN2020MD-6	plastic, leadless thermal enhanced ultra thin small outline package with side-wettable flanks (SWF); 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1220

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK4D122-20P	6H

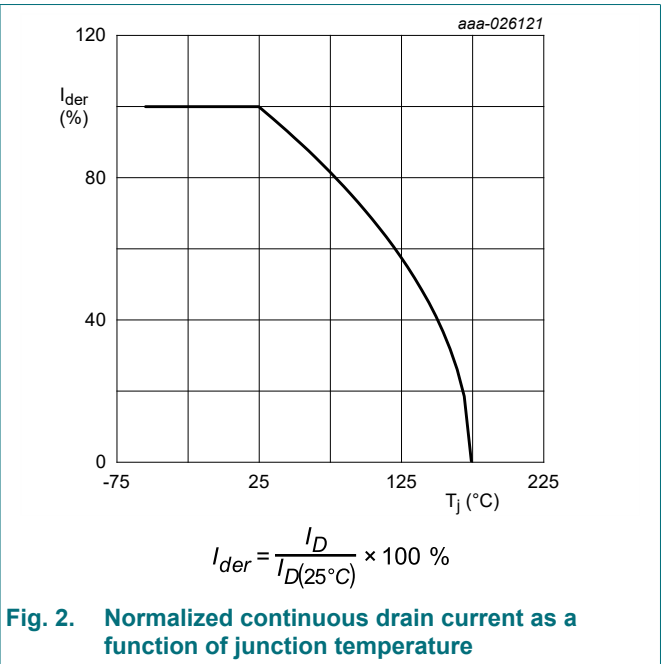
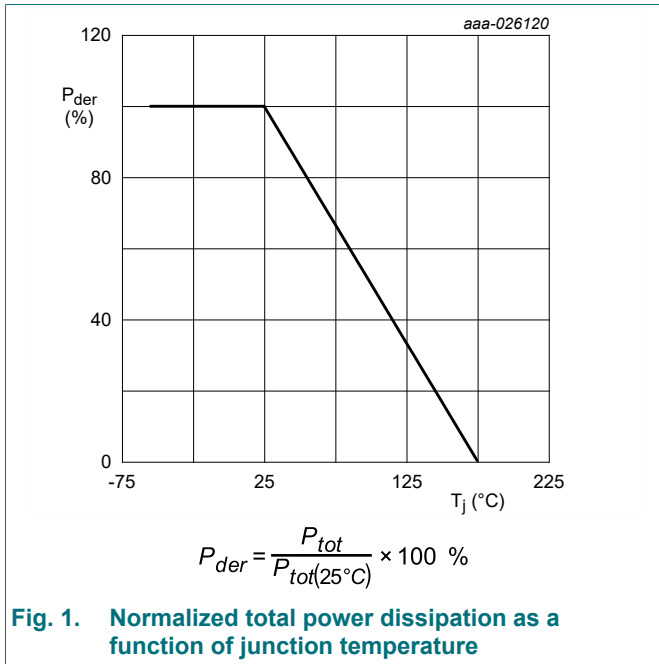
8. Limiting values

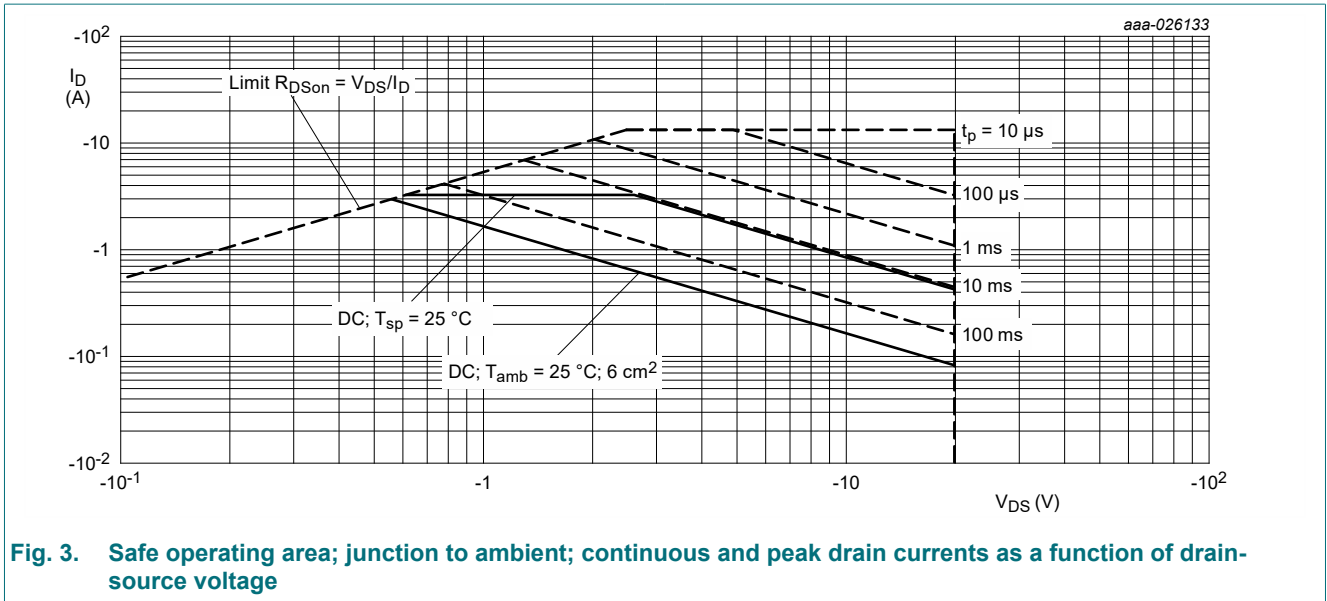
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-12	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-3.2	A
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-2	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-13	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	550	mW
			[1]	-	1.95	W
		T _{sp} = 25 °C		-	10	W
T _j	junction temperature			-55	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	T _{j(initial)} = 25 °C; I _D = -0.5 A; DUT in avalanche (unclamped)		-	5	mJ
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.9	A
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.
- [3] Measured between all pins.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	236	272	K/W
			[2]	-	67	77	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	12	15	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

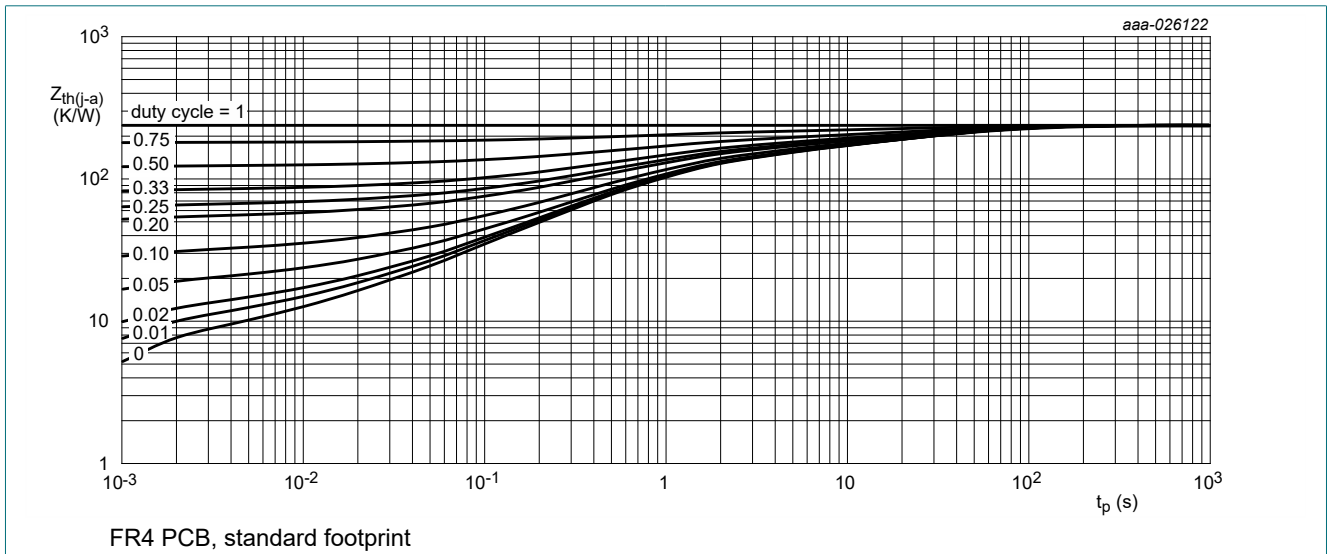


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

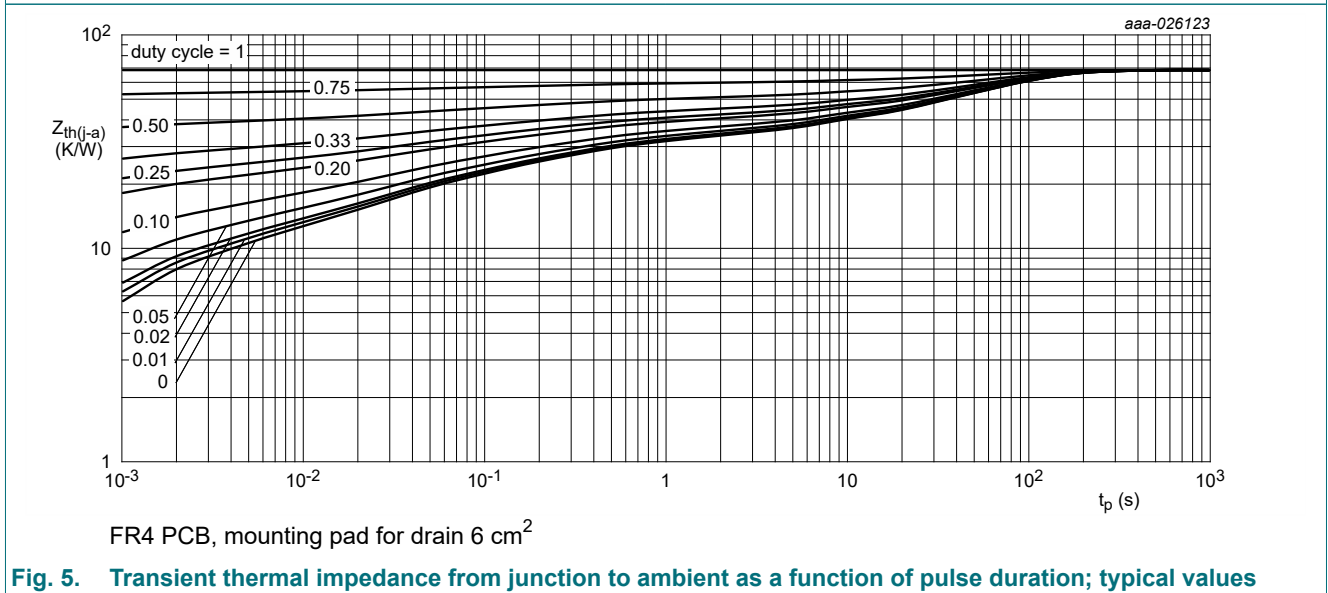


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	-0.75	-1	-1.25	V
I_{DSS}	drain leakage current	$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	μA
I_{GSS}	gate leakage current	$V_{GS} = -12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-10	μA
		$V_{GS} = 8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	5	μA
		$V_{GS} = -4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-2	μA
		$V_{GS} = 4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	2	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -3.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	100	122	m Ω
		$V_{GS} = -4.5 \text{ V}; I_D = -3.2 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$	-	157	191	m Ω
		$V_{GS} = -3 \text{ V}; I_D = -2.6 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	125	190	m Ω
g_{fs}	forward transconductance	$V_{DS} = -10 \text{ V}; I_D = -3.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	7	-	S
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	18.6	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 \text{ V}; I_D = -3.2 \text{ A}; V_{GS} = -4.5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	3.3	5	nC
Q_{GS}	gate-source charge		-	0.8	-	nC
Q_{GD}	gate-drain charge		-	0.8	-	nC
C_{iss}	input capacitance	$V_{DS} = -10 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	388	-	pF
C_{oss}	output capacitance		-	56	-	pF
C_{rss}	reverse transfer capacitance		-	39	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 \text{ V}; I_D = -2.6 \text{ A}; V_{GS} = -4.5 \text{ V}; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	5	-	ns
t_r	rise time		-	4	-	ns
$t_{d(off)}$	turn-off delay time		-	36	-	ns
t_f	fall time		-	17	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -1.9 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-0.9	-1.2	V
t_{rr}	reverse recovery time	$I_S = -1.9 \text{ A}; dI_S/dt = 100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = -10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	13.7	-	ns
Q_r	recovered charge		-	4.5	-	nC

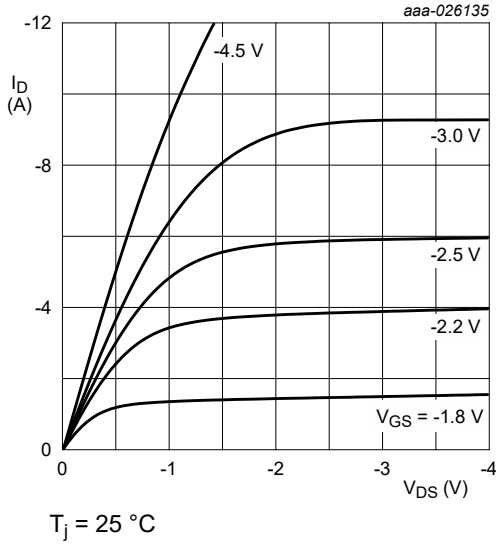


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

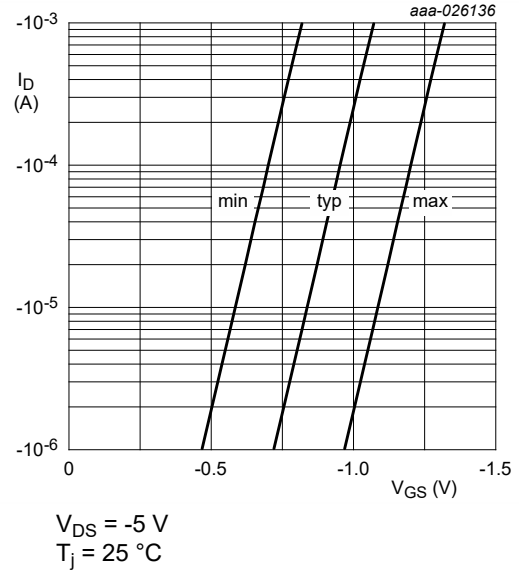


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

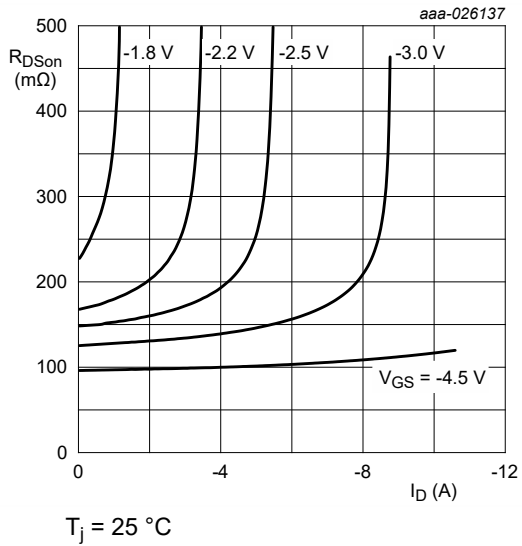


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

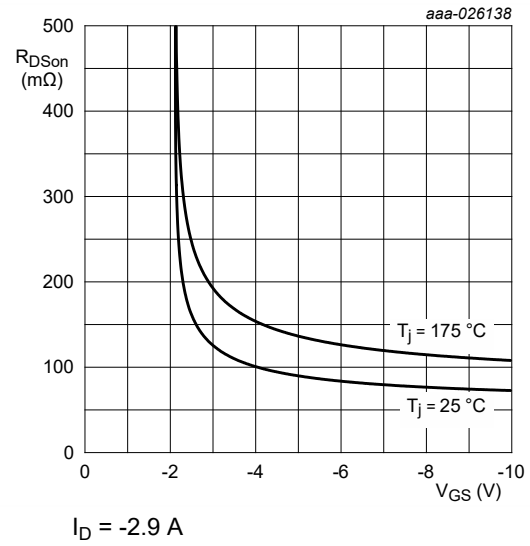
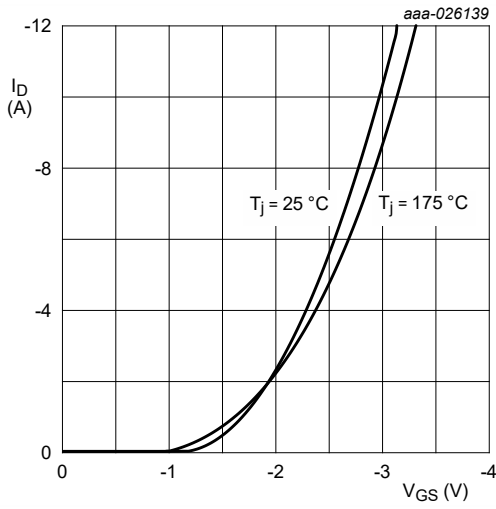
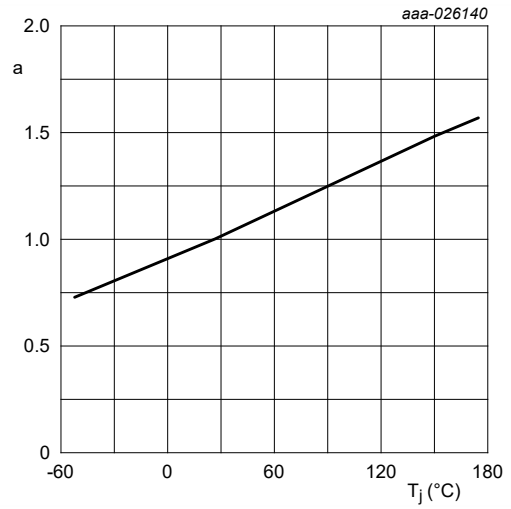


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



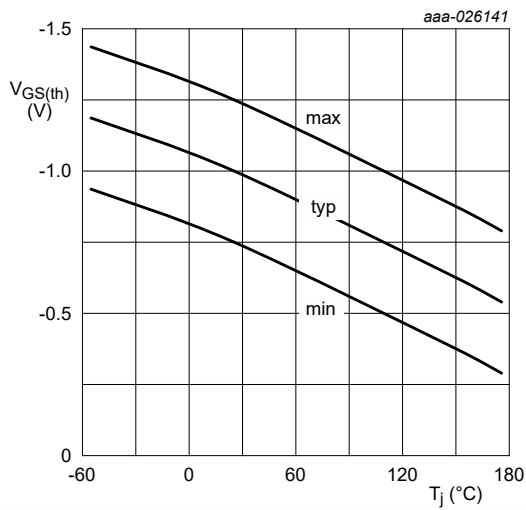
$$V_{DS} > I_D \times R_{DSon}$$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



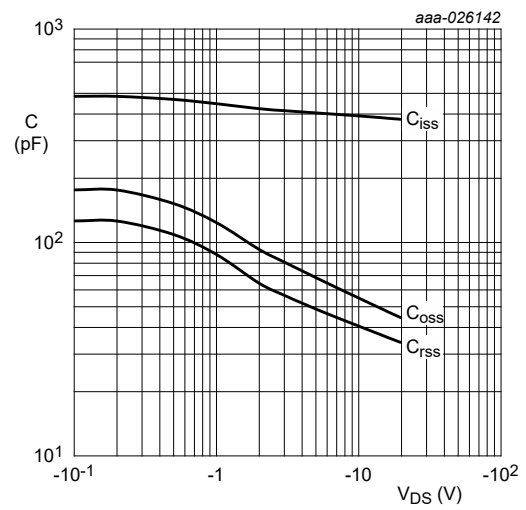
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



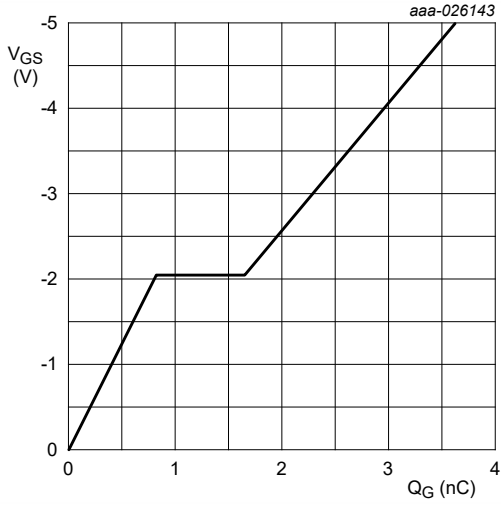
$$I_D = -250 \mu\text{A}; V_{DS} = V_{GS}$$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = -10\text{ V}; I_D = -3.2\text{ A}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

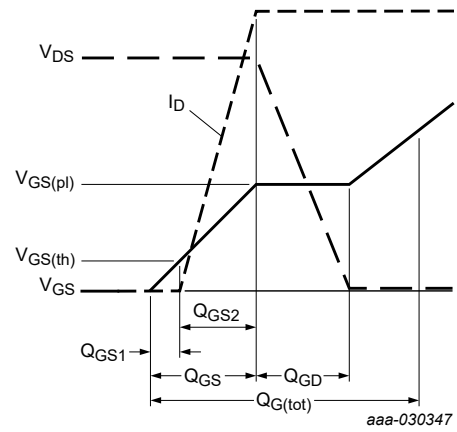
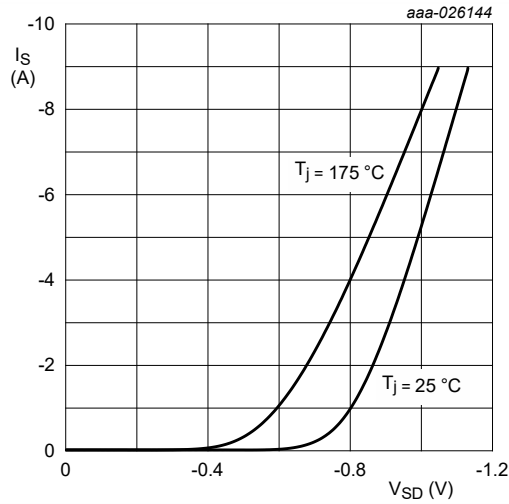


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

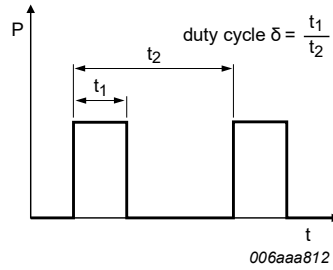


Fig. 17. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads;
6 terminals; body 2 x 2 x 0.65 mm

SOT1220

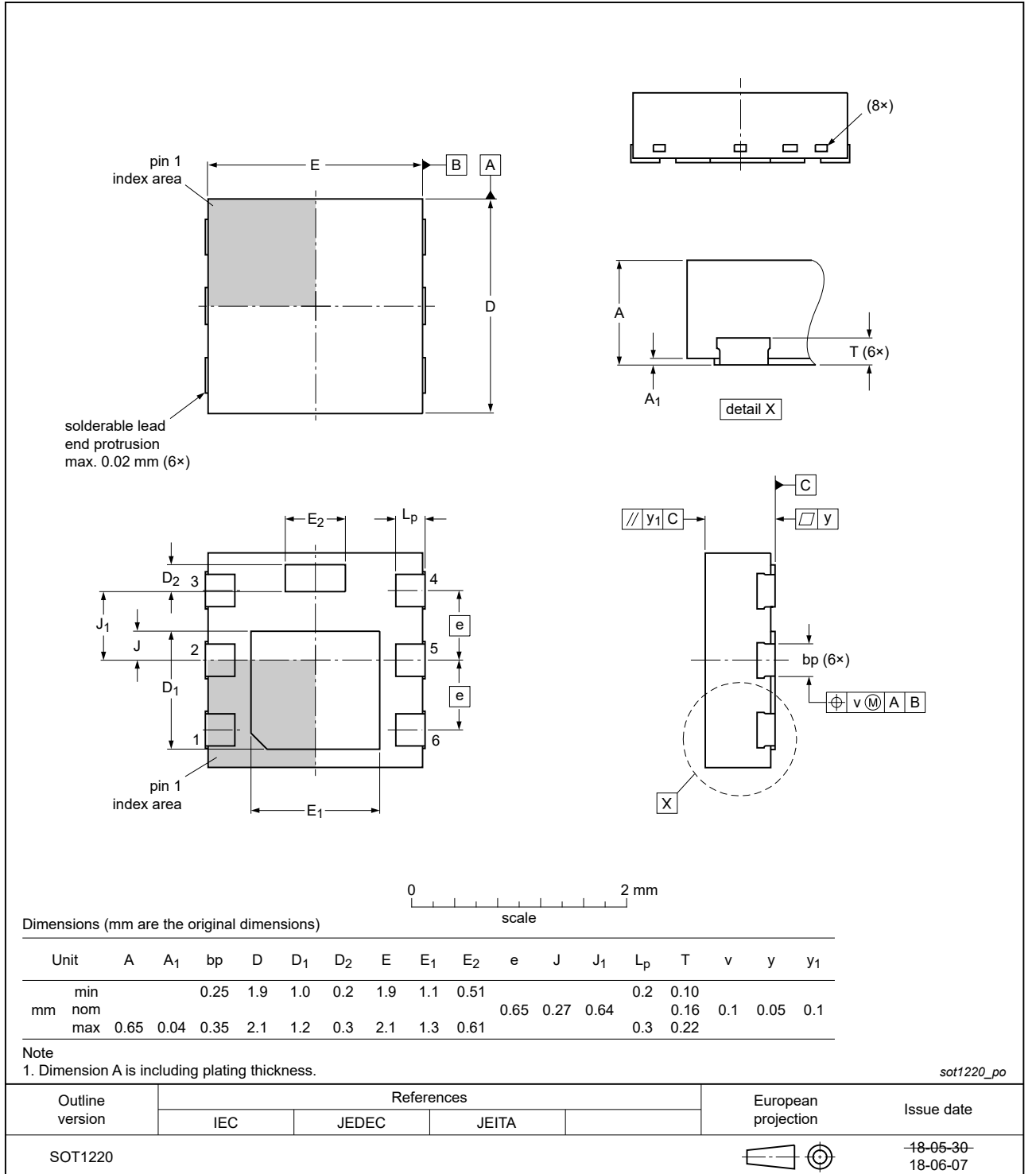


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

13. Soldering

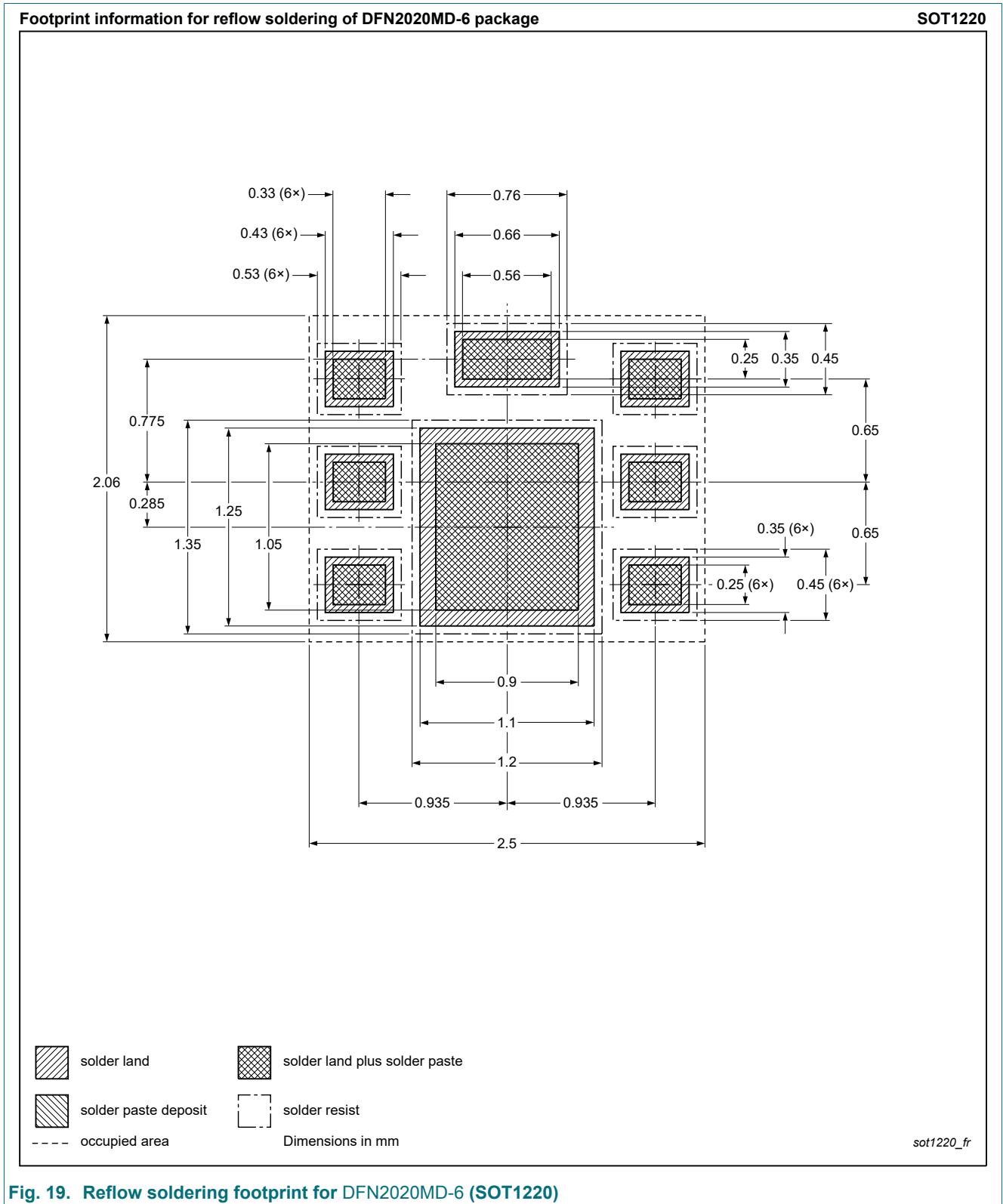


Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK4D122-20P v.2	20230327	Product data sheet	-	BUK4D122-20P v.1
Modifications:	• Complete rework			
BUK4D122-20P v.1	20200708	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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