
# PSMN9R3-60HS

## N-channel 60 V, 9.3 mOhm, standard level MOSFET in LFPAK56D using TrenchMOS technology

26 September 2022 Product data sheet

## 1. General description

Dual standard level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using TrenchMOS technology.

## 2. Features and benefits

- Dual MOSFET
- Repetitive avalanche rated
- High reliability LFPAK56D package
- Copper-clip, solder die attach
- Qualified to 175 °C

## 3. Applications

- Brushless DC motor control
- DC-to-DC converters
- High-performance synchronous rectification
- High performance and high efficiency server power supply

## 4. Quick reference data

**Table 1. Quick reference data**

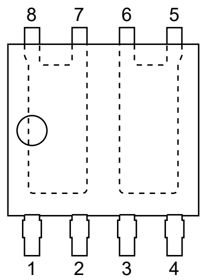
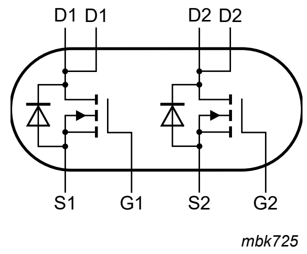
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | - | 60 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | - | 40 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 68 | W |
| $T_j$ | junction temperature | | | -55 | - | 175 | °C |
| **Static characteristics FET1 and FET2** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 10 A; $T_j$ = 25 °C; Fig. 11 | | - | 7.64 | 9.3 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 10 A; $T_j$ = 175 °C; Fig. 11; Fig. 12 | | - | 17.1 | 20.8 | mΩ |
| **Dynamic characteristics FET1 and FET2** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 10 A; $V_{DS}$ = 48 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | - | 11 | - | nC |
| $Q_{G(tot)}$ | total gate charge | | | - | 34.2 | - | nC |
| **Avalanche ruggedness FET1 and FET2** | | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 40 A; $V_{sup}$ ≤ 60 V; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; Fig. 4 | [2] [3] | - | - | 103 | mJ |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Source-drain diode FET1 and FET2** | | | | | | | |
| $Q_r$ | recovered charge | $I_S$ = 10 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 30 V; $T_j$ = 25 °C | | - | 24 | - | nC |

[1] Continuous current is limited by package.
[2] Refer to application note AN10273 for further information
[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

# 5. Pinning information

### Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S1 | source1 |  |  |
| 2 | G1 | gate1 | | |
| 3 | S2 | source2 | | |
| 4 | G2 | gate2 | | |
| 5 | D2 | drain2 | | |
| 6 | D2 | drain2 | | |
| 7 | D1 | drain1 | | |
| 8 | D1 | drain1 | **LFPAK56D; Dual LFPAK (SOT1205)** | |

# 6. Ordering information

### Table 3. Ordering information

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMN9R3-60HS | LFPAK56D; Dual LFPAK | plastic, single ended surface mounted package (LFPAK56D); 8 leads | SOT1205 |

# 7. Marking

### Table 4. Marking codes

| Type number | Marking code |
|---|---|
| PSMN9R3-60HS | 9R3S60H |

# 8. Limiting values

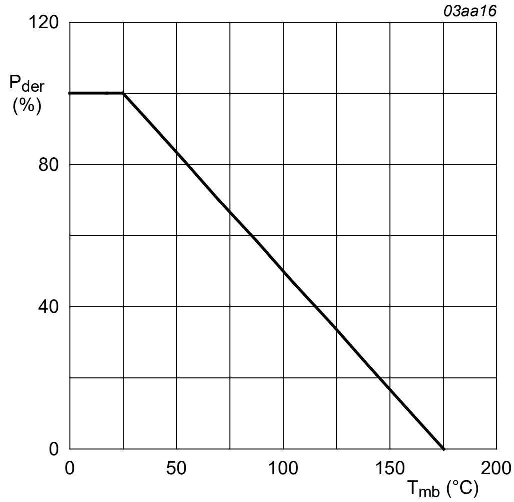
### Table 5. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | 60 | V |
| $V_{DGR}$ | drain-gate voltage | $R_{GS}$ = 20 kΩ | | - | 60 | V |
| $V_{GS}$ | gate-source voltage | DC; $T_j$ ≤ 175 °C | | -20 | 20 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 68 | W |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | 40 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; Fig. 2 | [1] | - | 40 | A |

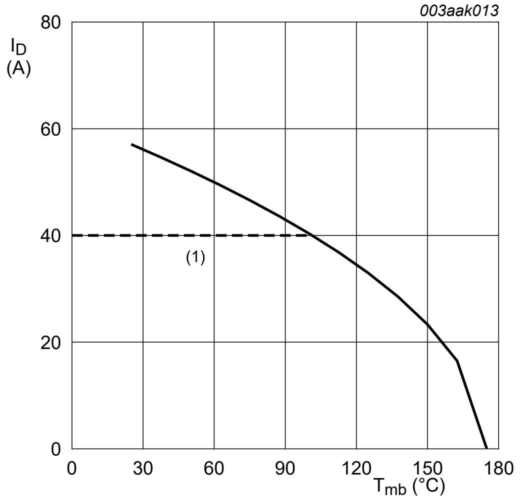
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DM}$ | peak drain current | pulsed; $t_p \leq$ 10 µs; $T_{mb}$ = 25 °C; Fig. 3 | | - | 228 | A |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| **Source-drain diode FET1 and FET2** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | [1] | - | 40 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p \leq$ 10 µs; $T_{mb}$ = 25 °C | | - | 228 | A |
| **Avalanche ruggedness FET1 and FET2** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 40 A; $V_{sup} \leq$ 60 V; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; Fig. 4 | [2] [3] | - | 103 | mJ |

[1] Continuous current is limited by package.
[2] Refer to application note AN10273 for further information
[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



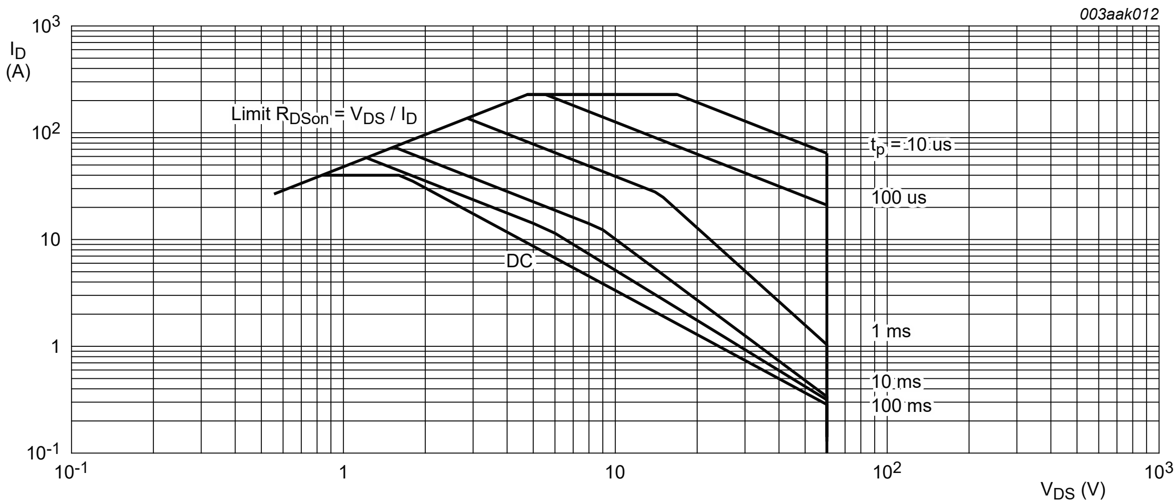

$$P_{der} = \frac{P_{tot}}{P_{tot(25\,°C)}} \times 100\,\%$$

**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**



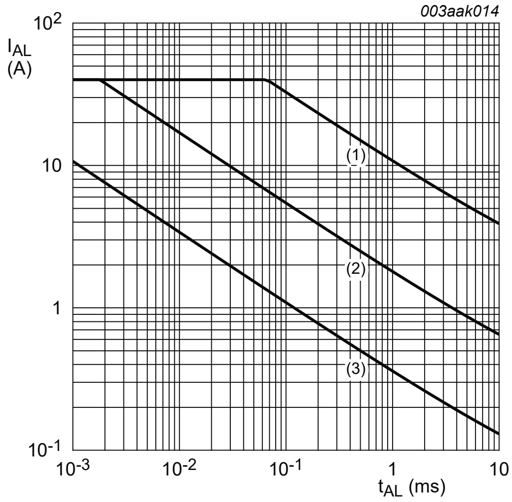

(1) Capped at 40 A due to package
$V_{GS} \geq$ 10 V

**Fig. 2. Continuous drain current as a function of mounting base temperature**




$T_{mb}$ = 25 °C; $I_{DM}$ is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**




(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

**Fig. 4. Avalanche rating; avalanche current as a function of avalanche time**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | | - | - | 2.21 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Minimum footprint; mounted on a printed circuit board | | - | 95 | - | K/W |

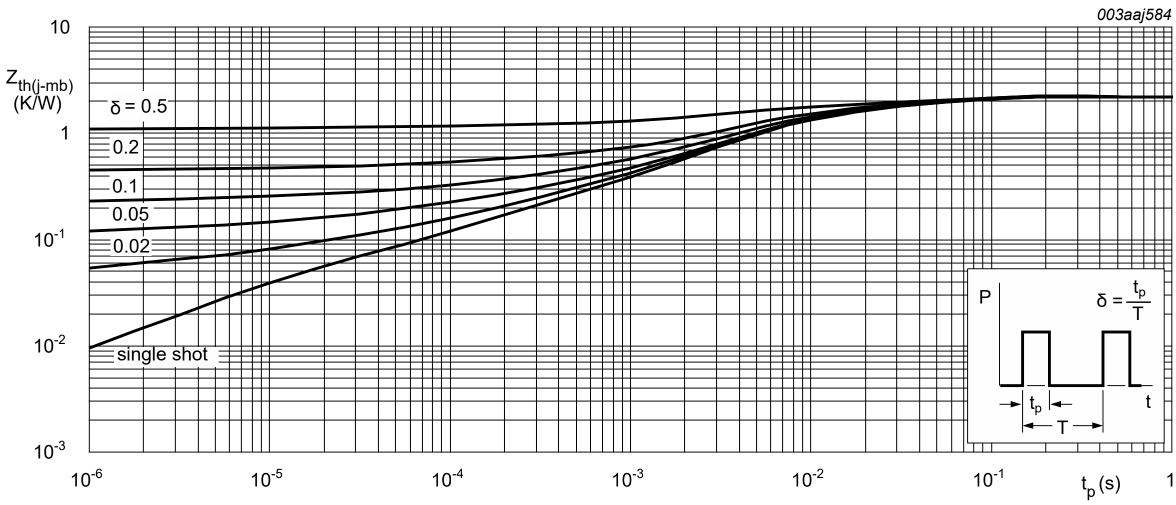
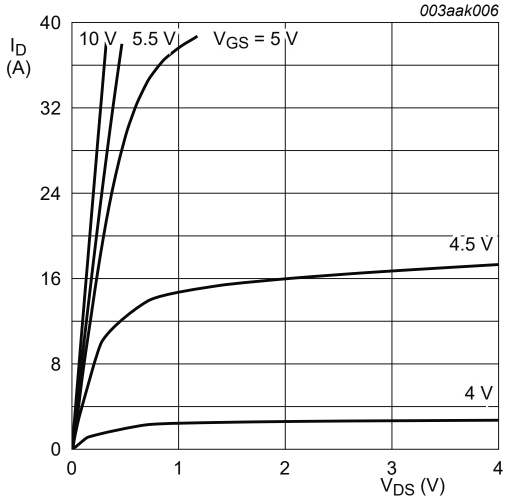



**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 10. Characteristics

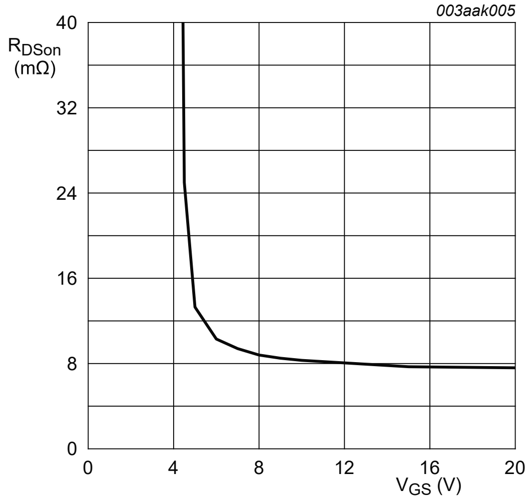
**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics FET1 and FET2** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 54 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 60 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 25 °C; Fig. 9; Fig. 10 | | 2.4 | 3 | 4 | V |
| | | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 175 °C; Fig. 9; Fig. 10 | | 1 | - | - | V |
| | | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = -55 °C; Fig. 9; Fig. 10 | | - | - | 4.5 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 60 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 0.02 | 1 | µA |
| | | $V_{DS}$ = 60 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C | | - | - | 500 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = -20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| | | $V_{GS}$ = 20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 10 A; $T_j$ = 25 °C; Fig. 11 | | - | 7.64 | 9.3 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 10 A; $T_j$ = 175 °C; Fig. 11; Fig. 12 | | - | 17.1 | 20.8 | mΩ |
| **Dynamic characteristics FET1 and FET2** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 10 A; $V_{DS}$ = 48 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | - | 34.2 | - | nC |
| $Q_{GS}$ | gate-source charge | | | - | 6.7 | - | nC |
| $Q_{GD}$ | gate-drain charge | | | - | 11 | - | nC |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 25 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 15 | | - | 1761 | 2348 | pF |
| $C_{oss}$ | output capacitance | | | - | 247 | 297 | pF |
| $C_{rss}$ | reverse transfer capacitance | | | - | 155 | 213 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 48 V; $R_L$ = 5 Ω; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 5 Ω; $T_j$ = 25 °C | | - | 9.1 | - | ns |
| $t_r$ | rise time | | | - | 12.5 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 23 | - | ns |
| $t_f$ | fall time | | | - | 15 | - | ns |
| **Source-drain diode FET1 and FET2** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 10 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 16 | | - | 0.78 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 10 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 30 V; $T_j$ = 25 °C | | - | 25 | - | ns |
| $Q_r$ | recovered charge | | | - | 24 | - | nC |



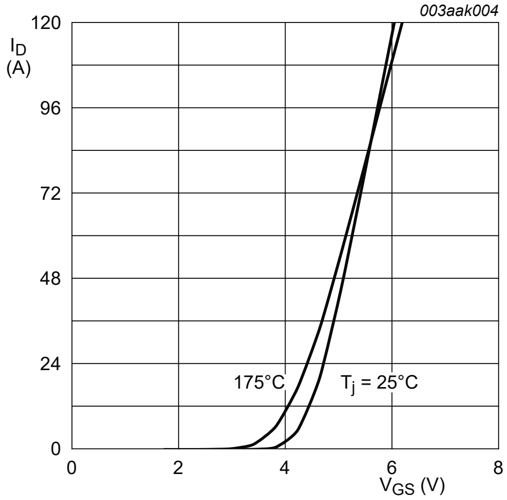

$T_j$ = 25 °C; $t_p$ = 300 µs

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



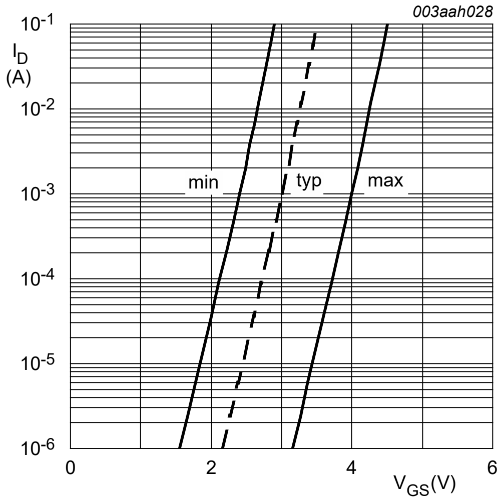

$T_j$ = 25 °C; $I_D$ = 10 A

**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**



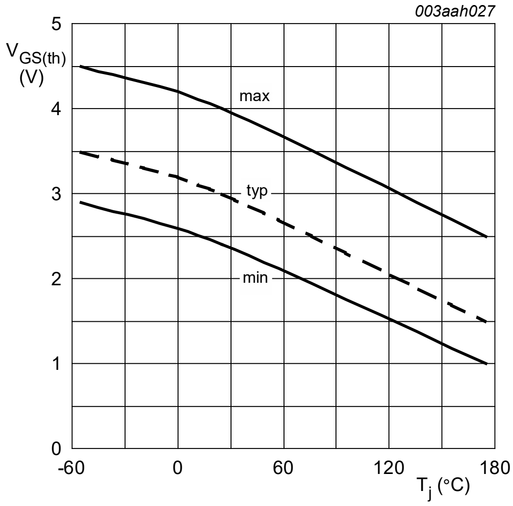

$V_{DS}$ = 10 V

**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



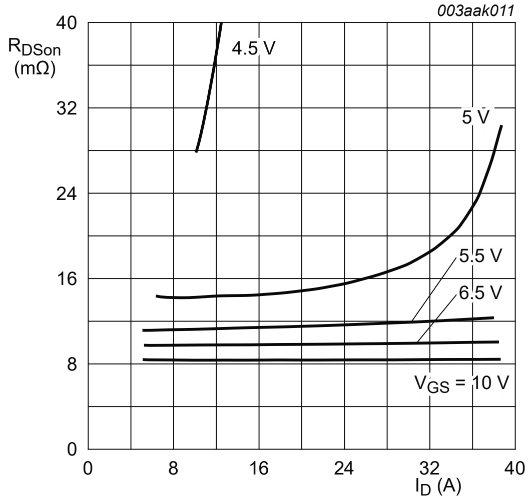

$T_j$ = 25 °C; $V_{DS}$ = 5 V

**Fig. 9. Sub-threshold drain current as a function of gate-source voltage**



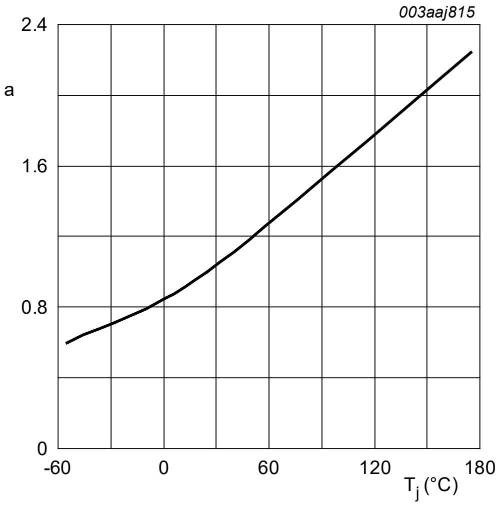

$I_D$ = 1 mA; $V_{DS} = V_{GS}$

**Fig. 10. Gate-source threshold voltage as a function of junction temperature**




$T_j$ = 25 °C; $t_p$ = 300 μs

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**




$$a = \frac{R_{DSon}}{R_{DSon\ (25°C)}}$$

**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

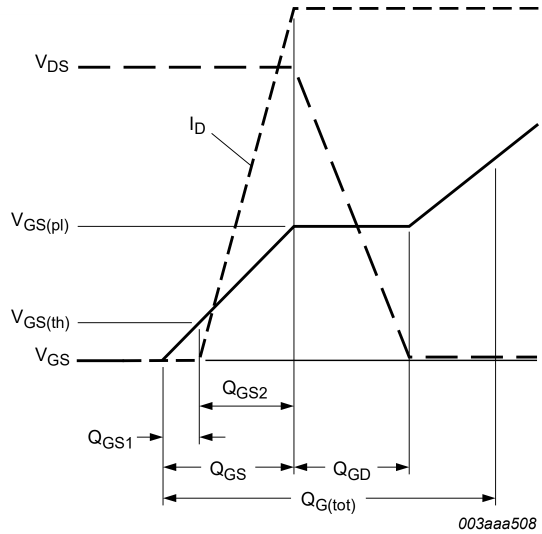
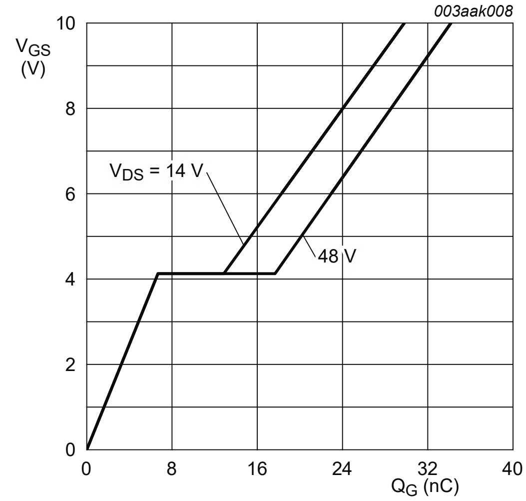
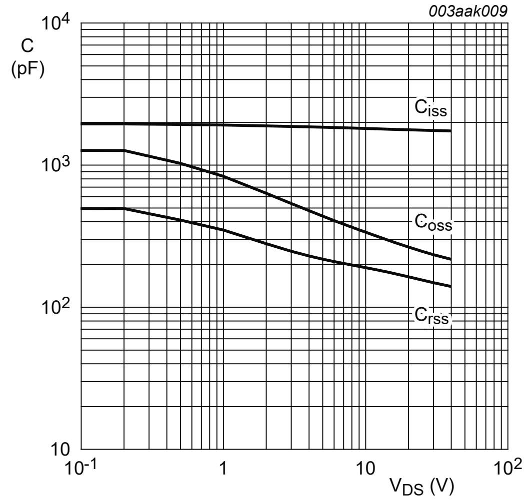



**Fig. 13. Gate charge waveform definitions**



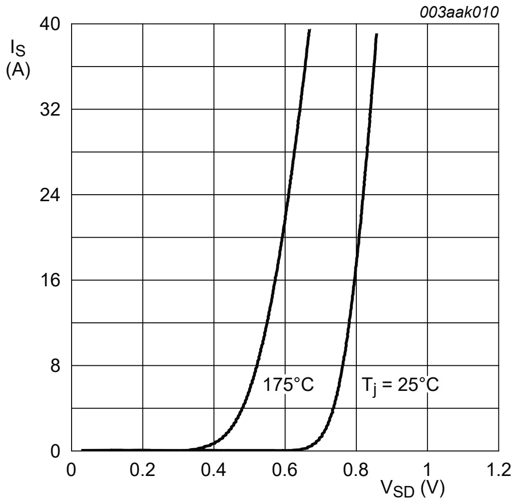

$T_j$ = 25 °C; $I_D$ = 10 A

**Fig. 14. Gate-source voltage as a function of gate charge; typical values**




$V_{GS}$ = 0 V; $I_D$ = 10 A

**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

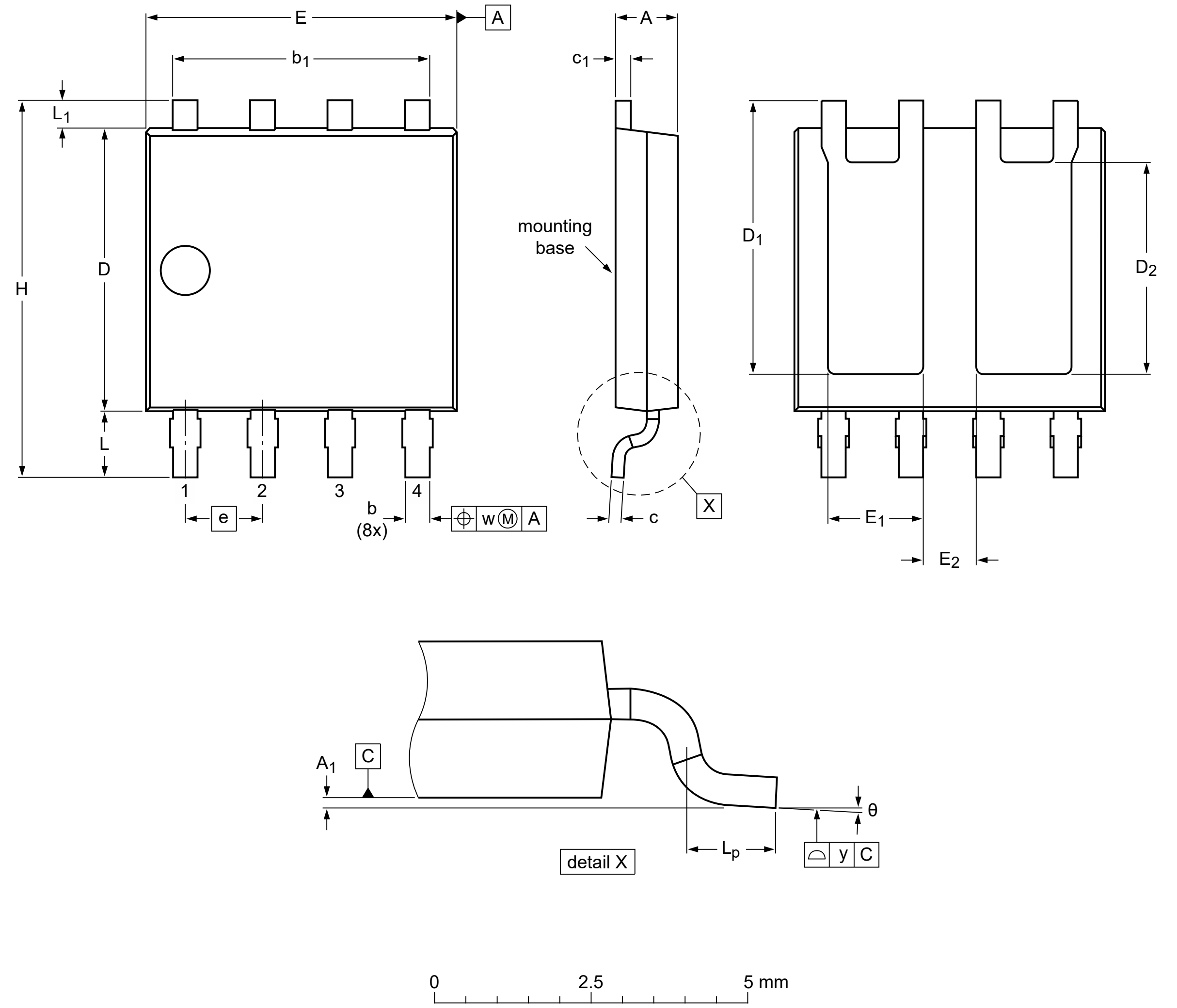



$V_{GS}$ = 0 V

**Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

## 11. Package outline

**Plastic single ended surface mounted package LFPAK56D; 8 leads** **SOT1205**




Dimensions

| Unit | | A | $A_1$ | b | $b_1$ | c | $c_1$ | D(1) | $D_1$(1) | $D_2$ (ref) | E(1) | $E_1$(1) | $E_2$ | e | H | L | $L_1$ | $L_p$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.05 | 0.1 | 0.50 | 4.4 | 0.25 | 0.30 | 4.70 | 4.55 | 3.5 | 5.30 | 1.8 | 0.85 | | 6.2 | 1.3 | 0.55 | 0.85 | | | 8° |
| | nom | | | | | | | | | | | | | 1.27 | | | | | 0.25 | 0.1 | |
| | min | 1.02 | 0.0 | 0.35 | 4.1 | 0.19 | 0.24 | 4.45 | 4.35 | 3.4 | 4.95 | 1.6 | 0.60 | | 5.9 | 0.8 | 0.30 | 0.40 | | | 0° |

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

*sot1205_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1205 | | | | | | ~~14-08-21~~<br>14-10-28 |

**Fig. 17. Package outline LFPAK56D; Dual LFPAK (SOT1205)**

## 12. Soldering

**Footprint information for reflow soldering of LFPAK56D package** **SOT1205**

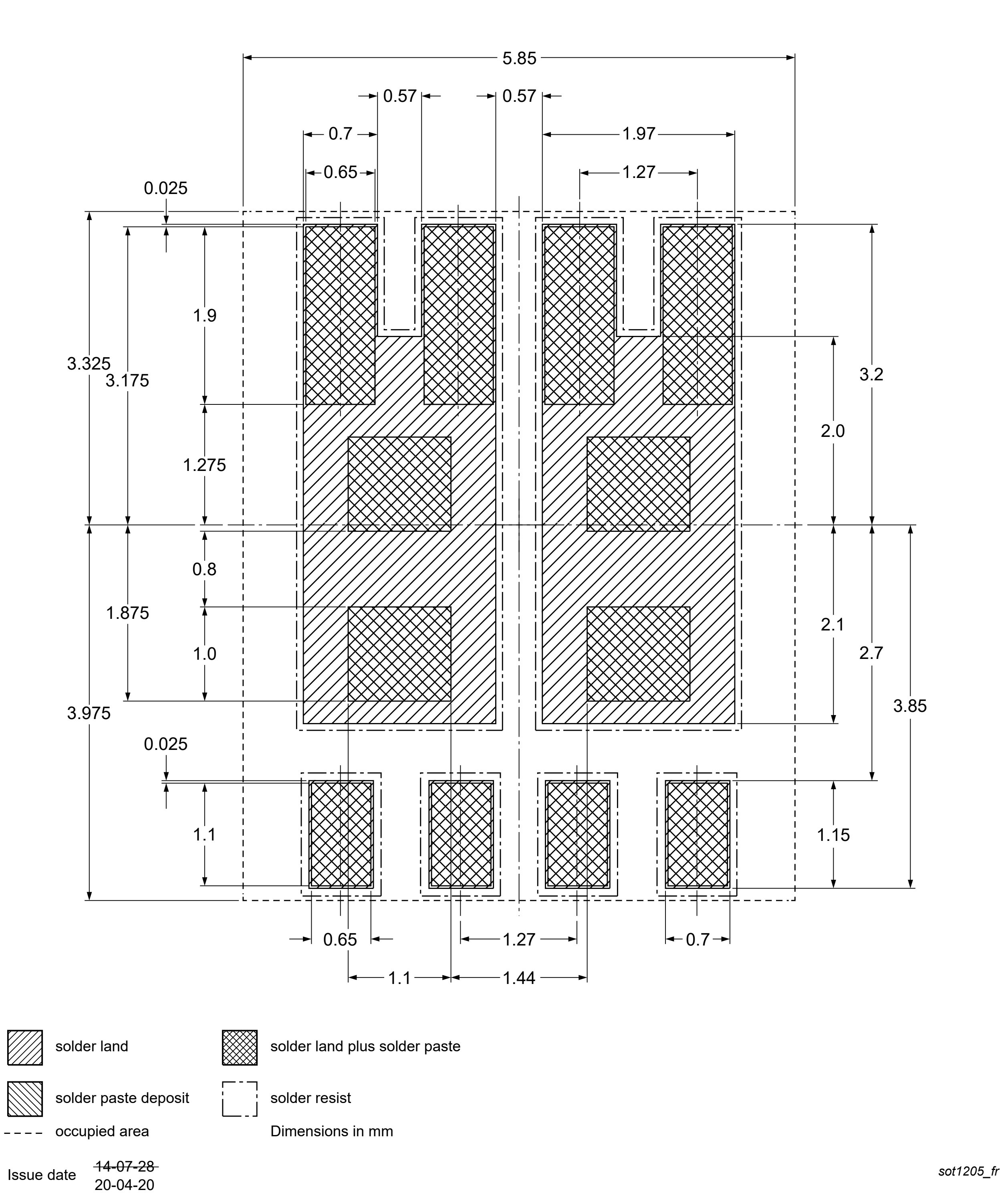



**Fig. 18. Reflow soldering footprint for LFPAK56D; Dual LFPAK (SOT1205)**

# 13. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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