

74AUP2G08

Low-power dual 2-input AND gate

Rev. 12 — 19 July 2023

Product data sheet

1. General description

The 74AUP2G08 is a dual 2-input AND gate. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- CMOS low power dissipation
- Low static power consumption; $I_{CC} = 0.9 \mu\text{A}$ (maximum)
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Overvoltage tolerant inputs to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AUP2G08DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AUP2G08GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74AUP2G08GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74AUP2G08GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203
74AUP2G08GX	-40 °C to +125 °C	X2SON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 × 0.8 × 0.32 mm	SOT1233-2

4. Marking

Table 2. Marking

Type number	Marking code[1]
74AUP2G08DC	p08
74AUP2G08GT	p08
74AUP2G08GN	pE
74AUP2G08GS	pE
74AUP2G08GX	pE

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

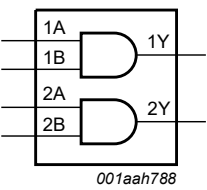


Fig. 1. Logic symbol

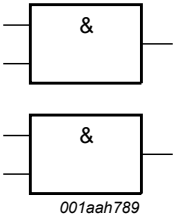


Fig. 2. IEC logic symbol

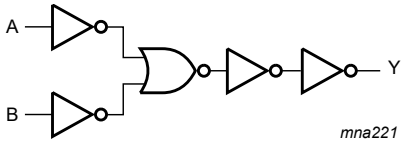
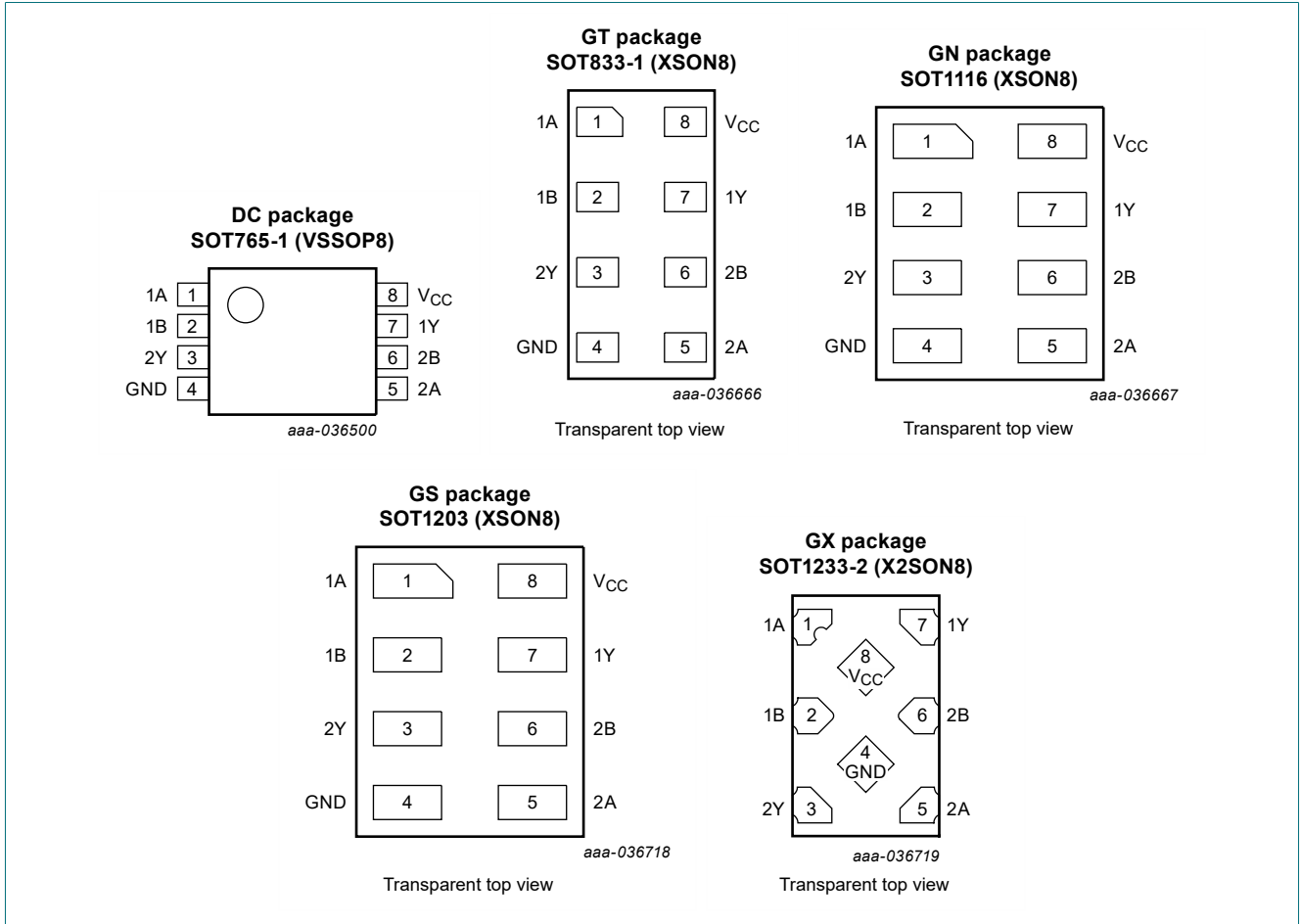


Fig. 3. Logic diagram (one gate)

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage		[1] -0.5	+4.6	V
V_O	output voltage	Active mode and Power-down mode	[1] -0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0\text{ V}$	-50	-	mA
I_{OK}	output clamping current	$V_O < 0\text{ V}$	-50	-	mA
I_O	output current	$V_O = 0\text{ V to }V_{CC}$	-	±20	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$			
		SOT765-1 (VSSOP8) SOT833-1 (XSON8) SOT1116 (XSON8) SOT1203 (XSON8)	[2] -	250	mW
		SOT1233-2 (X2SON8)	[3] -	300	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

For SOT833-1 (XSON8) package: P_{tot} derates linearly with 3.1 mW/K above 68 °C.

For SOT1116 (XSON8) package: P_{tot} derates linearly with 4.2 mW/K above 90 °C.

For SOT1203 (XSON8) package: P_{tot} derates linearly with 3.6 mW/K above 81 °C.

[3] For SOT1233-2 (X2SON8) package: P_{tot} derates linearly with 7.7 mW/K above 118 °C.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.8$ V to 3.6 V	-	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 0.8$ V	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.6	-	-	V
		$V_{CC} = 3.0$ V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 0.8$ V	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 3.0$ V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20$ μ A; $V_{CC} = 0.8$ V to 3.6 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -1.1$ mA; $V_{CC} = 1.1$ V	$0.75 \times V_{CC}$	-	-	V
		$I_O = -1.7$ mA; $V_{CC} = 1.4$ V	1.11	-	-	V
		$I_O = -1.9$ mA; $V_{CC} = 1.65$ V	1.32	-	-	V
		$I_O = -2.3$ mA; $V_{CC} = 2.3$ V	2.05	-	-	V
		$I_O = -3.1$ mA; $V_{CC} = 2.3$ V	1.9	-	-	V
		$I_O = -2.7$ mA; $V_{CC} = 3.0$ V	2.72	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 3.0$ V	2.6	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20$ μ A; $V_{CC} = 0.8$ V to 3.6 V	-	-	0.1	V
		$I_O = 1.1$ mA; $V_{CC} = 1.1$ V	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7$ mA; $V_{CC} = 1.4$ V	-	-	0.31	V
		$I_O = 1.9$ mA; $V_{CC} = 1.65$ V	-	-	0.31	V
		$I_O = 2.3$ mA; $V_{CC} = 2.3$ V	-	-	0.31	V
		$I_O = 3.1$ mA; $V_{CC} = 2.3$ V	-	-	0.44	V
		$I_O = 2.7$ mA; $V_{CC} = 3.0$ V	-	-	0.31	V
		$I_O = 4.0$ mA; $V_{CC} = 3.0$ V	-	-	0.44	V
I_I	input leakage current	$V_I = \text{GND}$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	± 0.1	μ A
I_{OFF}	power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	± 0.2	μ A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔI_{OFF}	additional power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	± 0.2	μ A
I_{CC}	supply current	$V_I = GND$ or V_{CC} ; $I_O = 0$ A; $V_{CC} = 0.8$ V to 3.6 V	-	-	0.5	μ A
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 3.3$ V; per pin [1]	-	-	40	μ A
C_I	input capacitance	$V_{CC} = 0$ V to 3.6 V; $V_I = GND$ or V_{CC}	-	0.6	-	pF
C_O	output capacitance	$V_O = GND$; $V_{CC} = 0$ V	-	1.3	-	pF
$T_{amb} = -40$ °C to $+85$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 0.8$ V	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.6	-	-	V
		$V_{CC} = 3.0$ V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 0.8$ V	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 3.0$ V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20$ μ A; $V_{CC} = 0.8$ V to 3.6 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -1.1$ mA; $V_{CC} = 1.1$ V	$0.7 \times V_{CC}$	-	-	V
		$I_O = -1.7$ mA; $V_{CC} = 1.4$ V	1.03	-	-	V
		$I_O = -1.9$ mA; $V_{CC} = 1.65$ V	1.30	-	-	V
		$I_O = -2.3$ mA; $V_{CC} = 2.3$ V	1.97	-	-	V
		$I_O = -3.1$ mA; $V_{CC} = 2.3$ V	1.85	-	-	V
		$I_O = -2.7$ mA; $V_{CC} = 3.0$ V	2.67	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 3.0$ V	2.55	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20$ μ A; $V_{CC} = 0.8$ V to 3.6 V	-	-	0.1	V
		$I_O = 1.1$ mA; $V_{CC} = 1.1$ V	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7$ mA; $V_{CC} = 1.4$ V	-	-	0.37	V
		$I_O = 1.9$ mA; $V_{CC} = 1.65$ V	-	-	0.35	V
		$I_O = 2.3$ mA; $V_{CC} = 2.3$ V	-	-	0.33	V
		$I_O = 3.1$ mA; $V_{CC} = 2.3$ V	-	-	0.45	V
		$I_O = 2.7$ mA; $V_{CC} = 3.0$ V	-	-	0.33	V
		$I_O = 4.0$ mA; $V_{CC} = 3.0$ V	-	-	0.45	V
I_I	input leakage current	$V_I = GND$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	± 0.5	μ A
I_{OFF}	power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	± 0.5	μ A
ΔI_{OFF}	additional power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	± 0.6	μ A
I_{CC}	supply current	$V_I = GND$ or V_{CC} ; $I_O = 0$ A; $V_{CC} = 0.8$ V to 3.6 V	-	-	0.9	μ A
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 3.3$ V; per pin [1]	-	-	50	μ A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.75 × V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.70 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.25 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.6 × V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	0.93	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.17	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.40	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.30	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.33 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.75	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	1.4	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V; per pin [1]	-	-	75	μA

[1] One input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_L = 5 pF										
t _{pd}	propagation delay	nA, nB to nY; see Fig. 4 [2]								
		V _{CC} = 0.8 V	-	17.0	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.6	5.1	10.8	2.1	11.7	2.1	12.9	ns
		V _{CC} = 1.4 V to 1.6 V	1.6	3.7	6.5	1.5	7.5	1.5	8.3	ns
		V _{CC} = 1.65 V to 1.95 V	1.3	3.0	5.2	1.3	6.1	1.3	6.7	ns
		V _{CC} = 2.3 V to 2.7 V	1.1	2.4	4.0	1.0	4.8	1.0	5.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.2	3.5	0.9	4.3	0.9	4.8	ns
C_L = 10 pF										
t _{pd}	propagation delay	nA, nB to nY; see Fig. 4 [2]								
		V _{CC} = 0.8 V	-	20.6	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.4	6.0	12.5	2.2	13.6	2.2	15.0	ns
		V _{CC} = 1.4 V to 1.6 V	2.0	4.3	7.6	1.8	8.9	1.8	9.8	ns
		V _{CC} = 1.65 V to 1.95 V	1.7	3.6	6.1	1.6	7.2	1.6	7.9	ns
		V _{CC} = 2.3 V to 2.7 V	1.4	2.9	4.8	1.3	5.7	1.3	6.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.3	2.7	4.2	1.2	4.7	1.2	5.2	ns
C_L = 15 pF										
t _{pd}	propagation delay	nA, nB to nY; see Fig. 4 [2]								
		V _{CC} = 0.8 V	-	24.1	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.4	6.8	14.2	3.1	15.7	3.1	17.3	ns
		V _{CC} = 1.4 V to 1.6 V	2.3	4.9	8.6	2.1	10.1	2.1	11.2	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	4.0	6.9	1.8	8.2	1.8	9.0	ns
		V _{CC} = 2.3 V to 2.7 V	1.7	3.4	5.5	1.6	6.5	1.6	7.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.1	4.8	1.5	5.9	1.5	6.5	ns
C_L = 30 pF										
t _{pd}	propagation delay	nA, nB to nY; see Fig. 4 [2]								
		V _{CC} = 0.8 V	-	34.4	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.6	9.1	19.4	4.1	21.8	4.1	24.0	ns
		V _{CC} = 1.4 V to 1.6 V	3.4	6.4	11.5	2.9	13.6	2.9	15.0	ns
		V _{CC} = 1.65 V to 1.95 V	2.6	5.3	9.1	2.4	10.9	2.4	12.1	ns
		V _{CC} = 2.3 V to 2.7 V	2.3	4.5	7.2	2.2	8.6	2.2	9.5	ns
		V _{CC} = 3.0 V to 3.6 V	2.2	4.2	6.2	2.1	7.5	2.1	8.3	ns

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_L = 5 pF, 10 pF, 15 pF and 30 pF										
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} [3]								
		V _{CC} = 0.8 V	-	2.5	-	-	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	2.6	-	-	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	2.7	-	-	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	2.8	-	-	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	3.2	-	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	3.7	-	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

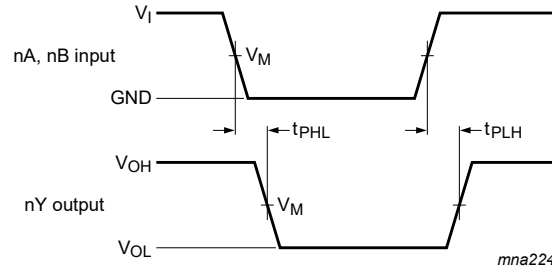
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of outputs.

11.1. Waveforms and test circuit



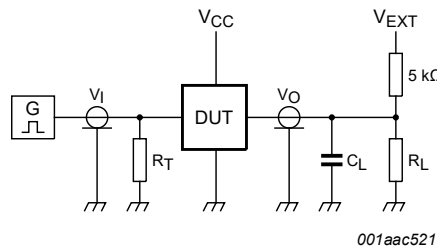
Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The data input (nA or nB) to output (nY) propagation delays

Table 9. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 5. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times $R_L = 5$ kΩ.

For measuring propagation delays, setup and hold times and pulse width $R_L = 1$ MΩ.

12. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

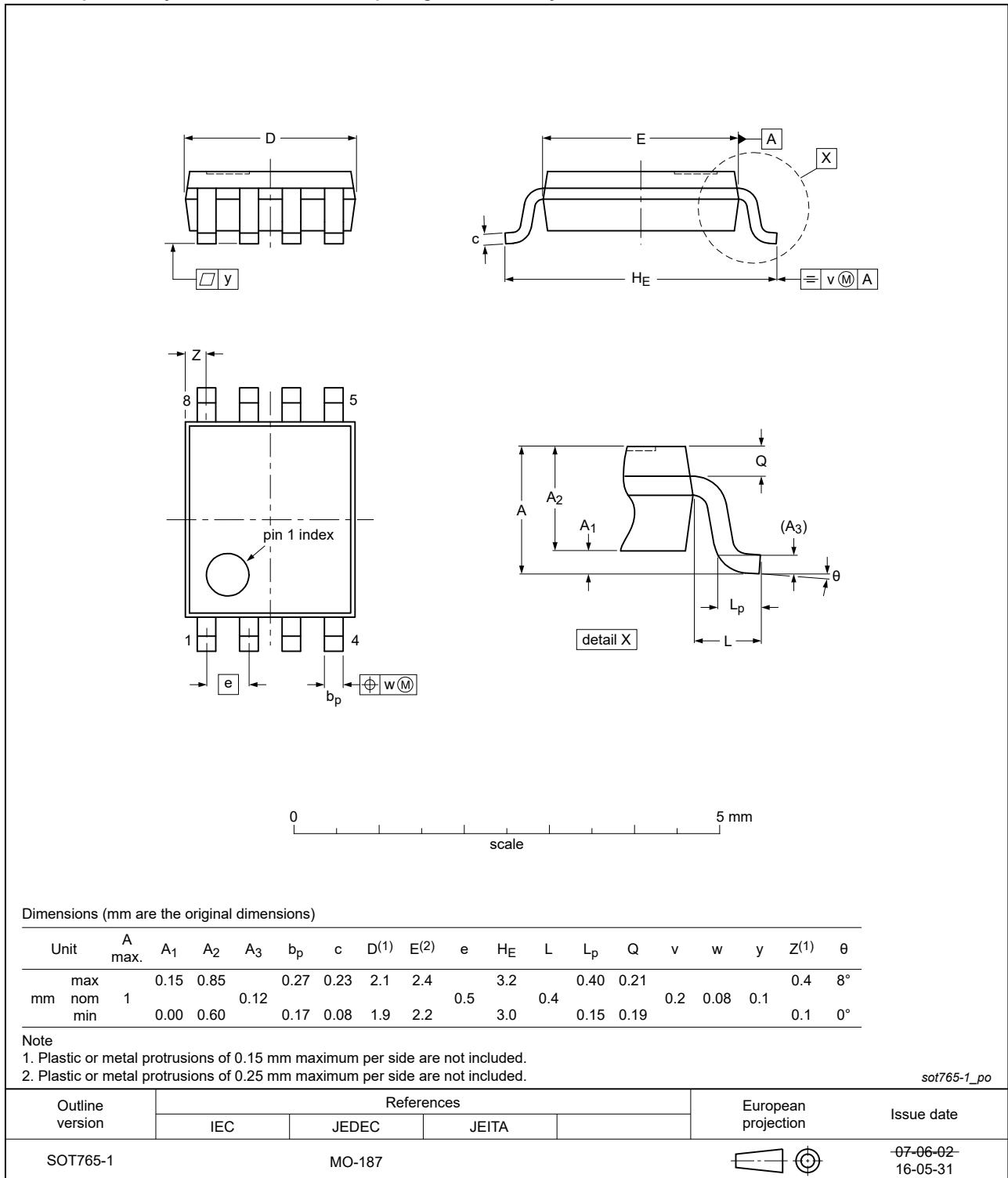


Fig. 6. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



Fig. 7. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116

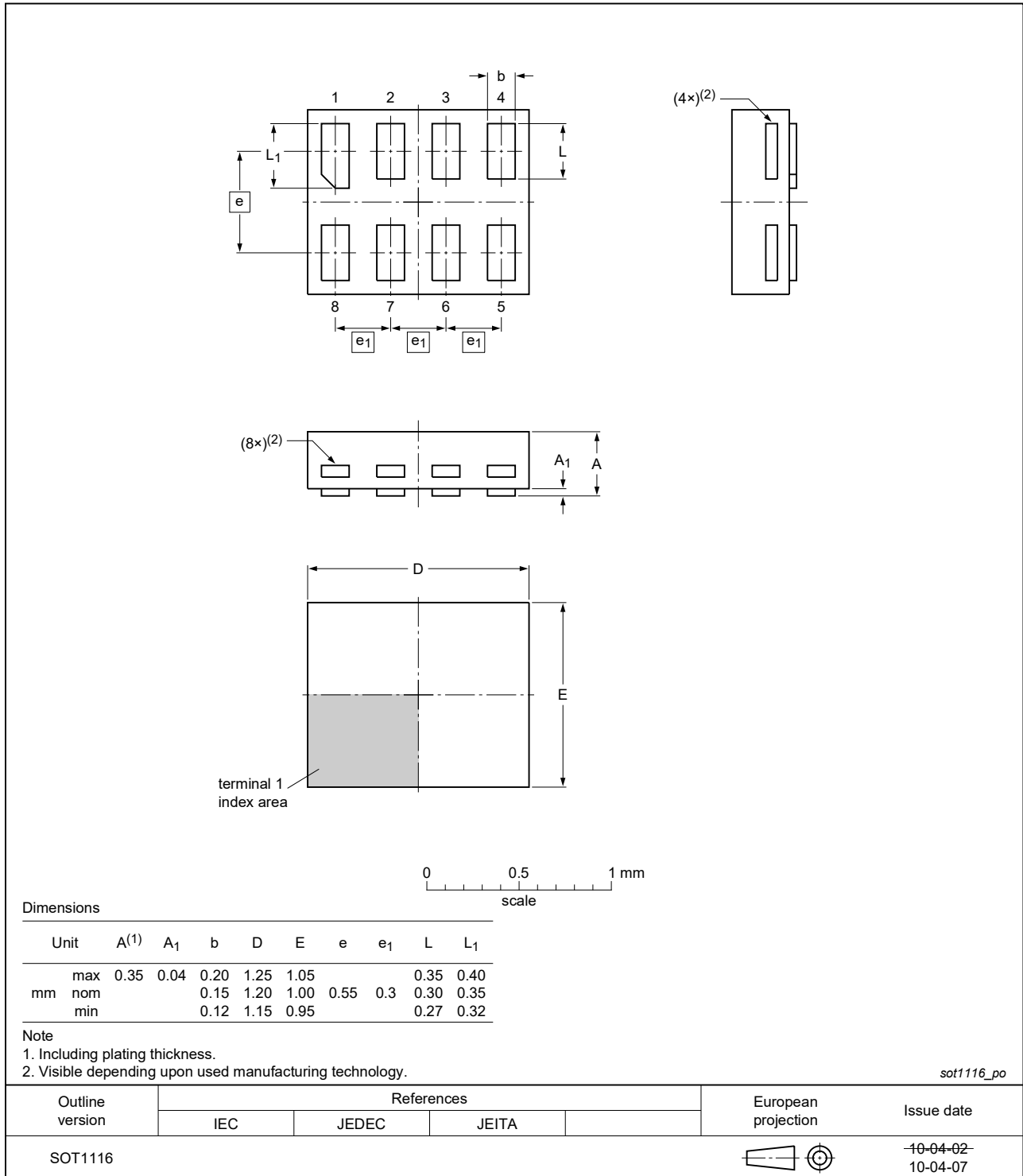


Fig. 8. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203

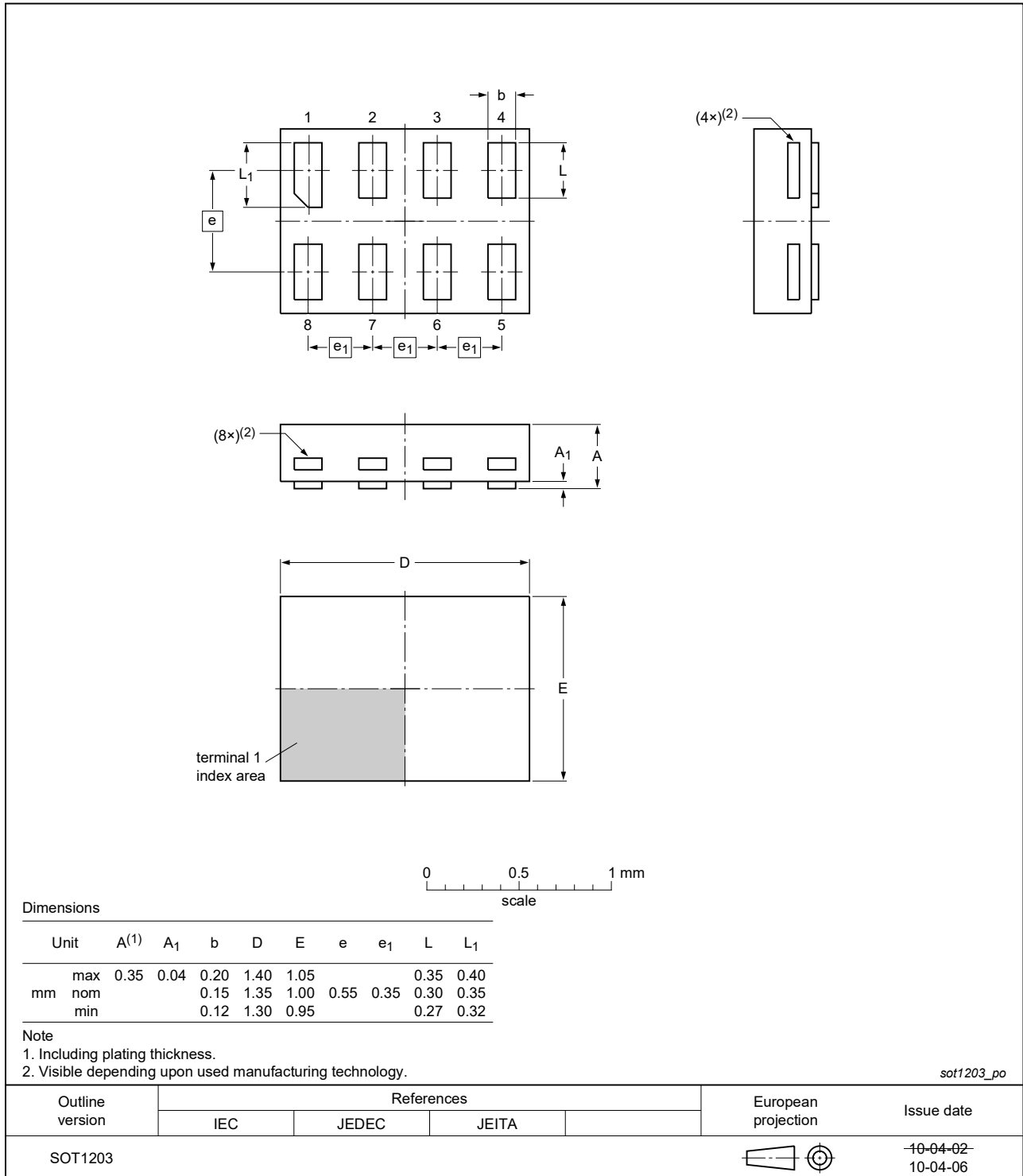


Fig. 9. Package outline SOT1203 (XSON8)

X2SON8: plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 x 0.8 x 0.32 mm

SOT1233-2

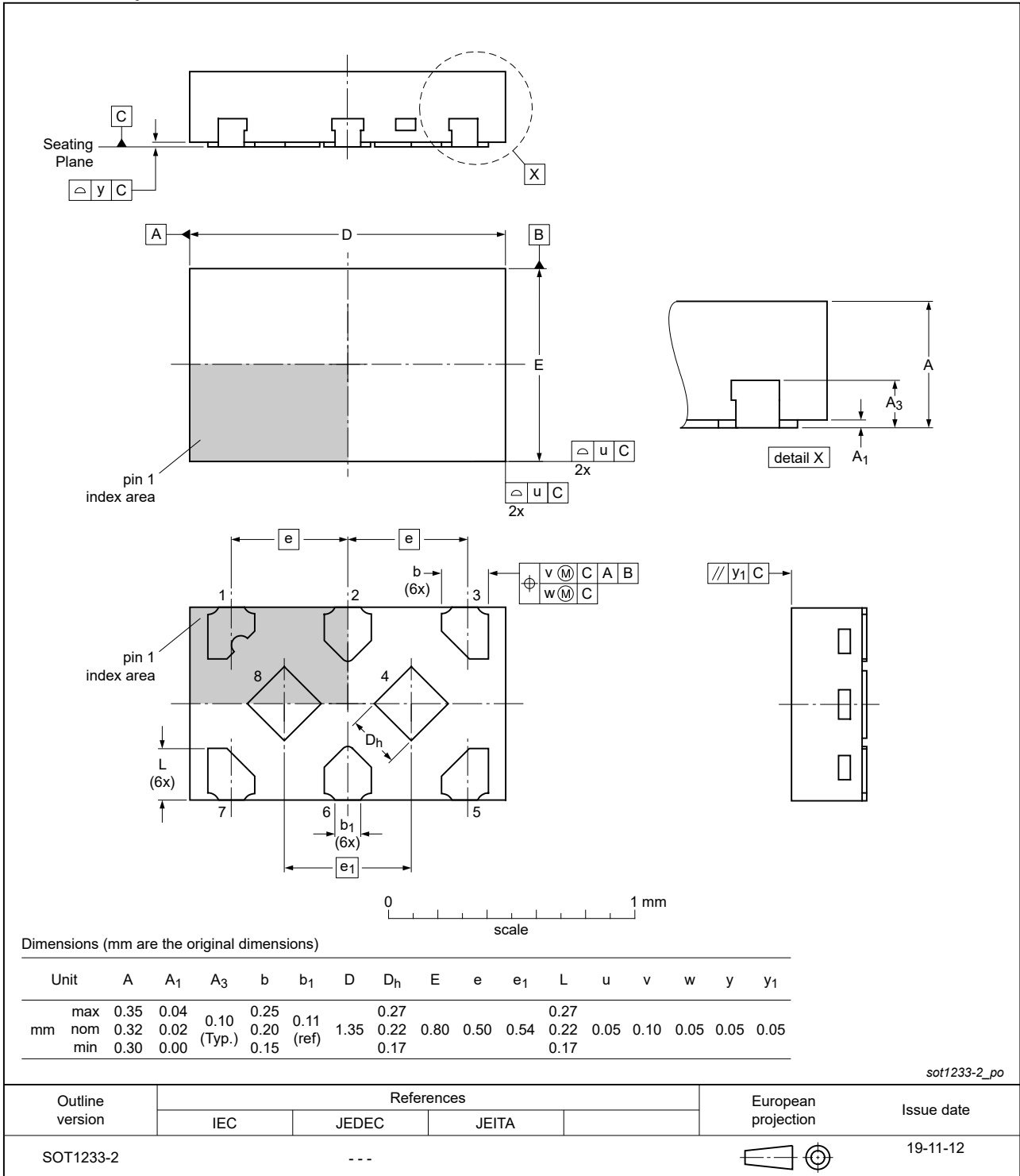


Fig. 10. Package outline SOT1233-2 (X2SON8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G08 v.12	20230719	Product data sheet	-	74AUP2G08 v.11
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. Type number 74AUP2G08GM (SOT902-2/XQFN8) removed. 			
74AUP2G08 v.11	20220617	Product data sheet	-	74AUP2G08 v.10
Modifications:	<ul style="list-style-type: none"> Package SOT1233 (X2SON8) changed to SOT1233-2 (X2SON8). 			
74AUP2G08 v.10	20220308	Product data sheet	-	74AUP2G08 v.9
Modifications:	<ul style="list-style-type: none"> Type number 74AUP2G08GF (SOT1089/XSON8) removed. Section 1 and Section 2 updated. Table 5: Derating values for P_{tot} total power dissipation have been updated. 			
74AUP2G08 v.9	20170703	Product data sheet	-	74AUP2G08 v.8
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 6.1 and Fig. 10 (drawings SOT1233/X2SON8) updated. Type number 74AUP2G08GD removed. 			
74AUP2G08 v.8	20161028	Product data sheet	-	74AUP2G08 v.7
Modifications:	<ul style="list-style-type: none"> Added type number 74AUP2G08GX (SOT1233/X2SON8) 			
74AUP2G08 v.7	20130118	Product data sheet	-	74AUP2G08 v.6
Modifications:	<ul style="list-style-type: none"> For type number 74AUP2G08GD XSON8U has changed to XSON8. 			
74AUP2G08 v.6	20120607	Product data sheet	-	74AUP2G08 v.5
74AUP2G08 v.5	20111201	Product data sheet	-	74AUP2G08 v.4
74AUP2G08 v.4	20101109	Product data sheet	-	74AUP2G08 v.3
74AUP2G08 v.3	20080529	Product data sheet	-	74AUP2G08 v.2
74AUP2G08 v.2	20080407	Product data sheet	-	74AUP2G08 v.1
74AUP2G08 v.1	20061006	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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