

74LV14A

Hex inverting Schmitt trigger

Rev. 5 — 8 April 2024

Product data sheet

1. General description

The 74LV14A is a hex inverter with Schmitt-trigger inputs, capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

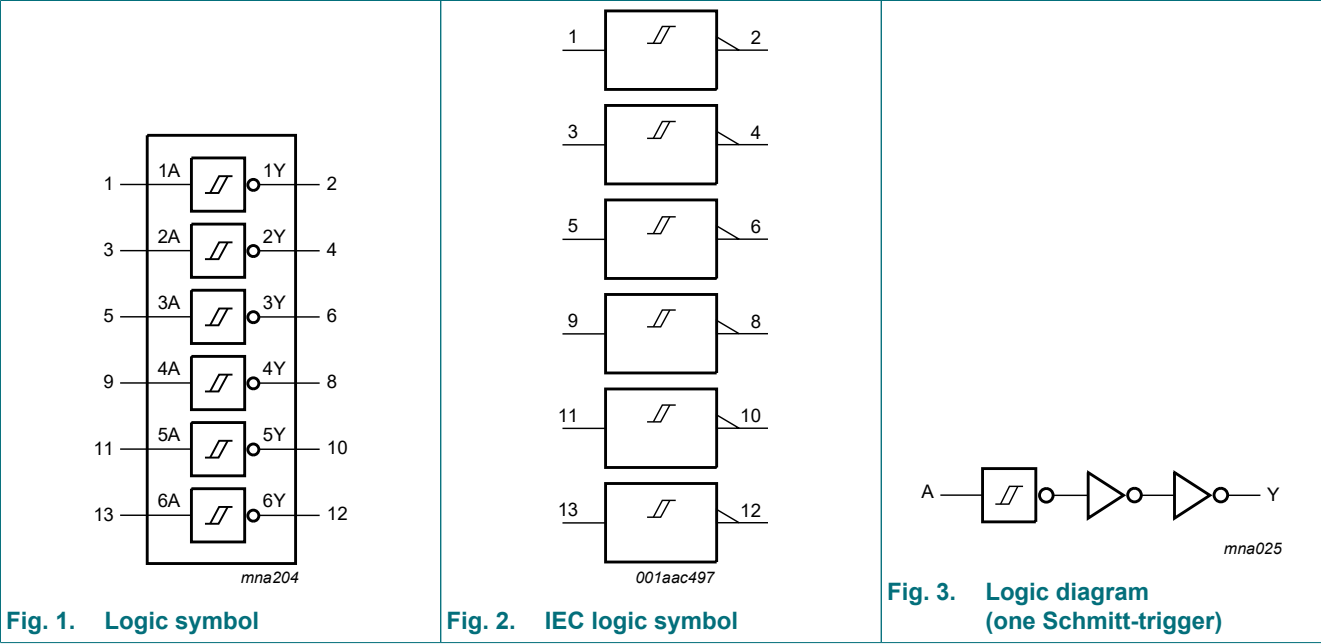
- Wide supply voltage range from 2.0 V to 5.5 V
- Maximum t_{pd} of 10 ns at 5 V
- Typical $V_{OL(p)} < 0.8$ V at $V_{CC} = 3.3$ V, $T_{amb} = 25$ °C
- Typical $V_{OH(v)} > 2.3$ V at $V_{CC} = 3.3$ V, $T_{amb} = 25$ °C
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 3000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 2000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

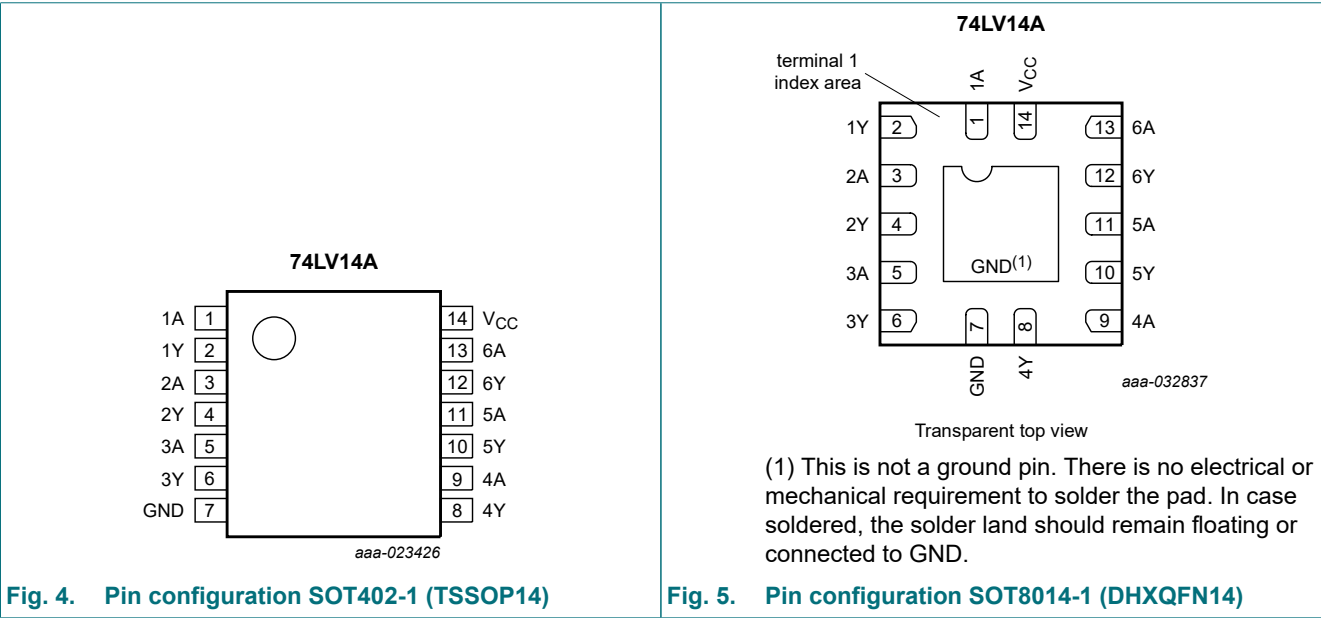
Type number	Package			
	Temperature range	Name	Description	Version
74LV14APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV14ABZ	-40 °C to +125 °C	DHXQFN14	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 14 terminals; 0.4 mm pitch; body 2 mm × 2 mm × 0.48 mm	SOT8014-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output
nA	nY
L	H
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage	[1]	-0.5	+7.0	V
V _O	output voltage	output HIGH or LOW state [2] [3]	-0.5	V _{CC} + 0.5	V
		output power-down [2]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-20	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±35	mA
I _{CC}	supply current		-	70	mA
I _{GND}	ground current		-70	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		SOT402-1 [4]	-	500	mW
		SOT8014-1 [5]	-	250	mW

[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.
[2] If the output current ratings are observed, the output voltage ratings may be exceeded.
[3] This value is limited to 7 V maximum.
[4] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
[5] For SOT8014-1 (DHXQFN14) package: P_{tot} derates linearly with 8.7 mW/K above 121 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.0	5.0	5.5	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	output HIGH or LOW state	0	-	V _{CC}	V
		output power-down	0	-	5.5	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.3 V to 2.7 V	-	-	50	ms/V
		V _{CC} = 3.0 V to 3.6 V	-	-	20	ms/V
		V _{CC} = 4.5 V to 5.5 V	-	-	1	ms/V

9. Static characteristics

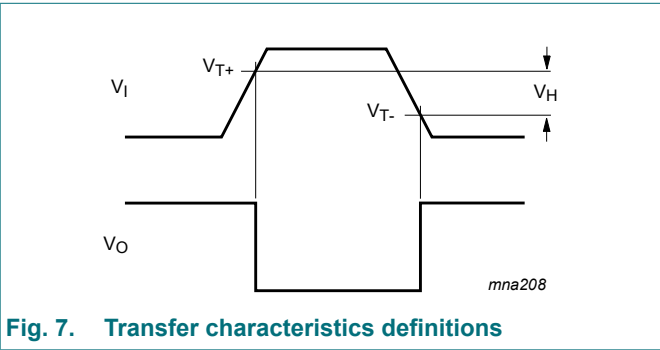
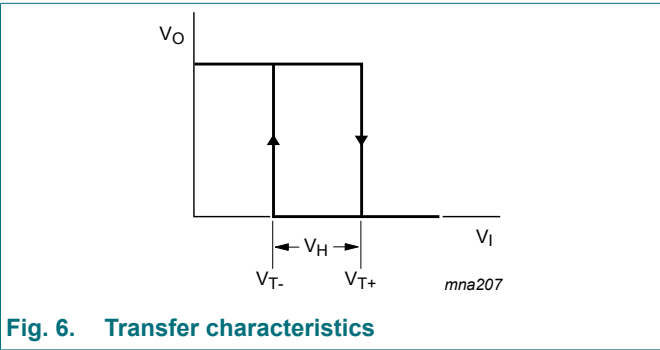
Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{T+}	positive-going threshold voltage	V _{CC} = 2.5 V	-	-	1.75	-	1.75	-	1.75	V
		V _{CC} = 3.3 V	-	-	2.31	-	2.31	-	2.31	V
		V _{CC} = 5.0 V	-	-	3.5	-	3.5	-	3.5	V
V _{T-}	negative-going threshold voltage	V _{CC} = 2.5 V	0.75	-	-	0.75	-	0.75	-	V
		V _{CC} = 3.3 V	0.99	-	-	0.99	-	0.99	-	V
		V _{CC} = 5.0 V	1.5	-	-	1.5	-	1.5	-	V
V _H	hysteresis voltage	V _{CC} = 2.5 V	0.25	-	-	0.25	-	0.25	-	V
		V _{CC} = 3.3 V	0.33	-	-	0.33	-	0.33	-	V
		V _{CC} = 5.0 V	0.5	-	-	0.5	-	0.5	-	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		V _{CC} = 2.0 V to 5.5 V; I _O = -50 μA	V _{CC} -0.1	-	-	V _{CC} -0.1	-	V _{CC} -0.1	-	V
		V _{CC} = 2.3 V; I _O = -2 mA	2	-	-	2	-	2	-	V
		V _{CC} = 3.0 V; I _O = -6 mA	2.48	-	-	2.48	-	2.48	-	V
		V _{CC} = 4.5 V; I _O = -12 mA	3.8	-	-	3.8	-	3.8	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		V _{CC} = 2.0 V to 5.5 V; I _O = 50 μA	-	-	0.1	-	0.1	-	0.1	V
		V _{CC} = 2.3 V; I _O = 2 mA	-	-	0.4	-	0.4	-	0.4	V
		V _{CC} = 3.0 V; I _O = 6 mA	-	-	0.44	-	0.44	-	0.44	V
		V _{CC} = 4.5 V; I _O = 12 mA	-	-	0.55	-	0.55	-	0.55	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _{OFF}	power-off leakage current	V _I or V _O = GND to 5.5 V; V _{CC} = 0 V	-	-	0.5	-	5	-	5	μA
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 0 V to 5.5 V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2	-	20	-	20	μA

9.1. Transfer characteristics waveforms



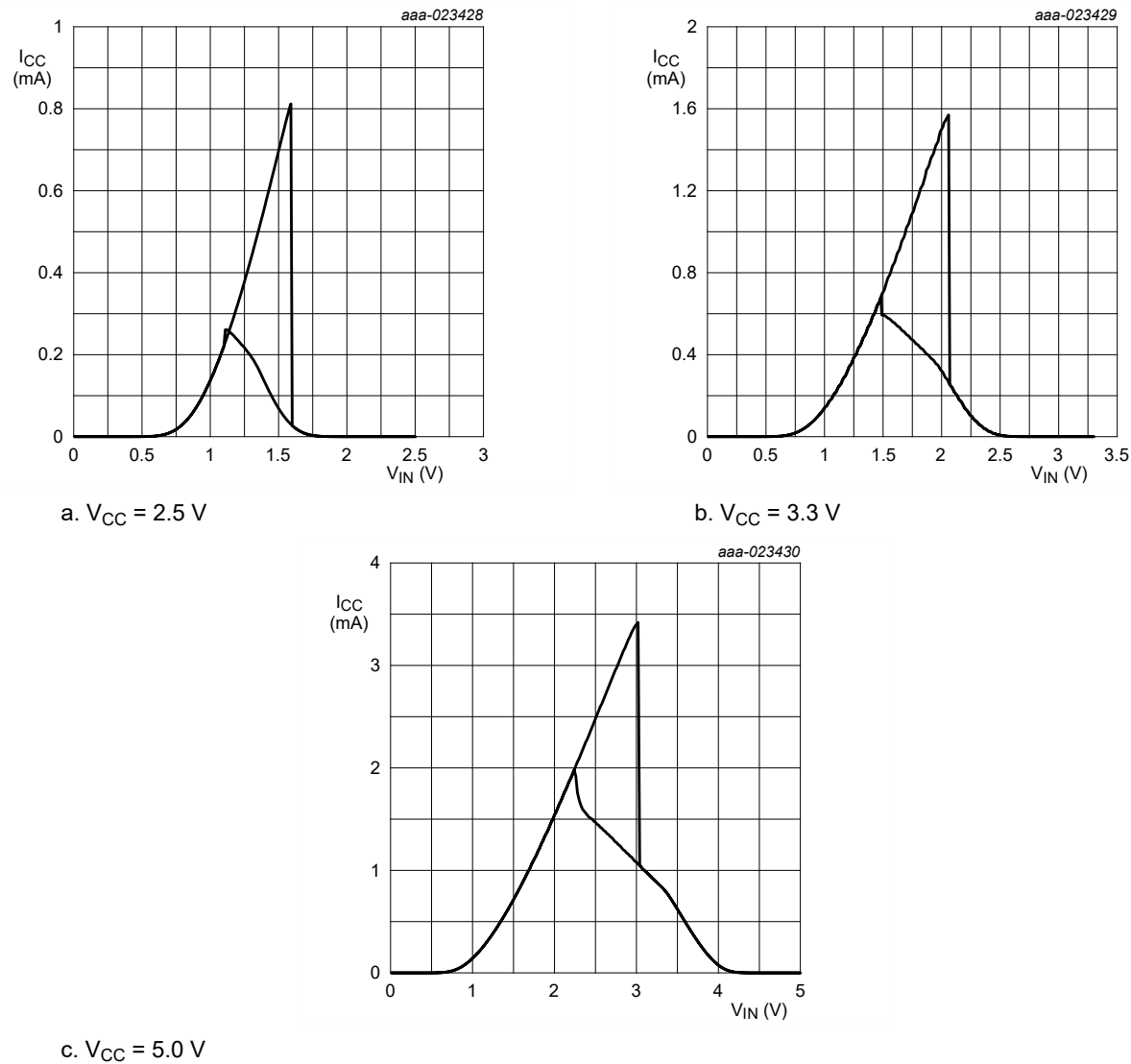


Fig. 8. Typical transfer characteristics

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. For test circuit, see Fig. 10.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Fig. 9 [2]								
		V _{CC} = 2.3 V to 2.7 V								
		C _L = 15 pF	-	5.6	19.7	1	22	1	23	ns
		C _L = 50 pF	-	8.7	24	1	27	1	28	ns
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.4	12.8	1	15	1	16	ns
		C _L = 50 pF	-	6.7	16.3	1	18.5	1	19.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.4	8.6	1	10	1	11	ns
		C _L = 50 pF	-	5.2	10.6	1	12	1	13	ns
C _I	input capacitance	V _I = V _{CC} or GND; V _{CC} = 3.3 V	-	2	6	-	6	-	6	pF
C _O	output capacitance	V _O = V _{CC} or GND; V _{CC} = 3.3 V	-	5	-	-	-	-	-	pF
C _{PD}	power dissipation capacitance	per buffer; C _L = 50 pF; f = 10 MHz; V _I = GND to V _{CC} [3]								
		V _{CC} = 3.3 V	-	8	-	-	-	-	-	pF
		V _{CC} = 5.0 V	-	9	-	-	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 2.5 V, 3.3 V, and 5 V respectively, unless otherwise specified.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts.

Table 8. Noise characteristics

GND = 0 V. For test circuit, see Fig. 10.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ	Max	
V _{CC} = 3.3 V; C _L = 50 pF						
V _{OL(p)}	LOW-level output voltage (peak)		-	0.2	0.8	V
V _{OL(v)}	LOW-level output voltage (valley)		-0.8	-0.1	-	V
V _{OH(v)}	HIGH-level output voltage (valley)		-	3.1	-	V
V _{IH(AC)}	AC HIGH-level input voltage		2.31	-	-	V
V _{IL(AC)}	AC LOW-level input voltage		-	-	0.99	V

10.1. Waveforms and test circuit

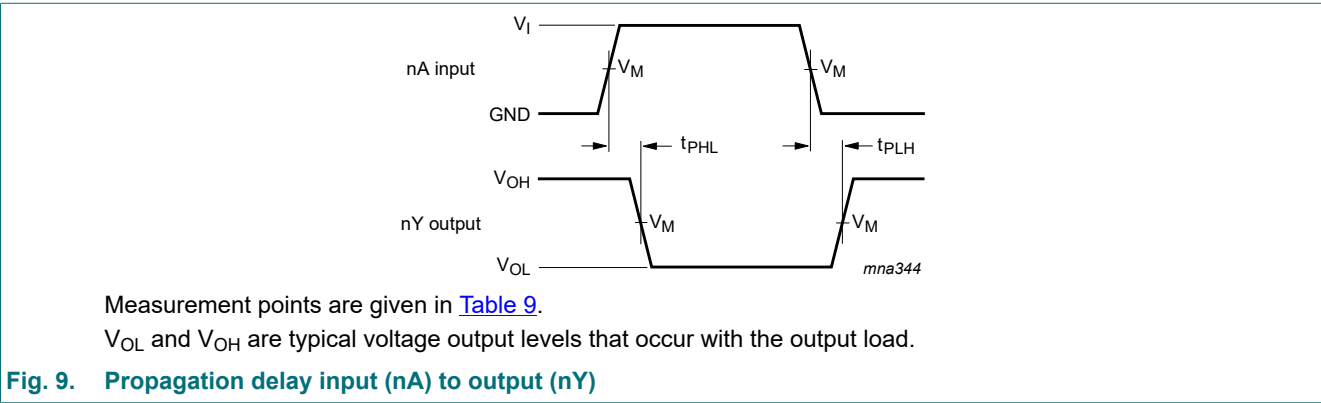


Table 9. Measurement points

Input	Output
V_M	V_M
$0.5V_{CC}$	$0.5V_{CC}$

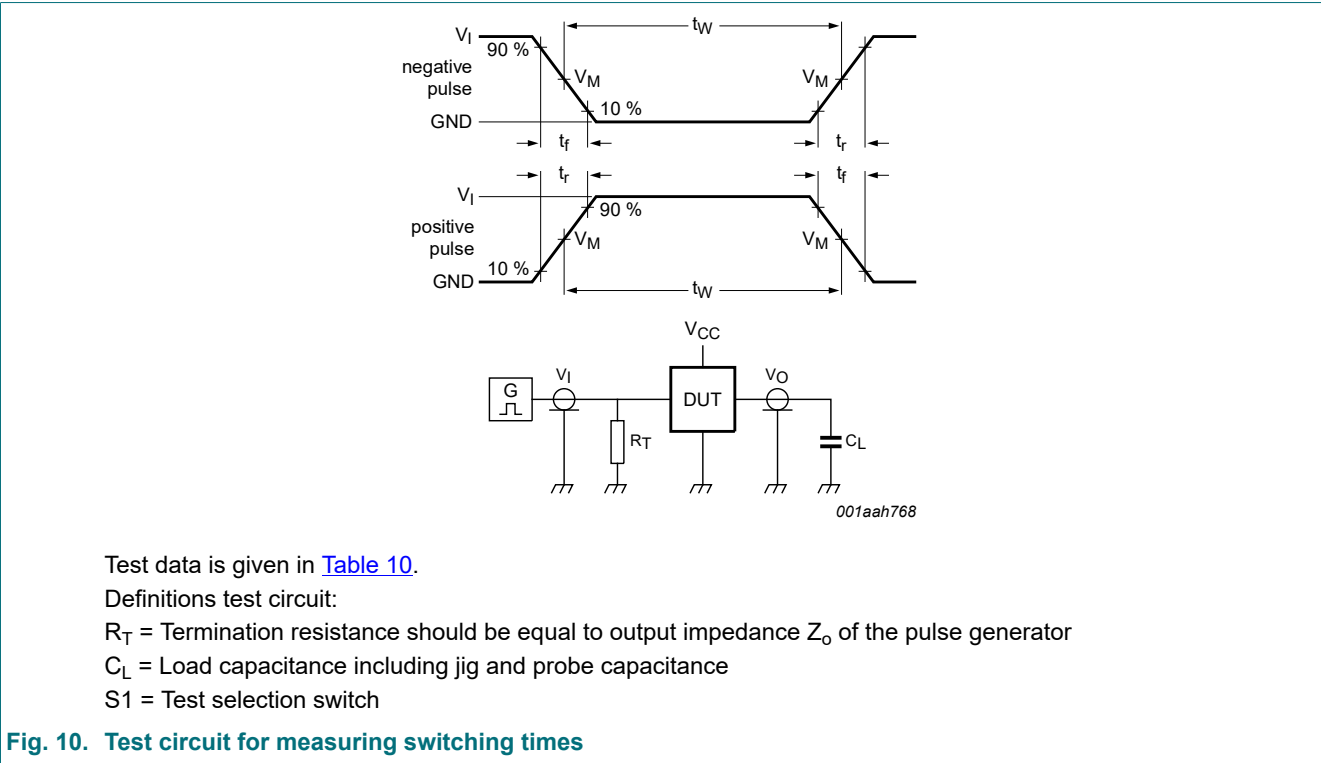


Table 10. Test data

Input		Load	Test
V_I	t_r, t_f	C_L	
GND to V_{CC}	3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm SOT402-1

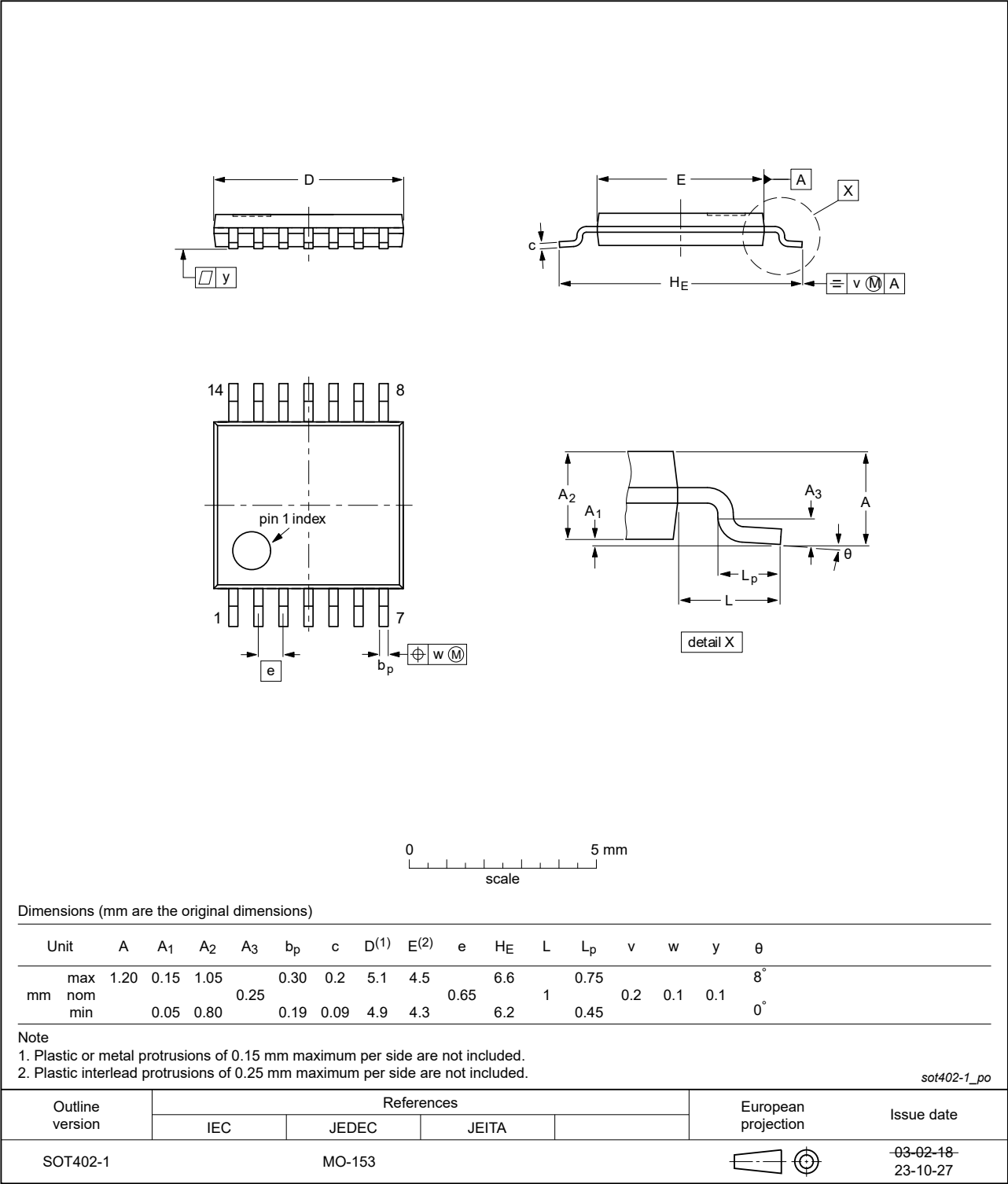


Fig. 11. Package outline SOT402-1 (TSSOP14)

DHXQFN14: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package;
no leads; 14 terminals; 0.4 mm pitch; body 2 mm x 2 mm x 0.48 mm

SOT8014-1

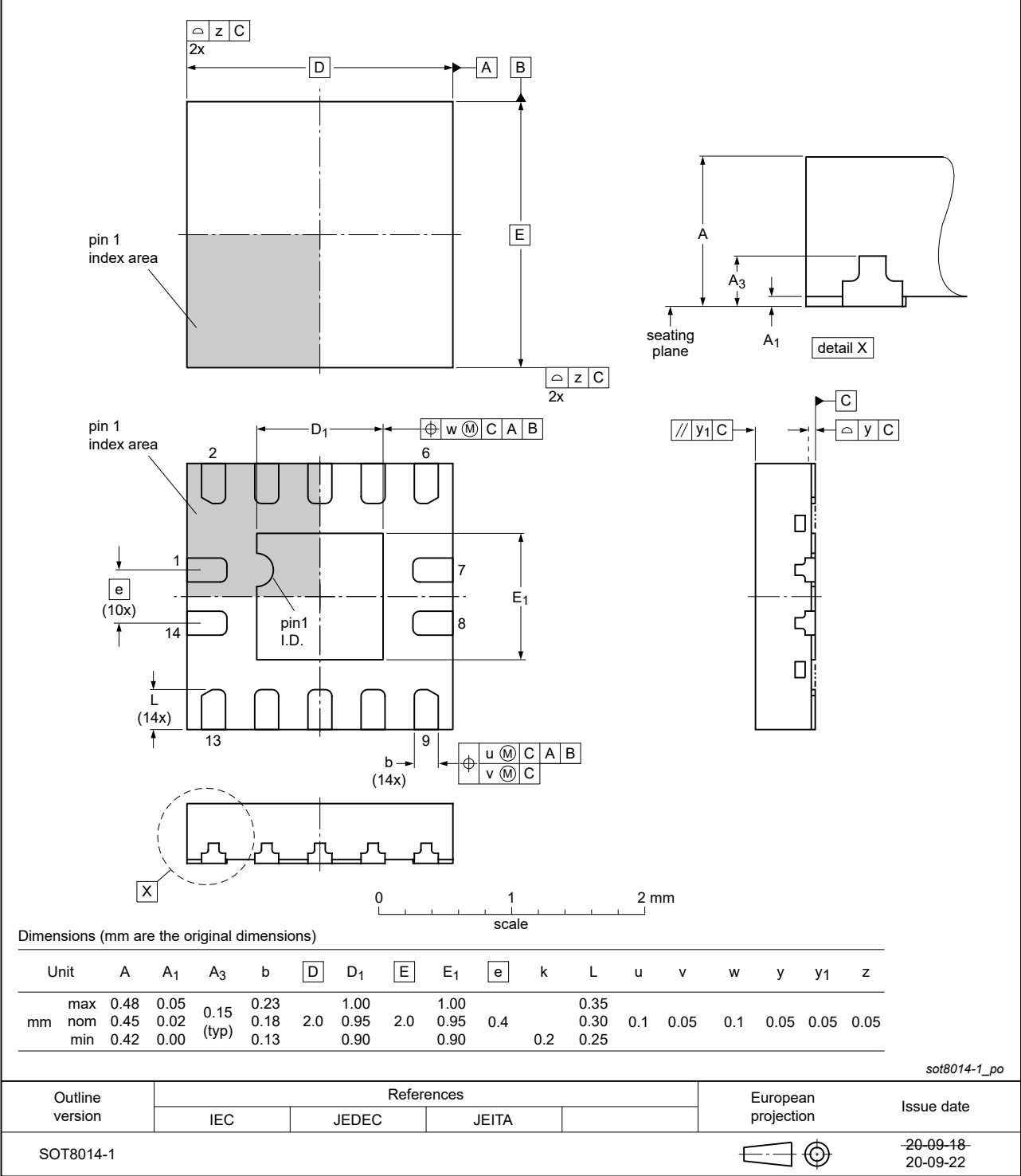


Fig. 12. Package outline SOT8014-1 (DHXQFN14)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV14A v.5	20240408	Product data sheet	-	74LV14A v.4
Modifications:	- Fig. 11: Aligned TSSOP package outline drawing to JEDEC MO-153. - Section 2: ESD specification updated according to the latest JEDEC standard.			
74LV14A v.4	20210429	Product data sheet	-	74LV14A v.3
Modifications:	- Type number 74LV14ABZ (SOT8014-1 / DHXQFN14) added. - Table 4: Derating value for P_{tot} total power dissipation updated.			
74LV14A v.3	20161102	Product data sheet	-	74LV14A v.2
Modifications:	Type numbers 74LV14AD and 74LV14ABQ removed.			
74LV14A v.2	20160809	Product data sheet	-	74LV14A v.1
Modifications:	Section 1: Typo corrected.			
74LV14A v.1	20160613	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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