



# PESD24VV1BLS

## Bidirectional ESD protection diode

3 June 2022

Product data sheet

## 1. General description

ESD protection device in a leadless ultra small DFN1006BD-2 (SOD882BD) Surface-Mounted Device (SMD) plastic package with side-wettable flanks, designed to protect one single line from the damage caused by ElectroStatic discharge (ESD) and other transients.

## 2. Features and benefits

- Reverse stand-off voltage:  $V_{RWM} = 24\text{ V}$
- Low clamping voltage:  $V_{CL} = 33\text{ V}$  at  $I_{PP} = 3.5\text{ A}$
- ESD protection up to 30 kV (IEC 61000-4-2)
- ESD protection up to 30 kV (ISO 10605: C = 330 pF, R = 330  $\Omega$ )
- Ultra low leakage current:  $I_{RM} < 1\text{ nA}$

## 3. Applications

ESD protection for low-speed interfaces in communication, consumer and computing devices

- USB Type-C, CC and SBU lines

## 4. Quick reference data

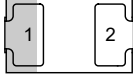
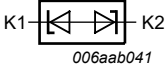
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RWM}$	reverse standoff voltage	$T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	24	V
$I_{PPM}$	rated peak pulse current	$t_p = 8/20\text{ }\mu\text{s}$	[1]	-	3.5	A
$V_{CL}$	clamping voltage	$I_{PPM} = 3.5\text{ A}$ ; $t_p = 8/20\text{ }\mu\text{s}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	33	42	V

[1] Device stressed with 8/20  $\mu\text{s}$  exponential decay waveform according to IEC 61000-4-5.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 <p>Transparent top view</p> <p><b>DFN1006BD-2 (SOD882BD)</b></p>	 <p>006aab041</p>
2	K2	cathode (diode 2)		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD24VV1BLS	DFN1006BD-2	Leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.47 mm body	SOD882BD

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PESD24VV1BLS	9D

## 8. Limiting values

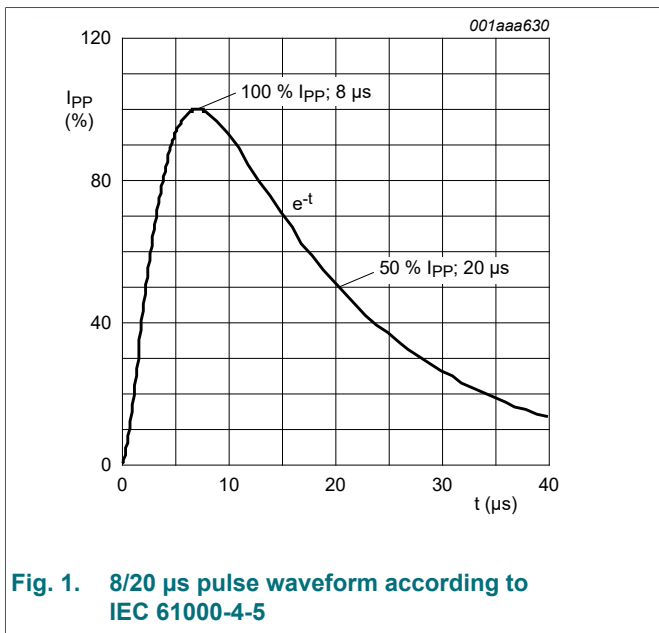
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

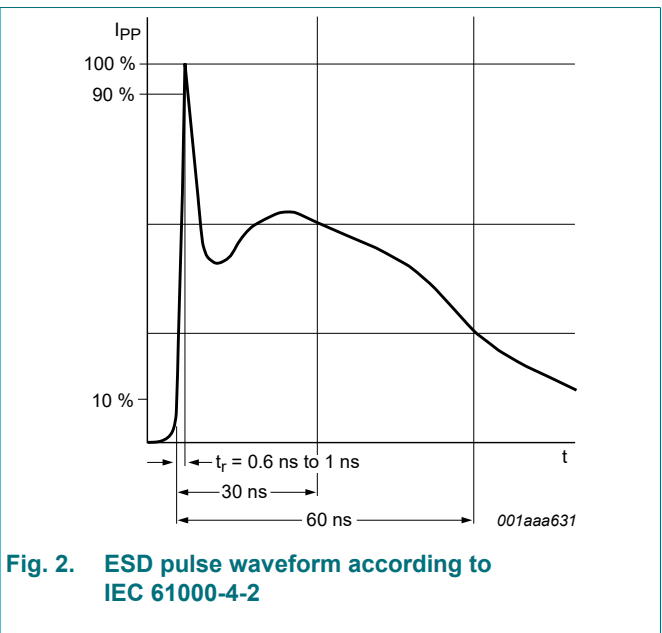
Symbol	Parameter	Conditions		Min	Max	Unit
$I_{PPM}$	rated peak pulse current	$t_p = 8/20 \mu s$	[1]	-	3.5	A
$T_j$	junction temperature			-	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C
<b>ESD maximum ratings</b>						
$V_{ESD}$	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2]	-	30	kV
		ISO 10605: contact discharge; C = 330 pF, R = 330 $\Omega$	[2]	-	30	kV
		ISO 10605: contact discharge; C = 150 pF, R = 330 $\Omega$	[2]	-	30	kV

[1] Device stressed with 8/20  $\mu s$  exponential decay waveform according to IEC 61000-4-5.

[2] Device stressed with ten non-repetitive ESD pulses.



**Fig. 1. 8/20  $\mu s$  pulse waveform according to IEC 61000-4-5**



**Fig. 2. ESD pulse waveform according to IEC 61000-4-2**

### 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{RWM}$	reverse standoff voltage	$T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	24	V	
$V_{BR}$	breakdown voltage	$I_R = 10\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$	25.5	30.5	35.5	V	
$I_{RM}$	reverse leakage current	$V_R = 24\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	1	50	nA	
$C_d$	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	14	17	pF	
$V_{CL}$	clamping voltage	$I_{PP} = 1\text{ A}; t_p = 8/20\text{ }\mu\text{s}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	31	40	V
		$I_{PPM} = 3.5\text{ A}; t_p = 8/20\text{ }\mu\text{s}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	33	42	V
		$I_{PP} = 16\text{ A}; t_p = 100\text{ ns}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	-	32	-	V
$R_{dyn}$	dynamic resistance	$I_R = 10\text{ A}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	-	0.2	$\Omega$	

- [1] Device stressed with 8/20  $\mu\text{s}$  exponential decay waveform according to IEC 61000-4-5.
- [2] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

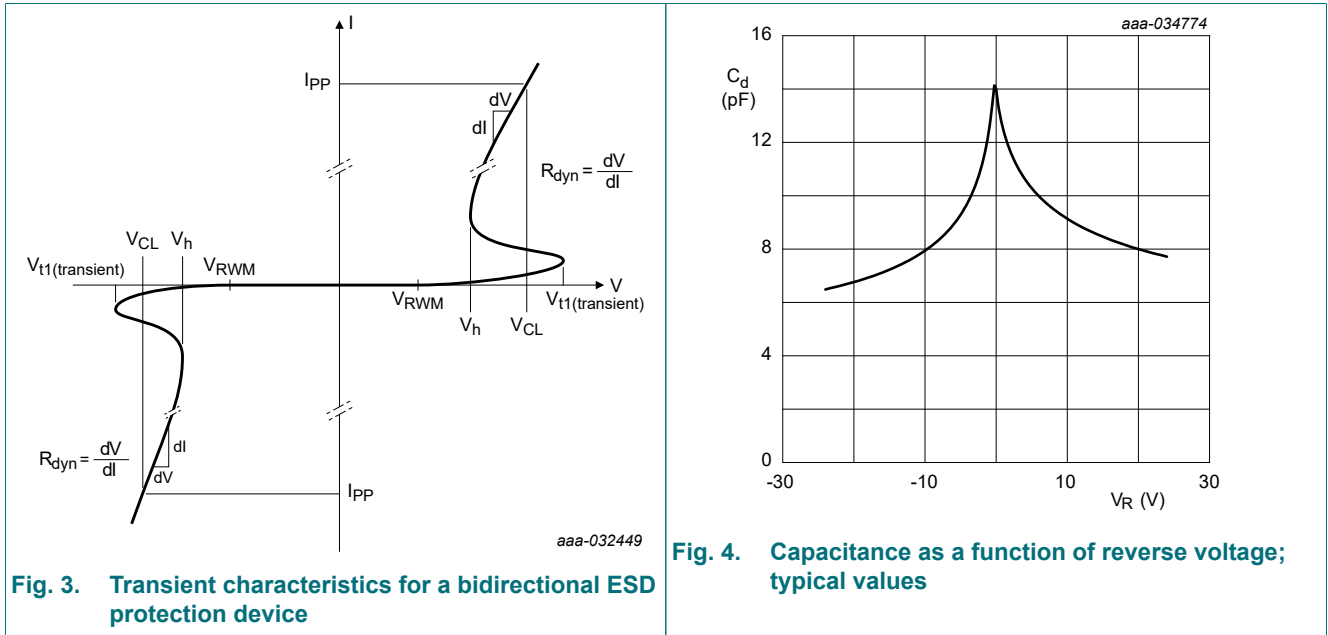


Fig. 3. Transient characteristics for a bidirectional ESD protection device

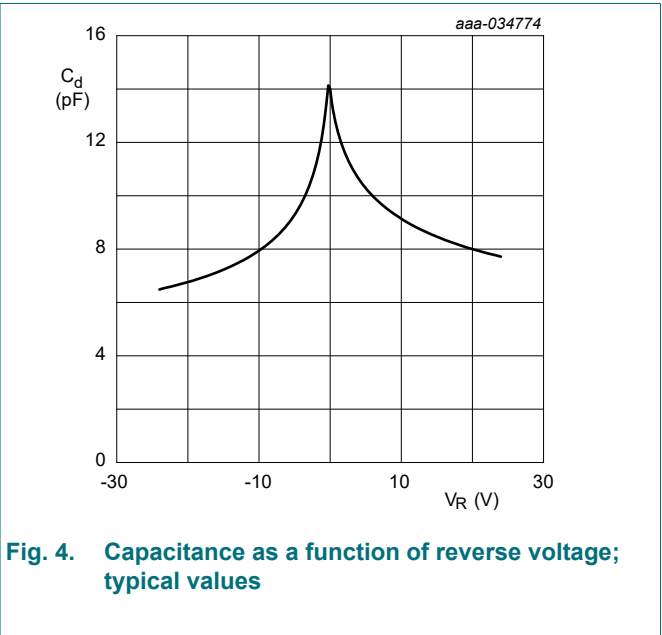
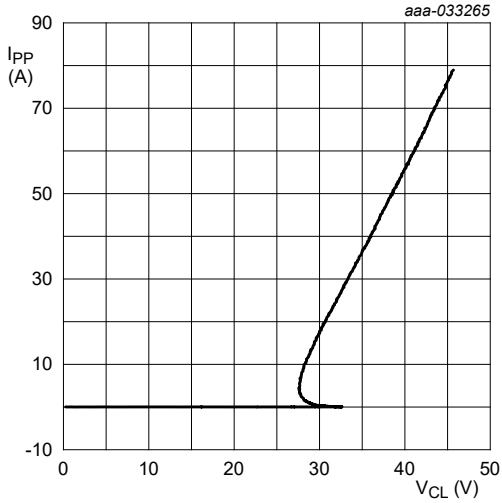
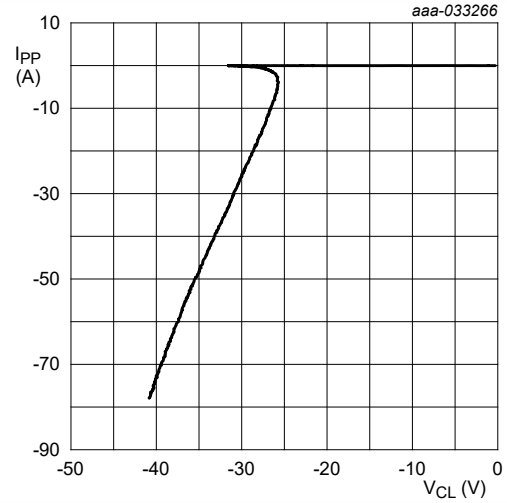


Fig. 4. Capacitance as a function of reverse voltage; typical values



Transmission Line Pulse (TLP);  
 $t_p = 100 \text{ ns}$ ;  $t_r = 1 \text{ ns}$

**Fig. 5. Dynamic resistance with positive clamping; typical values**



Transmission Line Pulse (TLP);  
 $t_p = 100 \text{ ns}$ ;  $t_r = 1 \text{ ns}$

**Fig. 6. Dynamic resistance with negative clamping; typical values**

## 10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

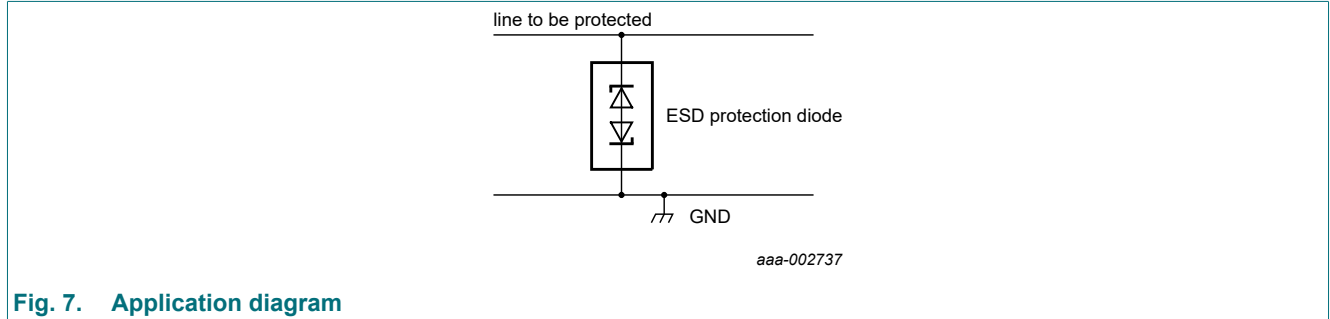


Fig. 7. Application diagram

### Circuit board layout and protection device placement

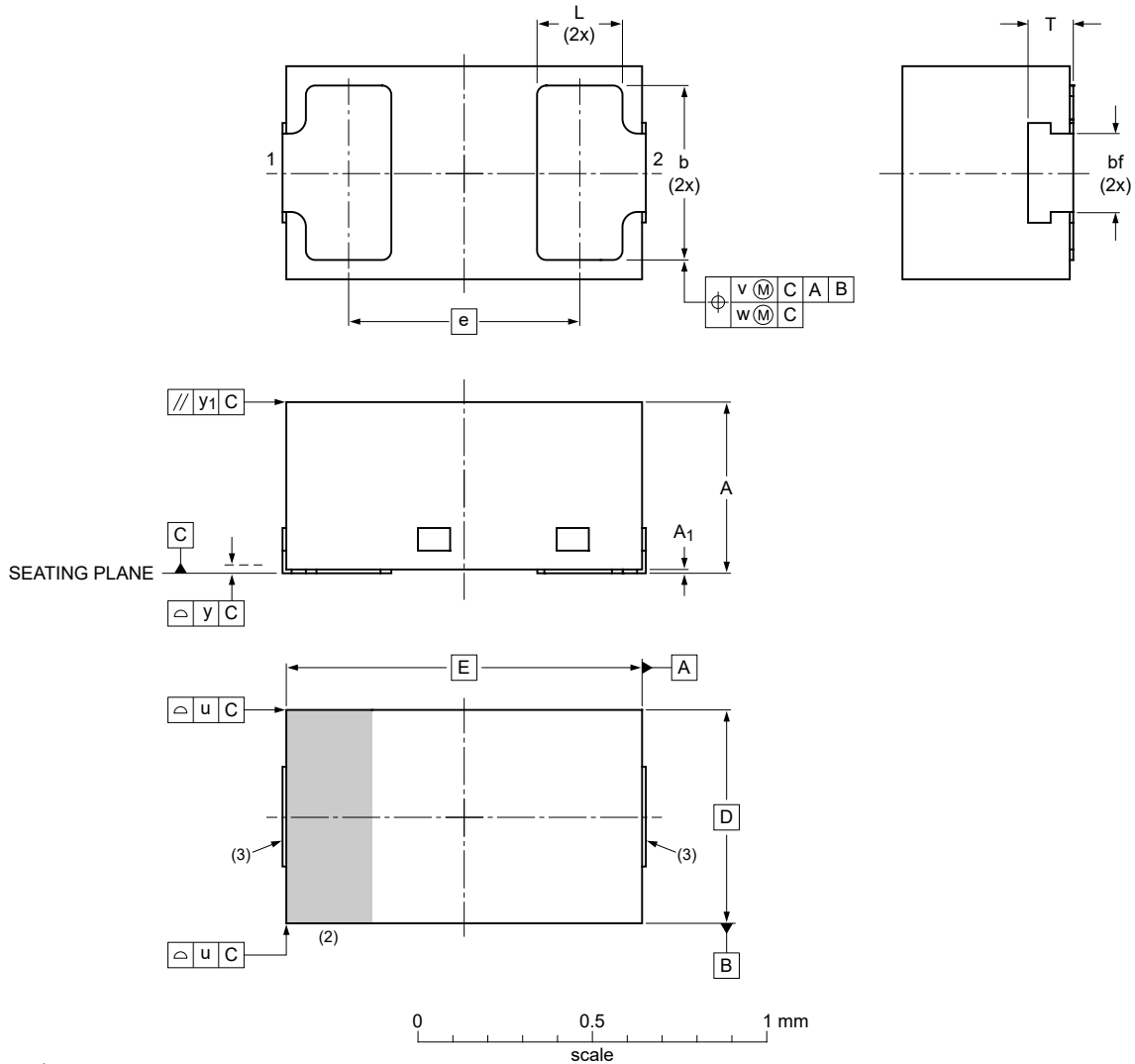
Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

### 11. Package outline

**DFN1006BD-2** Leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals;  
0.65 mm pitch; 1 mm x 0.6 mm x 0.47 mm body

**SOD882BD**



**Dimensions**

Unit	A <sup>(1)</sup>	A <sub>1</sub>	bf <sup>(1)</sup>	b	D	E	e	L	T <sup>(1)</sup>	u	v	w	y	y <sub>1</sub>
max	0.50	0.04		0.55				0.30	0.22					
nom	0.47			0.50	0.60	1.00	0.65	0.25	0.16	0.05	0.10	0.05	0.05	0.05
min	0.44		0.20	0.45				0.22	0.10					

**Note**

1. Dimension including plating thickness.
2. The marking bar indicates the cathode.
3. Solderable lead end, protrusion max. 0.02 mm.

sod882bd\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOD882BD		MO-343AA				20-06-22 20-06-23

**Fig. 8. Package outline DFN1006BD-2 (SOD882BD)**

## 12. Soldering

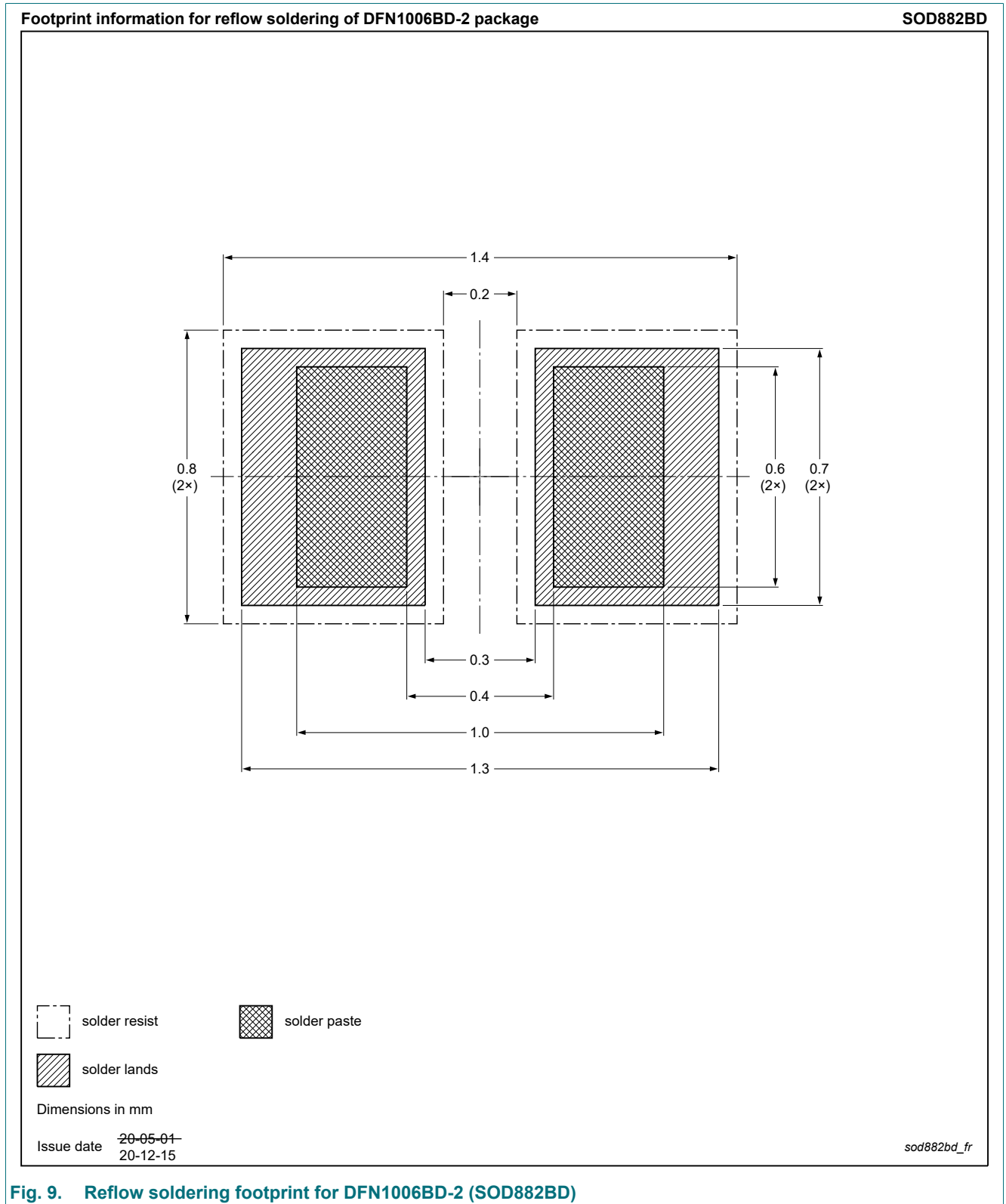


Fig. 9. Reflow soldering footprint for DFN1006BD-2 (SOD882BD)



### 13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD24VV1BLS v.1	20220603	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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