

PDTD113ZT

50 V, 500 mA NPN resistor-equipped transistor; R1 = 1 k Ω , R2 = 10 k Ω

1 January 2023

Product data sheet

1. General description

NPN 500 mA Resistor-Equipped Transistor (RET) in a small SOT23 Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTB113ZT

2. Features and benefits

- · Built-in bias resistors
- Reduces component count
- · Simplifies circuit design
- · Reduces pick and place costs
- 500 mA output current capability
- ± 10 % resistor ratio tolerance

3. Applications

- · Digital application in automotive and industrial segments
- Cost-saving alternative for BC817 series in digital applications
- · Controlling IC inputs
- · Switching loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
Io	output current		-	-	500	mA
R1	bias resistor 1 (input)	T _{amb} = 25 °C	0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		9	10	11	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)]3	
2	GND	ground (emitter)		R1
3	0	output (collector)	SOT23	GND R2 aaa-019964



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6. Ordering information

Table 3. Ordering information

Type number Package							
	Name	Description	Version				
PDTD113ZT		plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23				

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PDTD113ZT	%7V

^{[1] % =} placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	5	V
VI	input voltage	positive		-	10	V
		negative		-	-5	V
Io	output current			-	500	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	250	mW
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	500	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _{CBO}	collector-base cut-off	V _{CB} = 40 V; I _E = 0 A; T _{amb} = 25 °C	-	-	100	nA
	current	V _{CB} = 50 V; I _E = 0 A; T _{amb} = 25 °C	-	-	100	nA
I _{CEO}	collector-emitter cut-off current	$V_{CE} = 50 \text{ V}; I_{B} = 0 \text{ A}; T_{amb} = 25 \text{ °C}$	-	-	0.5	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A; T _{amb} = 25 °C	-	-	0.8	mA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 50 mA; T _{amb} = 25 °C	70	-	-	
V _{CEsat}	collector-emitter saturation voltage	$I_C = 50 \text{ mA}; I_B = 2.5 \text{ mA}; T_{amb} = 25 \text{ °C}$	-	-	300	mV
V _{I(off)}	off-state input voltage	V _{CE} = 5 V; I _C = 100 μA; T _{amb} = 25 °C	0.3	0.6	1	V
V _{I(on)}	on-state input voltage	$V_{CE} = 0.3 \text{ V}; I_{C} = 20 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$	0.4	0.8	1.4	V
R1	bias resistor 1 (input)	T _{amb} = 25 °C	0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		9	10	11	
C _c	collector capacitance	V_{CB} = 10 V; I_{E} = 0 A; i_{e} = 0 A; f = 100 MHz; T_{amb} = 25 °C	-	7	-	pF

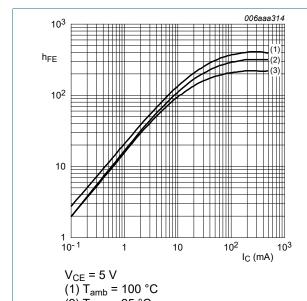
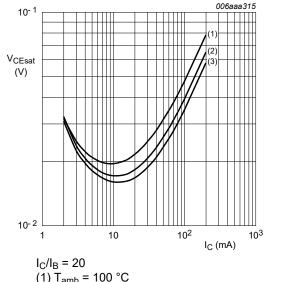


Fig. 1. DC current gain as a function of collector current; typical values

(2) $T_{amb} = 25 \text{ °C}$ (3) $T_{amb} = -40 \text{ °C}$

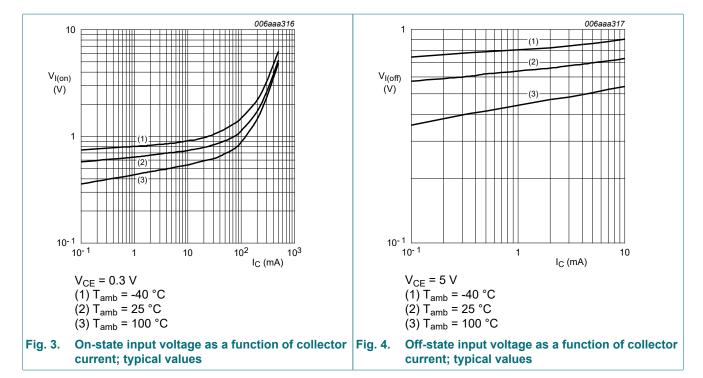


(1) T_{amb} = 100 °C (2) T_{amb} = 25 °C

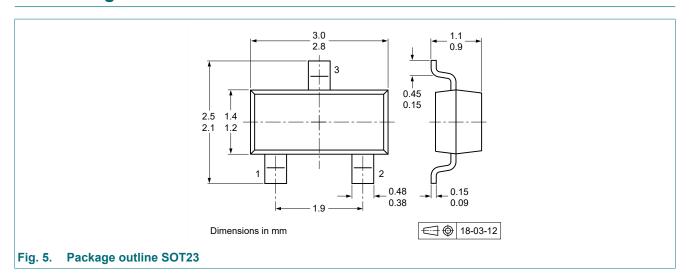
 $(3) T_{amb} = -40 °C$

Fig. 2. Collector-emitter saturation voltage as a function of collector current; typical values

50 V, 500 mA NPN resistor-equipped transistor; R1 = 1 k Ω , R2 = 10 k Ω

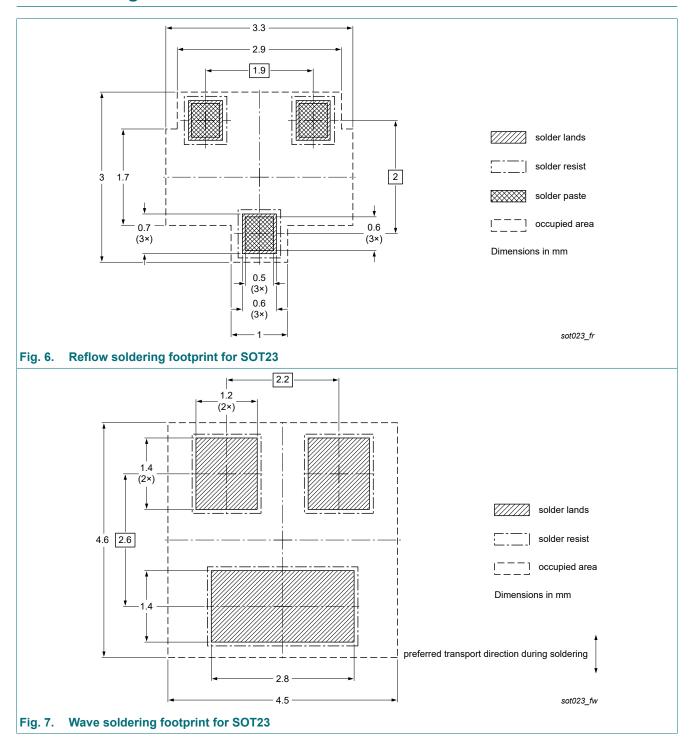


11. Package outline



50 V, 500 mA NPN resistor-equipped transistor; R1 = 1 k Ω , R2 = 10 k Ω

12. Soldering



50 V, 500 mA NPN resistor-equipped transistor; R1 = 1 k Ω , R2 = 10 k Ω

13. Revision history

Table 8. Revision history

Table 6. Revision history								
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes				
PDTD113ZT v.4	20230101	Product data sheet	-	PDTD113ZT v.3				
Modifications:		 Product(s) changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s). 						
PDTD113ZT v.3	20220406	Product data sheet	-	PDTD113ZT_2				
PDTD113ZT_2	20100923	Product data sheet	-	PDTD113Z_SER_1				
PDTD113Z_SER_1	20050405	Product data sheet	-	-				

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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