

74HC2G66-Q100; 74HCT2G66-Q100

Dual single-pole single-throw analog switch Rev. 3 — 21 November 2023

Product data sheet

1. General description

The 74HC2G66-Q100; 74HCT2G66-Q100 is a dual single pole, single-throw analog switch. Each switch has two input/output terminals (nY and nZ) and a digital enable input (nE). When nE is LOW, the analog switch is turned off. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 10.0 V for 74HC2G66-Q100
- Very low ON resistance:
 - 41 Ω (typ.) at V_{CC} = 4.5 V
 - 30 Ω (typ.) at V_{CC} = 6.0 V
 - 21 Ω (typ.) at V_{CC} = 9.0 V
- · CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number Package											
	rackage										
		Temperature range	Name	Description	Version						
	74HC2G66DP-Q100 74HCT2G66DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2						
	74HC2G66DC-Q100 74HCT2G66DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1						



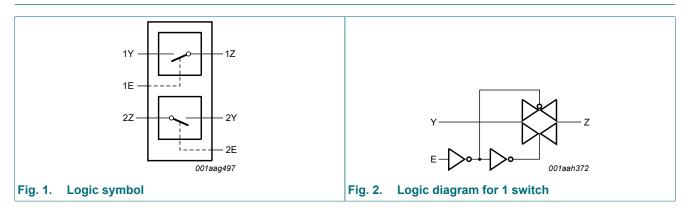
4. Marking

Table 2. Marking codes

Type number	Marking [1]
74HC2G66DP-Q100	H66
74HCT2G66DP-Q100	Т66
74HC2G66DC-Q100	H66
74HCT2G66DC-Q100	T66

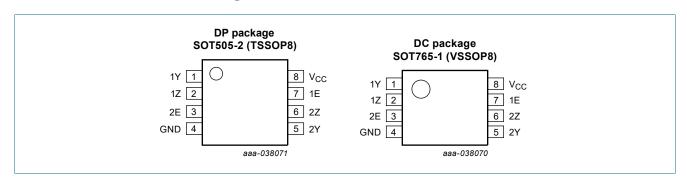
^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

able 6.1 in description							
Symbol	Pin	Description					
1Y, 2Y	2Y 1, 5 independent input or output						
1Z, 2Z	independent input or output						
GND	4	ground (0 V)					
1E, 2E	7, 3	enable input (active HIGH)					
V _{CC}	8	supply voltage					

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7. Functional description

Table 4. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$

Input nE	Switch
L	OFF
Н	ON

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+11.0	V
I _{IK}	input clamping current	$V_1 < -0.5 \text{ V or } V_1 > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I _{SK}	switch clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I _{SW}	switch current	$V_{SW} > -0.5 \text{ V or } V_{SW} < V_{CC} + 0.5 \text{ V}$	-	±20	mA
Icc	supply current		-	30	mA
I _{GND}	ground current		-30	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		per package [2]	-	250	mW
		per switch [2]	-	100	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC2G66-Q100			74H0	Unit		
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	10.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _{SW}	switch voltage	[1]	0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V
		V _{CC} = 10.0 V	-	-	35	-	-	-	ns/V

^[1] To avoid drawing V_{CC} current out of pin nZ, when switch current flows in pin nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pin nZ, no V_{CC} current will flow out of terminal nY. In this case there is no limit for the voltage drop across the switch, but the voltage at pins nY and nZ may not exceed V_{CC} or GND.

74HC_HCT2G66_Q100

^[2] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C. For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

10. Static characteristics

Table 7. Static characteristics

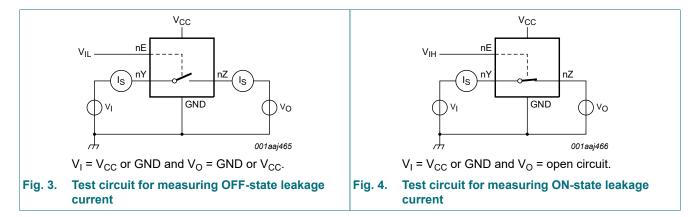
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	5°C	-40 °C to	+125 °C	Unit
			Min	Typ [1]	Max	Min	- \\\ - \\\ 1.35 \\\ 1.8 \\\ 2.7 \\\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \	
74HC2G	66-Q100			•				
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
		V _{CC} = 9.0 V	6.3	4.7	-	6.3	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
		V _{CC} = 9.0 V	-	4.3	2.7	-	2.7	V
l _l	input leakage current	nE; V _I = V _{CC} or GND						
		V _{CC} = 6.0 V	-	-	±0.1	-	±0.1	μΑ
		V _{CC} = 9.0 V	-	-	±0.2	-	±0.2	μΑ
I _{S(OFF)}	OFF-state leakage current	nY or nZ; V _{CC} = 9.0 V; see Fig. 3	-	0.1	1.0	-	1.0	μΑ
I _{S(ON)}	ON-state leakage current	nY or nZ; V _{CC} = 9.0 V; see Fig. 4	-	0.1	1.0	-	1.0	μΑ
I _{CC}	supply current	nE, nY and nZ = V _{CC} or GND						
		V _{CC} = 6.0 V	-	-	10	-	20	μΑ
		V _{CC} = 9.0 V	-	-	20	-	40	μA
Cı	input capacitance		-	3.5	-	-	-	pF
C_{PD}	power dissipation capacitance		-	9	-	-	-	pF
C _{S(ON)}	ON-state capacitance		-	8	-	-	-	pF
	G66-Q100							
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
l _l	input leakage current	nE; $V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±1.0	-	±1.0	μA
I _{S(OFF)}	OFF-state leakage current	nY or nZ; V _{CC} = 5.5 V; see <u>Fig. 3</u>	-	0.1	1.0	-	1.0	μΑ
I _{S(ON)}	ON-state leakage current	nY or nZ; V _{CC} = 5.5 V; see Fig. 4	-	0.1	1.0	-	1.0	μΑ
I _{CC}	supply current	nE, nY and nZ = V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	-	10	-	20	μΑ
ΔI _{CC}	additional supply current	nE = V_{CC} - 2.1 V; I_{O} = 0 A; V_{CC} = 4.5 V to 5.5 V;	-	-	375	-	410	μΑ
Cı	input capacitance		-	3.5	-	-	-	pF
C _{PD}	power dissipation capacitance		-	9	-	-	-	pF
C _{S(ON)}	ON-state capacitance		-	8	-	-	-	pF

^[1] Typical values are measured at T_{amb} = 25 °C.

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10.1. Test circuits



10.2. ON resistance

Table 8. ON resistance for 74HC2G66-Q100 and 74HCT2G66-Q100

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graph see Fig. 6.

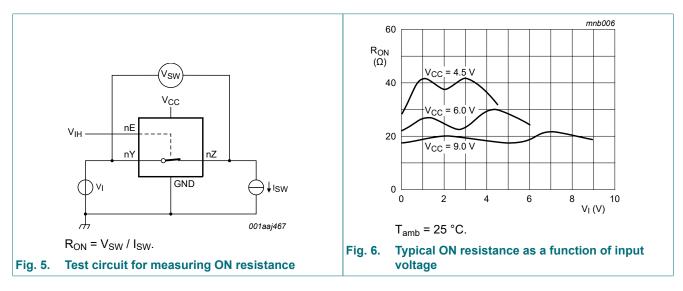
Symbol	Parameter	Conditions	-40	°C to +85	5°C	-40 °C to	o +125 °C	Unit
			Min	Typ [1]	Max	Min Max		
74HC2G6	66-Q100 [2]						'	
R _{ON(peak)}	ak) ON resistance	V _I = GND to V _{CC} ; see <u>Fig. 5</u> and <u>Fig. 6</u>						
	(peak)	I _{SW} = 0.1 mA; V _{CC} = 2.0 V	-	250	-	-	-	Ω
		I _{SW} = 1.0 mA; V _{CC} = 4.5 V	-	41	118	-	142	Ω
		I _{SW} = 1.0 mA; V _{CC} = 6.0 V	-	30	105	-	126	Ω
		I _{SW} = 1.0 mA; V _{CC} = 9.0 V	-	21	88	-	105	Ω
R _{ON(rail)}	ON resistance (rail)	V _I = GND; see <u>Fig. 5</u> and <u>Fig. 6</u>						
		I _{SW} = 0.1 mA; V _{CC} = 2.0 V	-	65	-	-	-	Ω
		I _{SW} = 1.0 mA; V _{CC} = 4.5 V	-	28	95	-	115	Ω
		I _{SW} = 1.0 mA; V _{CC} = 6.0 V	-	22	82	-	100	Ω
		I _{SW} = 1.0 mA; V _{CC} = 9.0 V	-	18	70	-	80	Ω
		V _I = V _{CC} ; see <u>Fig. 5</u> and <u>Fig. 6</u>						
		I _{SW} = 0.1 mA; V _{CC} = 2.0 V	-	65	-	-	-	Ω
		I _{SW} = 1.0 mA; V _{CC} = 4.5 V	-	31	106	-	128	Ω
		I _{SW} = 1.0 mA; V _{CC} = 6.0 V	-	23	94	-	113	Ω
		I _{SW} = 1.0 mA; V _{CC} = 9.0 V	-	19	78	-	95	Ω
ΔR_{ON}	ON resistance	V _I = V _{CC} to GND; see <u>Fig. 5</u> and <u>Fig. 6</u>						
	mismatch between channels	V _{CC} = 4.5 V	-	5	-	-	-	Ω
	Detween Granners	V _{CC} = 6.0 V	-	4	-	-	-	Ω
		V _{CC} = 9.0 V	-	3	-	-	-	Ω

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Symbol	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit
			Min	Typ [1]	Max	Min	Max	
74HCT2G	666-Q100					'		
R _{ON(peak)}		V _I = GND to V _{CC} ; see <u>Fig. 5</u> and <u>Fig. 6</u>						
	(peak)	I _{SW} = 1.0 mA; V _{CC} = 4.5 V	-	41	118	-	142	Ω
R _{ON(rail)}	ON resistance (rail)	V _I = GND; see <u>Fig. 5</u> and <u>Fig. 6</u>						
		I _{SW} = 1.0 mA; V _{CC} = 4.5 V	-	28	95	-	115	Ω
		V _I = V _{CC} ; see <u>Fig. 5</u> and <u>Fig. 6</u>						
		I _{SW} = 1.0 mA; V _{CC} = 4.5 V	-	31	106	-	128	Ω
ΔR_{ON}	ON resistance	V _I = V _{CC} to GND; see <u>Fig. 5</u> and <u>Fig. 6</u>						
	mismatch between channels	V _{CC} = 4.5 V	-	5	-	-	-	Ω

^[1] Typical values are measured at T_{amb} = 25 °C.

10.3. ON resistance test circuit and graphs



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^[2] At supply voltages approaching 2 V, the ON resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using this supply voltage.

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); For test circuit see Fig. 9.

Symbol	Parameter	Conditions		-40	°C to +85	o°C	-40 °C to	o +125 °C	Unit
				Min	Typ [1]	Max	Min	Max	
74HC2G	666-Q100								
t _{pd}	propagation delay	nY to nZ or nZ to nY; $R_L = \infty \Omega$; see Fig. 7	[2]						
		V _{CC} = 2.0 V		-	6.5	65	-	80	ns
		V _{CC} = 4.5 V		-	2	13	-	15	ns
		V _{CC} = 6.0 V		-	1.5	11	-	14	ns
		V _{CC} = 9.0 V		-	1.2	10	-	12	ns
t _{en}	enable time	nE to nY or nZ; see Fig. 8	[2]						
		V _{CC} = 2.0 V		-	40	125	-	150	ns
		V _{CC} = 4.5 V		-	12	29	-	30	ns
		V _{CC} = 6.0 V		-	10	21	-	26	ns
		V _{CC} = 9.0 V		-	7	16	-	20	ns
t _{dis}	disable time	nE to nY or nZ; see Fig. 8	[2]						
		V _{CC} = 2.0 V		-	21	145	-	175	ns
		V _{CC} = 4.5 V		-	12	29	-	35	ns
		V _{CC} = 6.0 V		-	11	28	-	33	ns
		V _{CC} = 9.0 V		-	10	23	-	27	ns
C _{PD}	power dissipation capacitance	$V_I = GND$ to V_{CC}	[3]	-	9	-	-	-	pF
74HCT2	G66-Q100						'	<u>'</u>	
t _{pd}	propagation delay	nY to nZ or nZ to nY; R _L = ∞ Ω; V _{CC} = 4.5 V; see Fig. 7	[2]	-	2	15	-	18	ns
t _{en}	enable time	nE to nY or nZ; V _{CC} = 4.5; see Fig. 8			13	30	-	36	ns
t _{dis}	disable time	nE to nY or nZ; V_{CC} = 4.5 V; see Fig. 8	[2]	-	13	44	-	53	ns
C _{PD}			[3]	-	9	-	-	-	pF

^[1] All typical values are measured at T_{amb} = 25 °C.

 t_{en} is the same as t_{PZL} and t_{PZH} .

 t_{dis} is the same as t_{PLZ} and t_{PHZ} . [3] C_{PD} is used to determine the dynamic power dissipation P_D (μ W).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma((C_L \times C_{SW}) \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

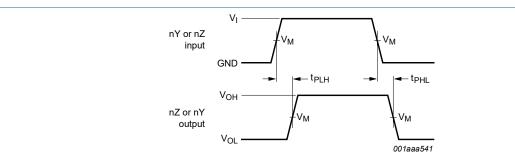
C_{SW} = maximum switch capacitance in pF (see <u>Table 7</u>);

V_{CC} = supply voltage in volts;

 $\Sigma((C_L \times C_{SW}) \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

^[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

11.1. Waveforms and test circuit



Measurement points are given in <u>Table 10</u>.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. Input (nY or nZ) to output (nZ or nY) propagation delays

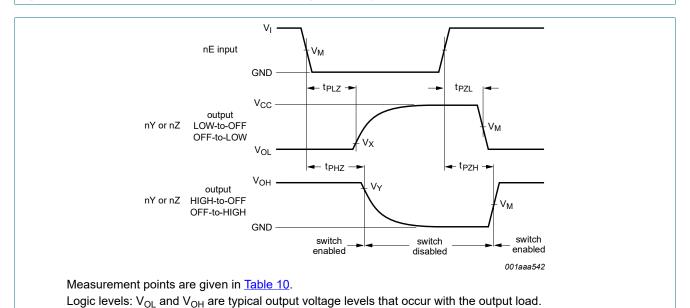
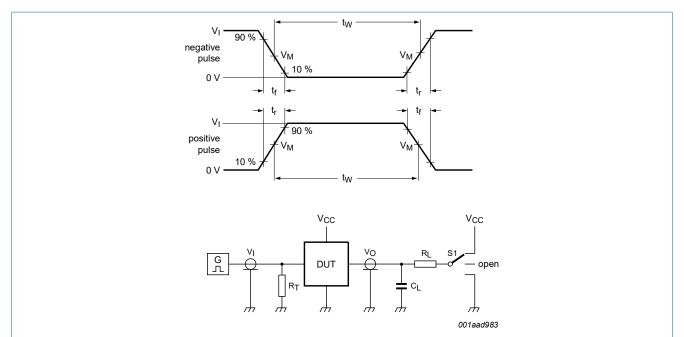


Fig. 8. Enable and disable times

Table 10. Measurement points

Туре	Input	Output					
	V _M	V _M	V _X				
74HC2G66-Q100	0.5V _{CC}	0.5V _{CC}	V _{OL} + 10 %	V _{OH} - 10 %			
74HCT2G66-Q100	1.3 V	1.3 V	V _{OL} + 10 %	V _{OH} - 10 %			



Test data is given in Table 11.

Definitions for test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig. 9. Test circuit for measuring switching times

Table 11. Test data

Туре	Input		Load		S1 position		
	V _I	t _r , t _f [1]	CL	R _L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
74HC2G66-Q100	GND to V _{CC}	6 ns	50 pF	1 kΩ	open	GND	V _{CC}
74HCT2G66-Q100	GND to 3 V	6 ns	50 pF	1 kΩ	open	GND	V _{CC}

[1] There is no constraint on t_{r} , t_{f} with a 50 % duty factor when measuring f_{max} .

11.2. Additional dynamic characteristics

Table 12. Additional dynamic characteristics for 74HC2G66-Q100 and 74HCT2G66-Q100

GND = 0 V; $t_r = t_f = 6.0$ ns; $C_L = 50$ pF; unless otherwise specified. All typical values are measured at $T_{amb} = 25$ °C.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
THD	total harmonic distortion	f_i = 1 kHz; R_L = 10 k Ω ; see Fig. 10				
		V _{CC} = 4.5 V; V _I = 4.0 V (p-p)	-	0.04	-	%
		V _{CC} = 9.0 V; V _I = 8.0 V (p-p)	-	0.02	-	%
		f_i = 10 kHz; R_L = 10 kΩ; see <u>Fig. 10</u>				
		V _{CC} = 4.5 V; V _I = 4.0 V (p-p)	-	0.12	-	%
		V _{CC} = 9.0 V; V _I = 8.0 V (p-p)	-	0.06	-	%
f _(-3dB)	-3 dB frequency response	$R_L = 50 \Omega$; $C_L = 10 pF$; see Fig. 11 and Fig. 12				
		V _{CC} = 4.5 V	-	180	-	MHz
		V _{CC} = 9.0 V	-	200	-	MHz
α_{iso}	isolation (OFF-state)	$R_L = 600 \Omega$; $f_i = 1 MHz$; see Fig. 13 and Fig. 14				
		V _{CC} = 4.5 V	-	-50	-	dB
		V _{CC} = 9.0 V	-	-50	-	dB
V _{ct}	crosstalk voltage	between digital input and switch (peak to peak value); $R_L = 600 \Omega$; $f_i = 1 MHz$; see Fig. 15				
		V _{CC} = 4.5 V	-	110	-	mV
		V _{CC} = 9.0 V	-	220	-	mV
Xtalk	crosstalk	between switches; R_L = 600 Ω ; f_i = 1 MHz; see Fig. 16				
		V _{CC} = 4.5 V	-	-60	-	dB
		V _{CC} = 9.0 V	-	-60	-	dB

11.3. Test circuits and graphs

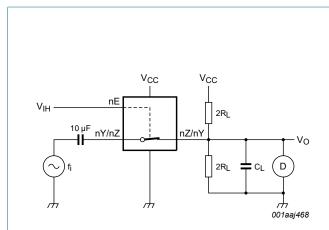
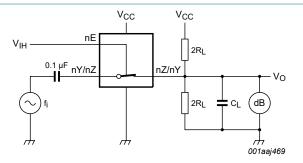
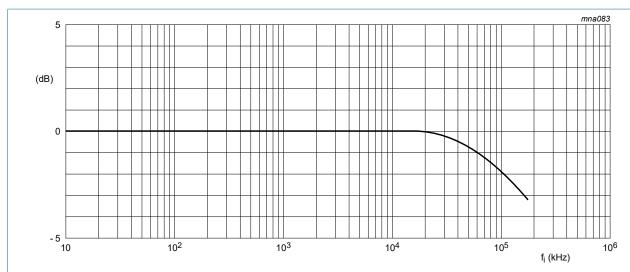


Fig. 10. Test circuit for measuring total harmonic distortion



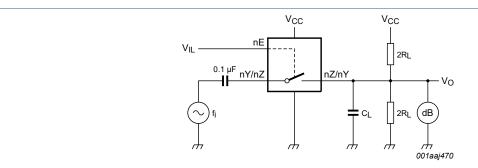
With f_i = 1 MHz adjust the switch input voltage for a 0 dBm level at the switch output, (0 dBm = 1 mW into 50 Ω). Then Increase the input frequency until the dB meter reads -3 dB.

Fig. 11. Test circuit for measuring the -3 dB frequency response



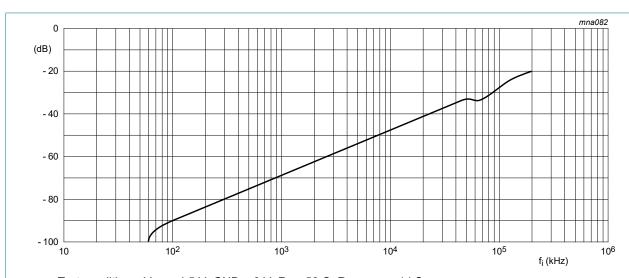
Test conditions: V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω ; R_{SOURCE} = 1 k Ω .

Fig. 12. Typical -3 dB frequency response



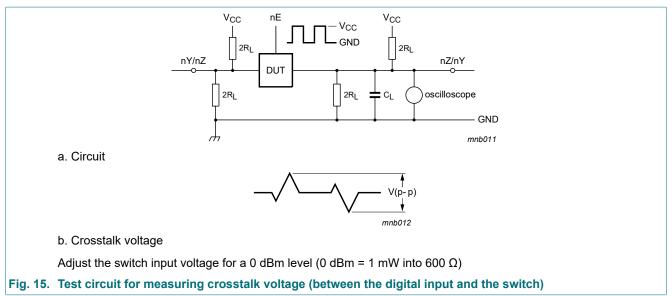
Adjust the switch input voltage for a 0 dBm level (0 dBm = 1 mW into 600 Ω)

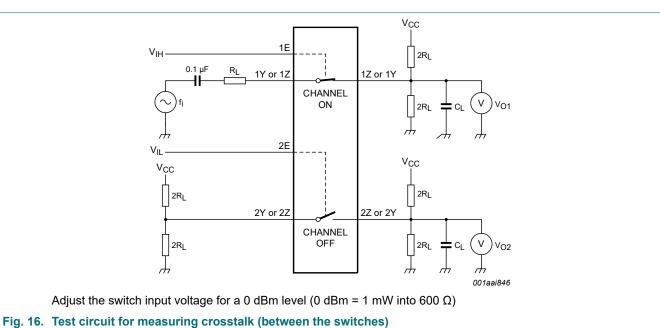
Fig. 13. Test circuit for measuring isolation (OFF-state)



Test conditions: V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω ; R_{SOURCE} = 1 k Ω .

Fig. 14. Typical isolation (OFF-state) as a function of frequency





12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

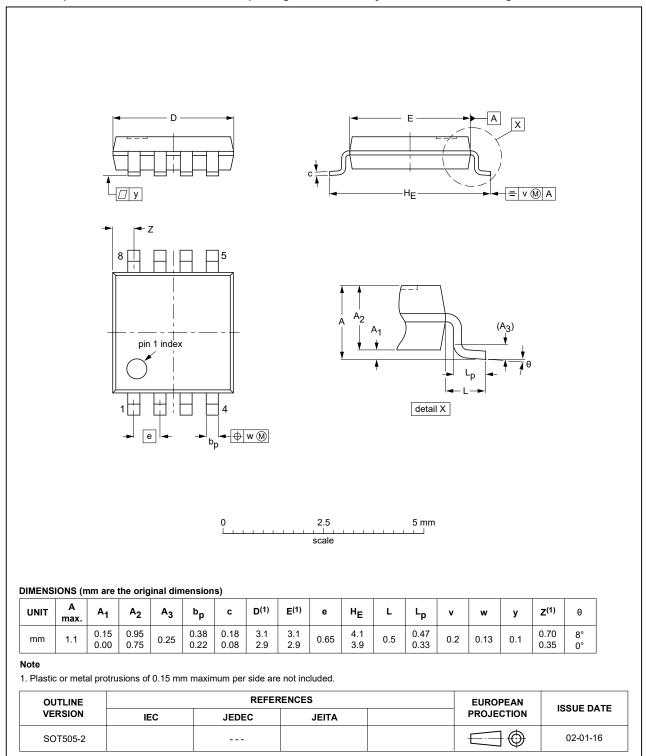


Fig. 17. Package outline SOT505-2 (TSSOP8)

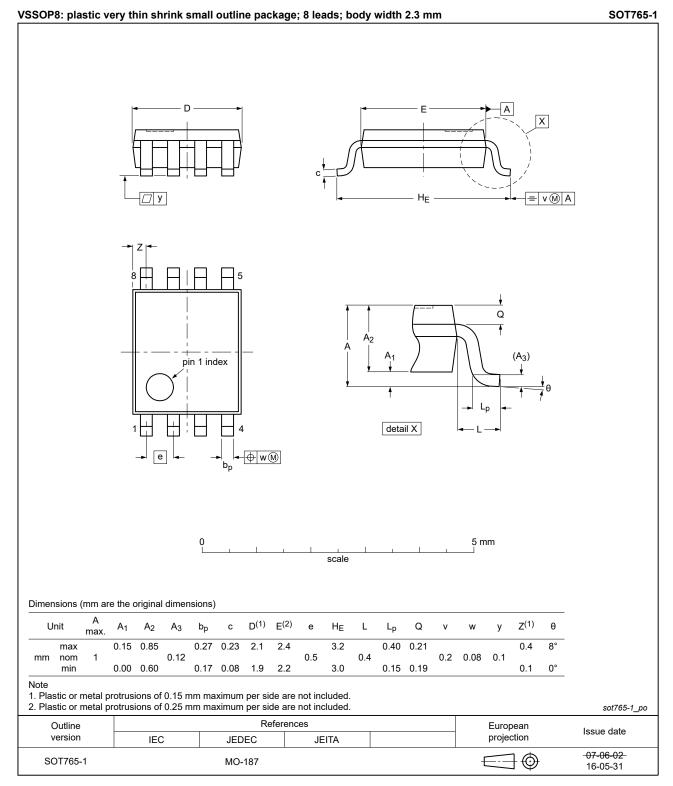


Fig. 18. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT2G66_Q100 v.3	20231121	Product data sheet	-	74HC_HCT2G66_Q100 v.2	
Modifications:	 <u>Section 2</u> updated. <u>Section 2</u>: ESD specification updated according to the latest JEDEC standard. <u>Section 8</u>: Derating values for P_{tot} total power dissipation updated. 				
74HC_HCT2G66_Q100 v.2	20181106	Product data sheet	-	74HC_HCT2G66_Q100 v.1	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Corrected Fig. 2 Package outline drawing SOT765-1 updated 				
74HC_HCT2G66_Q100 v.1	20131118	Product data sheet	-	-	

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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