

HEF4070B

Quad 2-input EXCLUSIVE-OR gate

Rev. 7 — 5 September 2024

Product data sheet

1. General description

The HEF4070B is a quad 2-input EXCLUSIVE-OR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD} .

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- CMOS low power dissipation
- High noise immunity
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$

3. Applications

- Logical comparators
- Parity checkers and generators

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
HEF4070BT	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

5. Functional diagram

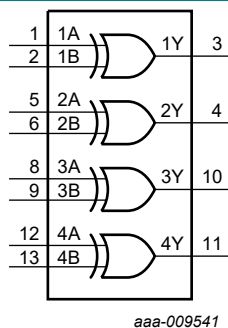


Fig. 1. Functional diagram

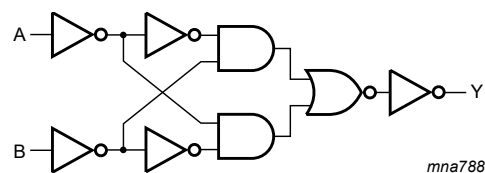


Fig. 2. Logic diagram (one gate)

6. Pinning information

6.1. Pinning

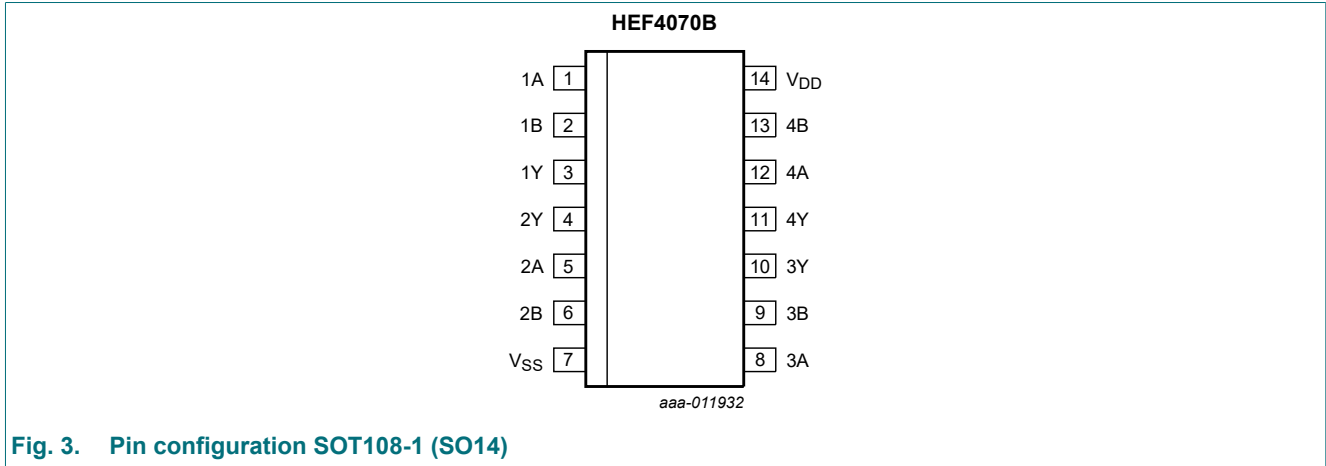


Fig. 3. Pin configuration SOT108-1 (SO14)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 5, 8, 12	data input
1B, 2B, 3B, 4B	2, 6, 9, 13	data input
1Y, 2Y, 3Y, 4Y	3, 4, 10, 11	data output
V _{SS}	7	ground (0 V)
V _{DD}	14	supply voltage

7. Functional description

Table 3. Functional table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0\text{ V}$ (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	± 10	mA
$I_{I/O}$	input/output current		-	± 10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$	-	500	mW
P	power dissipation	per output	-	100	mW

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	15	V
V_I	input voltage		0	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	0.08	$\mu\text{s/V}$

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} , unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = +25 °C		T _{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	µA
I _{DD}	supply current	all valid input combinations; I _O = 0 A	5 V	-	1.0	-	1.0	-	7.5	µA
			10 V	-	2.0	-	2.0	-	15.0	µA
			15 V	-	4.0	-	4.0	-	30.0	µA
C _I	input capacitance			-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = 25 °C, unless otherwise specified. For waveforms see Fig. 4; for test circuit see Fig. 5.

Symbol	Parameter[1]	Conditions	V _{DD}	Extrapolation formula	Min	Typ	Max	Unit
t _{PHL}	HIGH to LOW propagation delay	nA or nB to nY	5 V	58 ns + (0.55 ns/pF)C _L	-	85	175	ns
			10 V	24 ns + (0.23 ns/pF)C _L	-	35	75	ns
			15 V	21 ns + (0.16 ns/pF)C _L	-	30	55	ns
t _{PLH}	LOW to HIGH propagation delay	nA or nB to nY	5 V	43 ns + (0.55 ns/pF)C _L	-	75	150	ns
			10 V	19 ns + (0.23 ns/pF)C _L	-	30	65	ns
			15 V	17 ns + (0.16 ns/pF)C _L	-	25	50	ns
t _t	transition time		5 V [2]	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
			10 V [2]	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V [2]	6 ns + (0.28 ns/pF)C _L	-	20	40	ns

[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

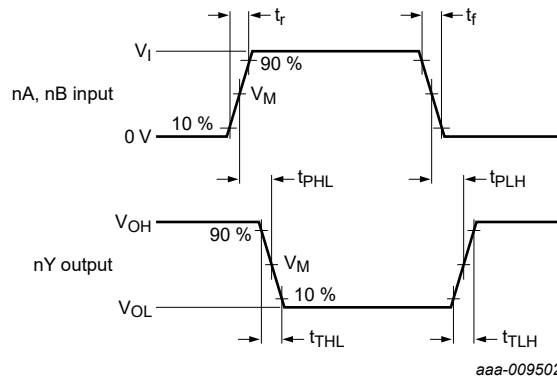
[2] t_t is the same as t_{THL} and t_{TLH}.

Table 8. Dynamic power dissipation

V_{SS} = 0 V; t_r = t_f ≤ 20 ns; T_{amb} = 25 °C.

Symbol	Parameter	V _{DD}	Typical formula	where:
P _D	dynamic power dissipation	5 V	P _D = 1100 × f _i + Σ(f _o × C _L) × V _{DD} ² (µW)	f _i = input frequency in MHz; f _o = output frequency in MHz; C _L = output load capacitance in pF; Σ(f _o × C _L) = sum of the outputs; V _{DD} = supply voltage in V.
		10 V	P _D = 4900 × f _i + Σ(f _o × C _L) × V _{DD} ² (µW)	
		15 V	P _D = 14400 × f _i + Σ(f _o × C _L) × V _{DD} ² (µW)	

11.1. Waveforms



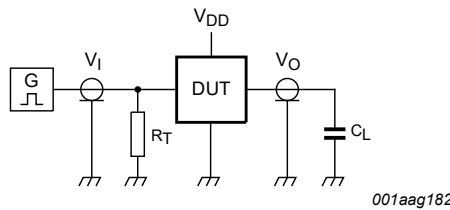
Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. Input to output propagation delay and output transition times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$



Test data is given in [Table 10](#).

Definitions test circuit:

C_L = load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 5. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

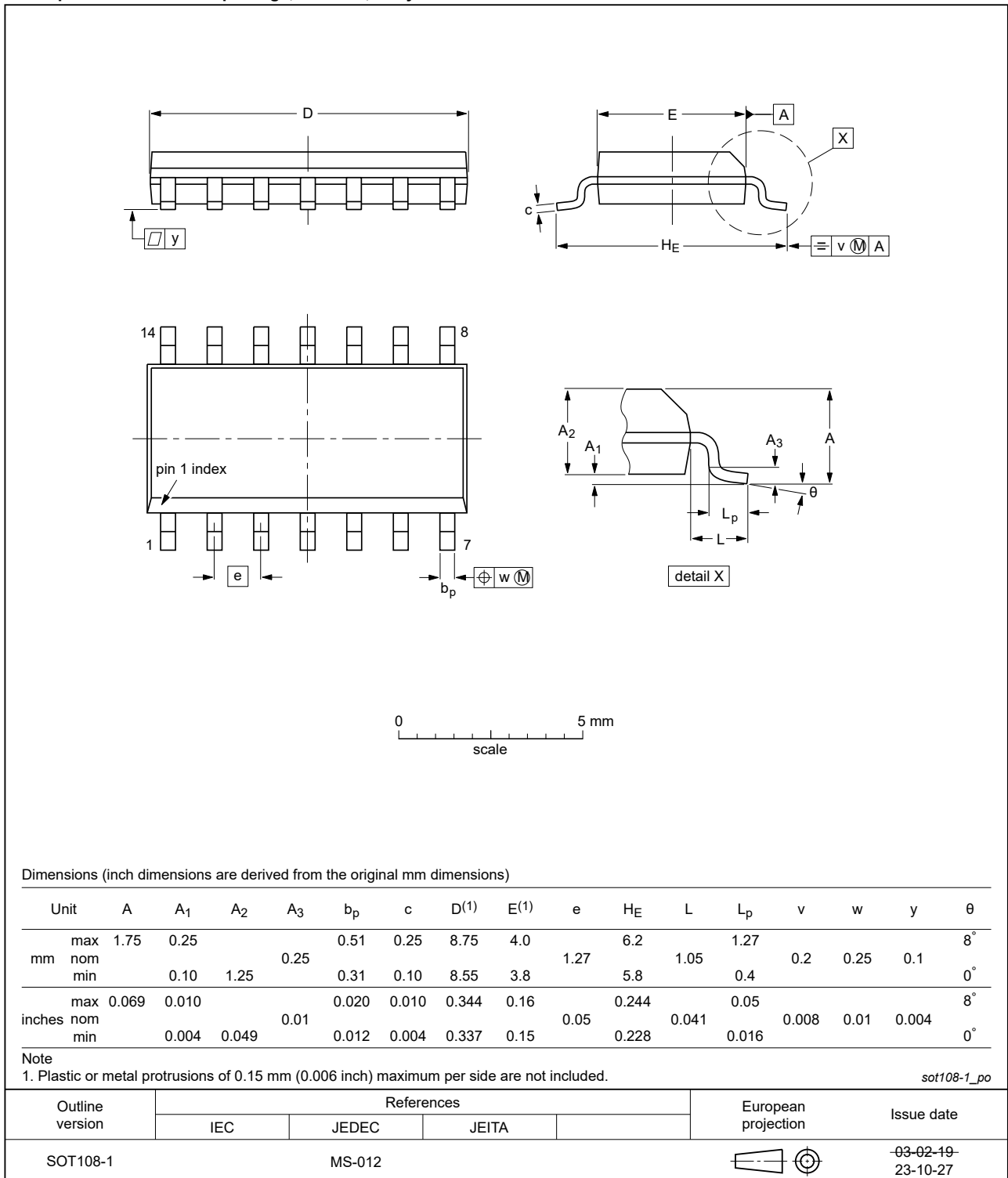


Fig. 6. Package outline SOT108-1 (SO14)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4070B v.7	20240905	Product data sheet	-	HEF4070B v.6
Modifications:	<ul style="list-style-type: none"> • Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 6: Aligned SO package outline drawing to JEDEC MS-012 			
HEF4070B v.6	20220214	Product data sheet	-	HEF4070B v.5
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. 			
HEF4070B v.5	20151216	Product data sheet	-	HEF4070B v.4
Modifications:	<ul style="list-style-type: none"> • Type number HEF4070BP (SOT27-1) removed. 			
HEF4070B v.4	20140327	Product data sheet	-	HEF4070B_CNV v.3
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. 			
HEF4070B_CNV v.3	19950101	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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