



# PDTC144EU

50 V, 100 mA NPN resistor-equipped transistor;

R1 = 47 k $\Omega$ , R2 = 47 k $\Omega$

11 July 2023

Product data sheet

## 1. General description

NPN Resistor-Equipped Transistor (RET) in a very small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTA144EU

## 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

## 3. Applications

- Digital application in industrial segments
- Cost-saving alternative for BC847 series in digital applications
- Controlling IC inputs
- Switching loads

## 4. Quick reference data

Table 1. Quick reference data

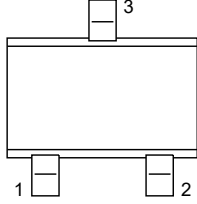
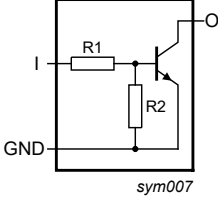
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	50	V
I <sub>O</sub>	output current		-	-	100	mA
R1	bias resistor 1 (input)	[1]	33	47	61	k $\Omega$
R2/R1	bias resistor ratio	[1]	0.8	1	1.2	

[1] See "Section 11: Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN resistor-equipped transistor; R1 = 47 kΩ, R2 = 47 kΩ

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 SC-70 (SOT323)	 sym007
2	GND	ground (emitter)		
3	O	output (collector)		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
<a href="#">PDTC144EU</a>	SC-70	plastic, surface-mounted package; 3 leads; 1.3 mm pitch; 2 mm x 1.25 mm x 0.95 mm body	<a href="#">SOT323</a>

## 7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PDTC144EU	%08

[1] % = placeholder for manufacturing site code

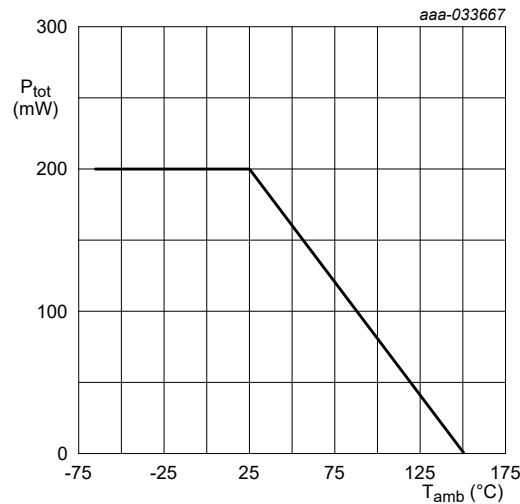
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CBO}$	collector-base voltage	open emitter	-	50	V
$V_{CEO}$	collector-emitter voltage	open base	-	50	V
$V_{EBO}$	emitter-base voltage	open collector	-	10	V
$V_I$	input voltage		-10	40	V
$I_O$	output current		-	100	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	200	mW
$T_j$	junction temperature		-	150	°C
$T_{amb}$	ambient temperature		-65	150	°C
$T_{stg}$	storage temperature		-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

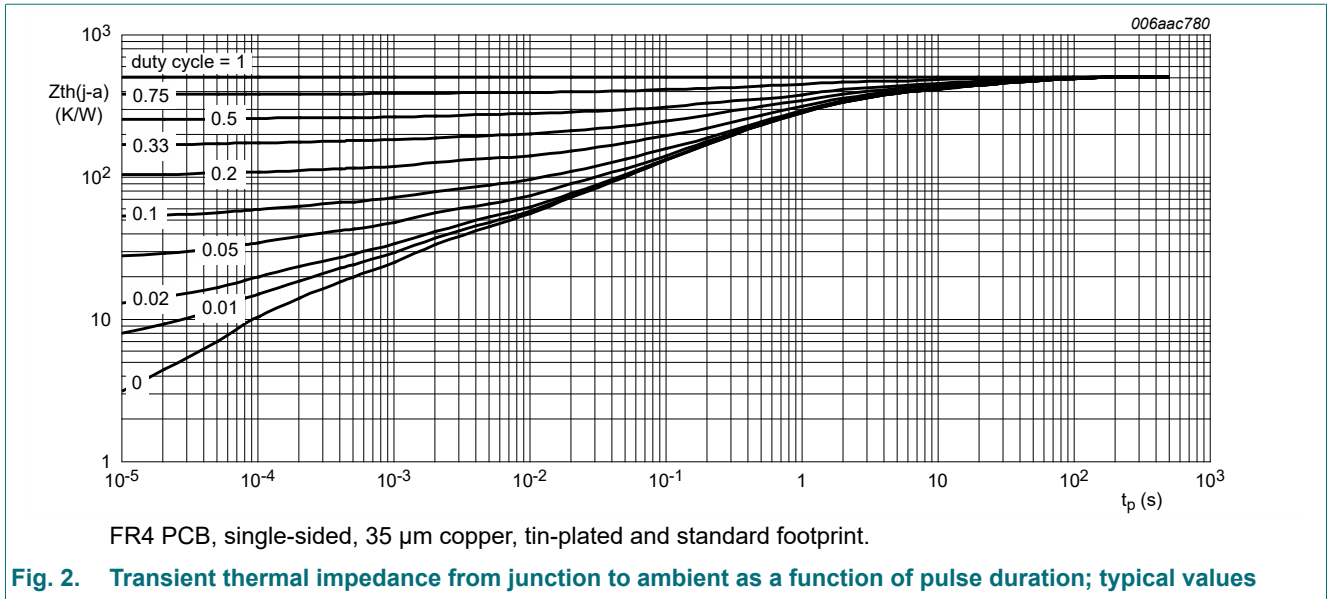
**Fig. 1. Power derating curve**

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.

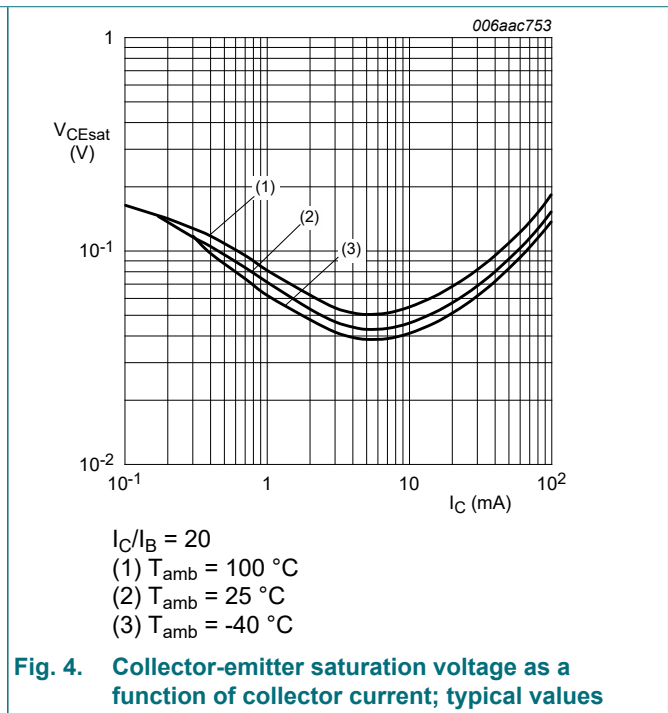
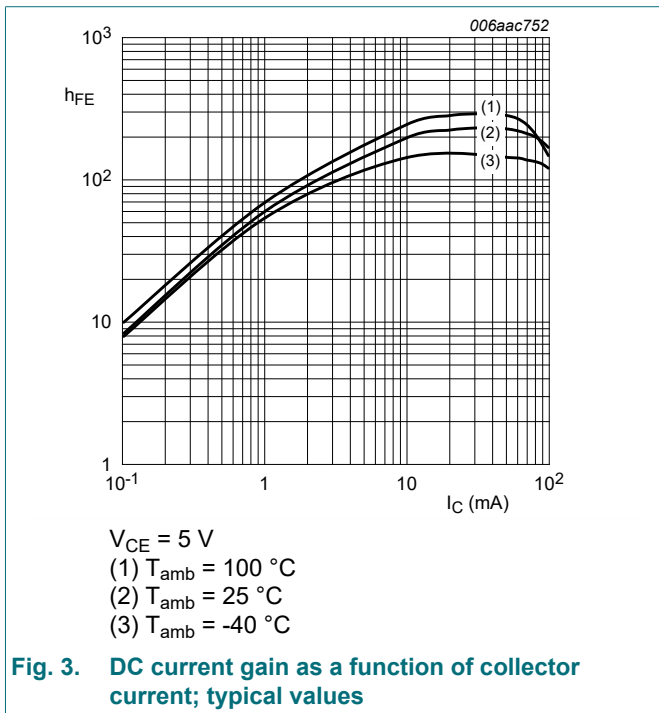


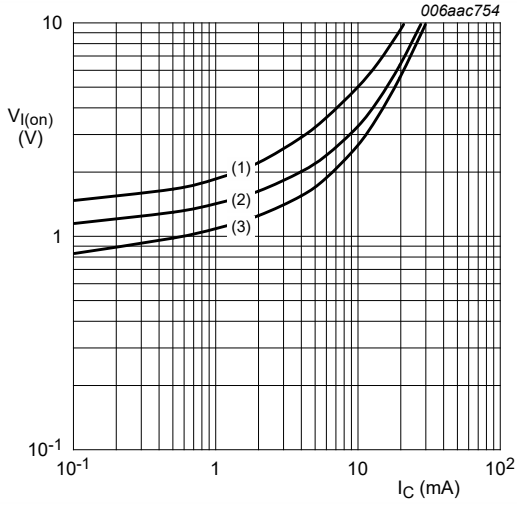
## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100 \mu A; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$	50	-	-	V	
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}; I_B = 0 A; T_{amb} = 25 \text{ }^\circ C$	50	-	-	V	
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50 \text{ V}; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	100	nA	
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}; I_B = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	100	nA	
		$V_{CE} = 30 \text{ V}; I_B = 0 A; T_j = 150 \text{ }^\circ C$	-	-	5	$\mu A$	
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_C = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	90	$\mu A$	
$h_{FE}$	DC current gain	$V_{CE} = 5 \text{ V}; I_C = 5 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	80	-	-		
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10 \text{ mA}; I_B = 0.5 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	-	-	150	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5 \text{ V}; I_C = 100 \mu A; T_{amb} = 25 \text{ }^\circ C$	-	1.2	0.8	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3 \text{ V}; I_C = 2 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	3	1.6	-	V	
R1	bias resistor 1 (input)		[1]	33	47	61	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
$C_c$	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 A; i_e = 0 A; f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ C$	-	-	2.5	pF	
$f_T$	transition frequency	$V_{CE} = 5 \text{ V}; I_C = 10 \text{ mA}; f = 100 \text{ MHz}; T_{amb} = 25 \text{ }^\circ C$	[2]	-	230	MHz	

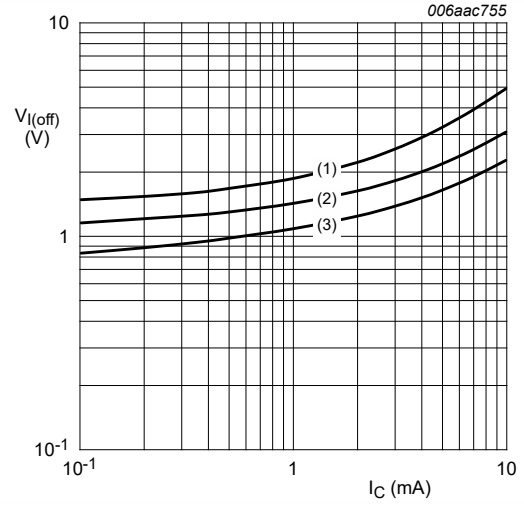
- [1] See "Section 11: Test information" for resistor calculation and test conditions.
- [2] Characteristics of built-in transistor.





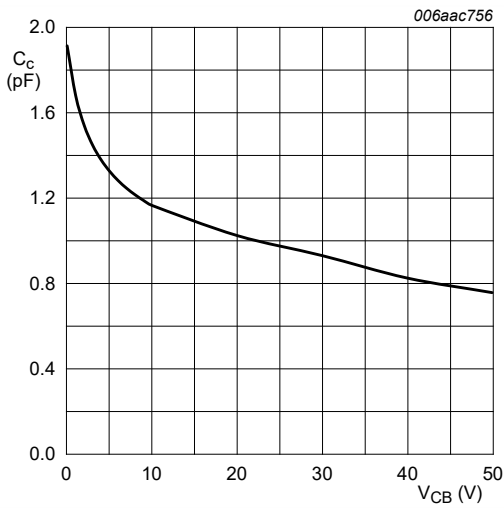
$V_{CE} = 0.3 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig. 5. On-state input voltage as a function of collector current; typical values**



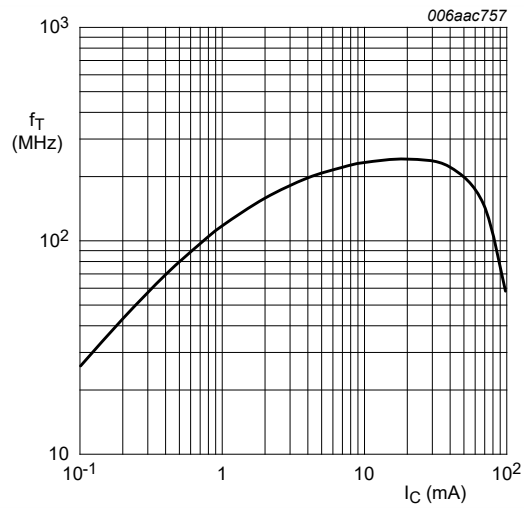
$V_{CE} = 5 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig. 6. Off-state input voltage as a function of collector current; typical values**



$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig. 7. Collector capacitance as a function of collector-base voltage; typical values**



$V_{CE} = 5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor**

## 11. Test information

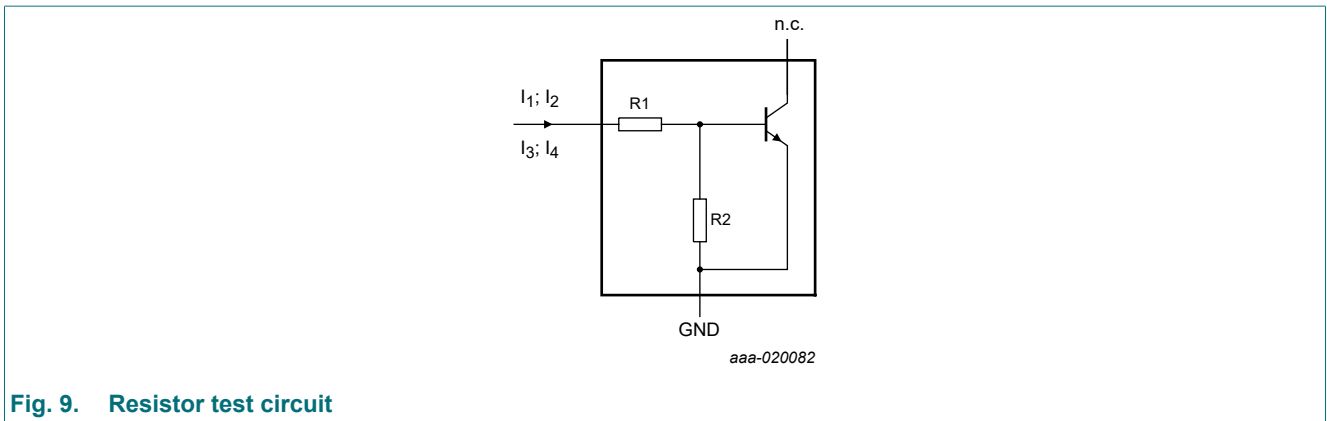
### Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$



**Fig. 9. Resistor test circuit**

### Resistor test conditions

**Table 8. Resistor test conditions**

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>
PDTC144EU	47	47	55 μA	105 μA	-55 μA	-105 μA

## 12. Package outline

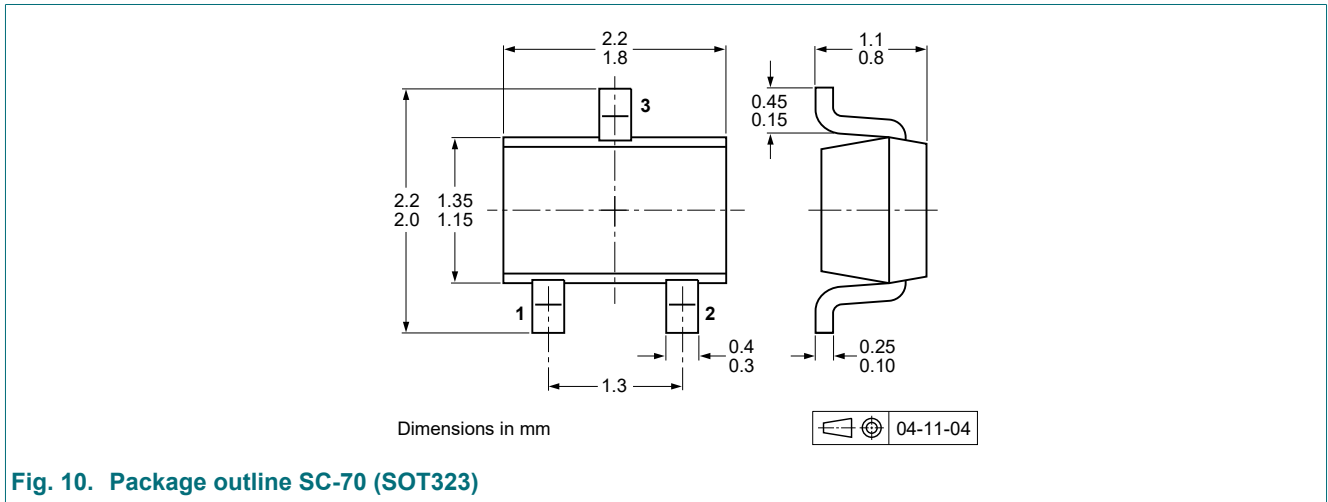


Fig. 10. Package outline SC-70 (SOT323)

## 13. Soldering

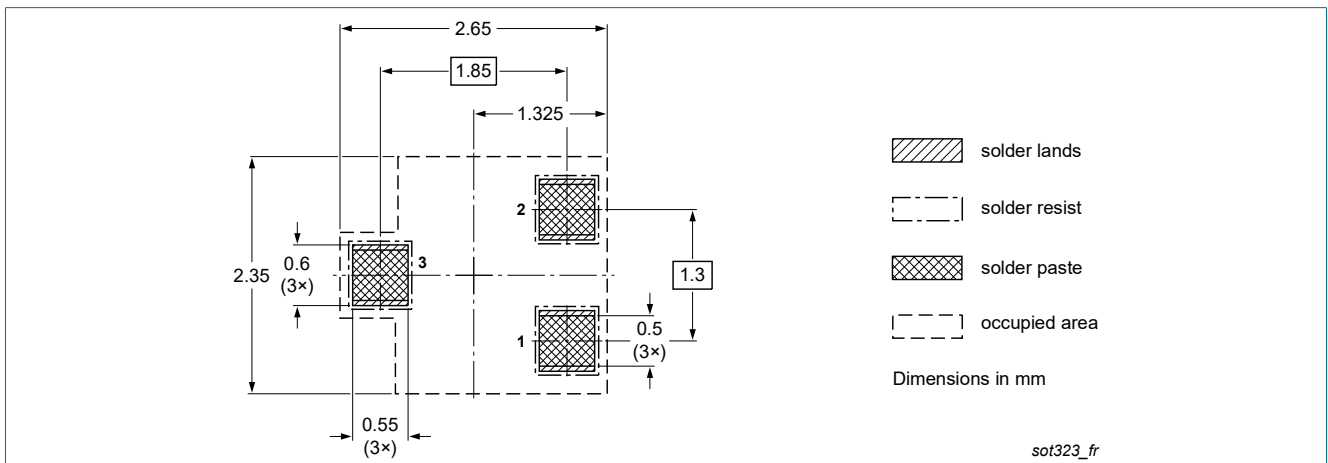


Fig. 11. Reflow soldering footprint for SC-70 (SOT323)

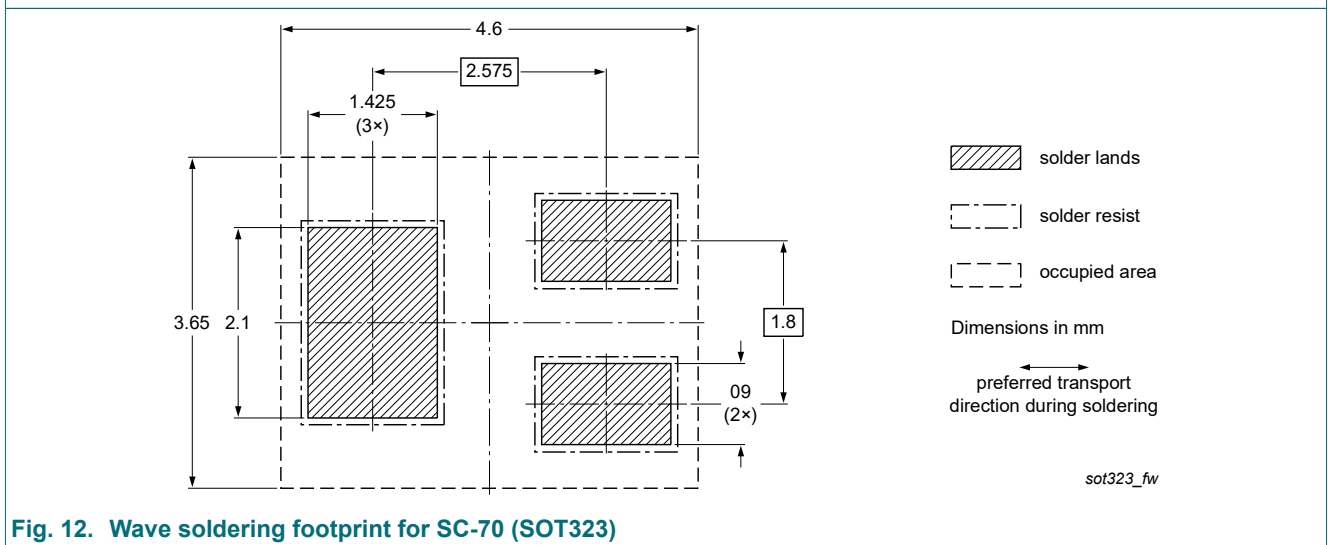


Fig. 12. Wave soldering footprint for SC-70 (SOT323)



## 14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTC144EU v.10	20230711	Product data sheet	-	PDTC144E_SER v.9
Modification:	<ul style="list-style-type: none"> <li>Family data sheet reduced to single type data sheet.</li> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Product changed to non automotive. Please refer to the automotive product(s) with -Q.</li> <li>Packing information removed.</li> </ul>			
PDTC144E_SER v.9	20040318	Product specification	-	PDTC144E_SERIES v.8
PDTC144E_SERIES v.8	20040112	Product specification	-	PDTC144E_SERIES v.7
PDTC144E_SERIES v.7	20030910	Product specification	-	PDTC144E_SERIES v.6
PDTC144E_SERIES v.6	20030410	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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