



PBSS4160DPN

60 V, 1 A NPN/PNP low V_{CEsat} transistor

3 March 2025

Product data sheet

1. General description

NPN/PNP low V_{CEsat} transistor pair in a SOT457 (SC-74) Surface Mounted Device (SMD) plastic package.

2. Features and benefits

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability: I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors
- AEC-Q101 qualified

3. Applications

- Complementary MOSFET driver
- Half and full bridge motor drivers
- Dual low power switches (e.g. motors, fans)
- Automotive applications

4. Quick reference data

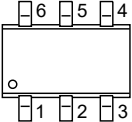
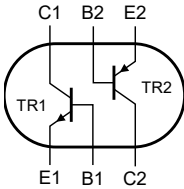
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor unless otherwise specified; for the PNP transistor with negative polarity							
V _{CEO}	collector-emitter voltage	open base		-	-	60	V
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms		-	-	2	A
TR1 (NPN)							
I _C	collector current		[1]	-	-	1	A
R _{CEsat}	collector-emitter saturation resistance	I _C = 1 A; I _B = 100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C		-	200	250	mΩ
TR2 (PNP)							
I _C	collector current		[1]	-	-	-900	mA
R _{CEsat}	collector-emitter saturation resistance	I _C = -1 A; I _B = -100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C		-	250	330	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 TSOP6 (SOT457)	 sym139
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4160DPN	TSOP6	plastic, surface-mounted package (SC-74; TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

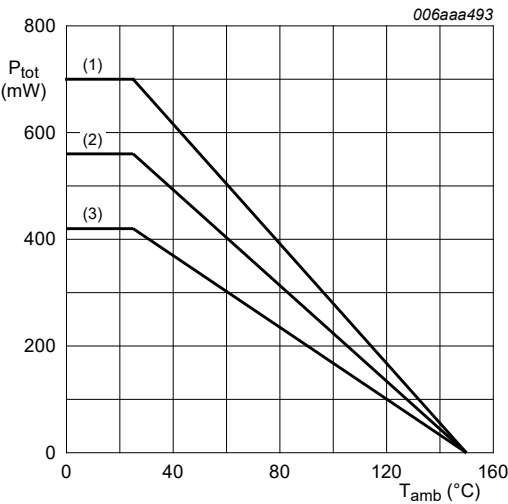
Type number	Marking code
PBSS4160DPN	B4

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor unless otherwise specified; for the PNP transistor with negative polarity						
V _{CBO}	collector-base voltage	open emitter		-	80	V
V _{CEO}	collector-emitter voltage	open base		-	60	V
V _{EBO}	emitter-base voltage	open collector		-	5	V
I _C	collector current		[1]	-	1	A
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms		-	2	A
I _B	base current			-	300	mA
I _{BM}	peak base current	single pulse; t _p ≤ 1 ms		-	1	A
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[2]	-	290	mW
			[3]	-	370	mW
			[1]	-	450	mW
TR1 (NPN)						
I _C	collector current		[2]	-	870	mA
			[3]	-	1	A
TR2 (PNP)						
I _C	collector current		[2]	-	-770	mA
			[3]	-	-900	mA
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[2]	-	420	mW
			[3]	-	560	mW
			[1]	-	700	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².



- (1) Ceramic PCB, Al₂O₃, standard footprint
- (2) FR4 PCB, mounting pad for collector 1 cm²
- (3) FR4 PCB, standard footprint

Fig. 1. Power derating curves

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	431	K/W
			[2]	-	-	338	K/W
			[3]	-	-	278	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	105	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

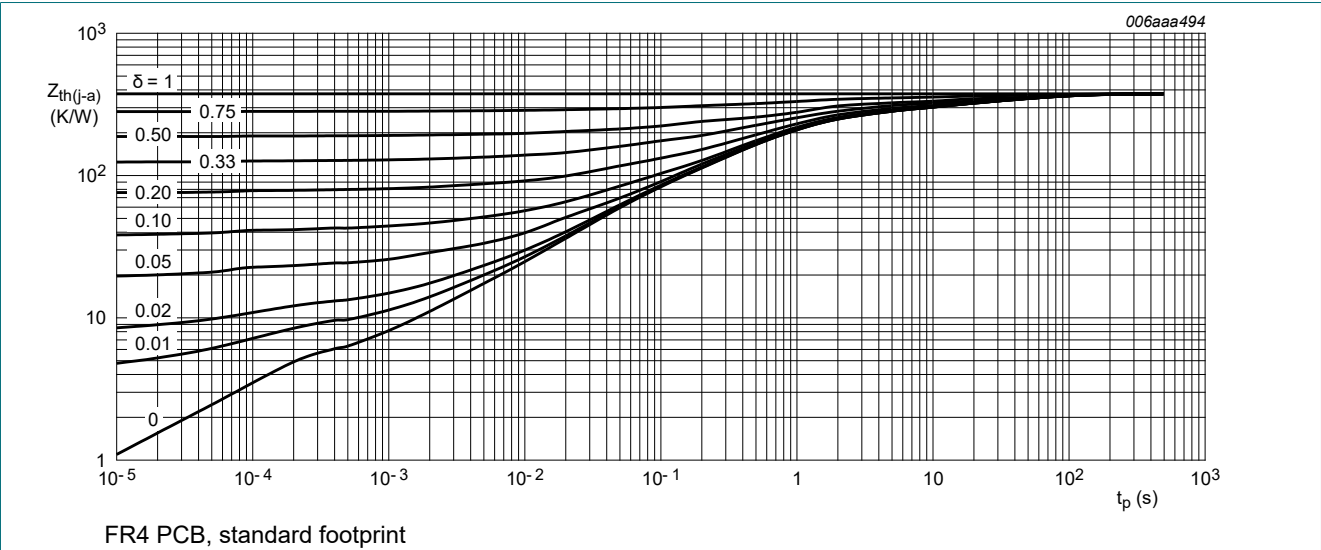


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

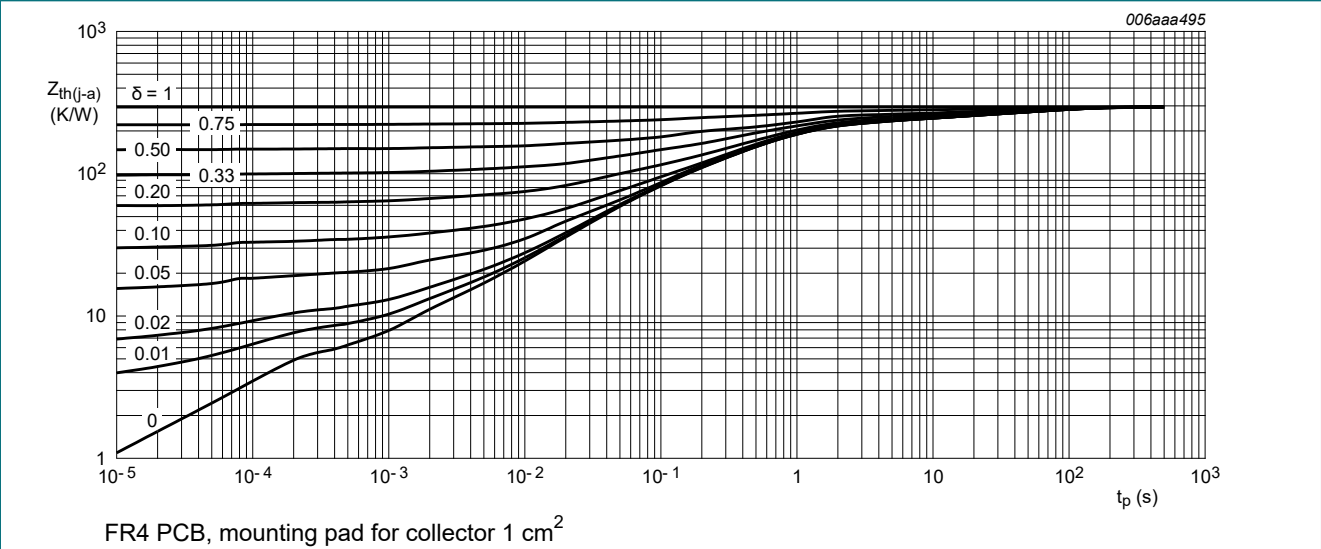
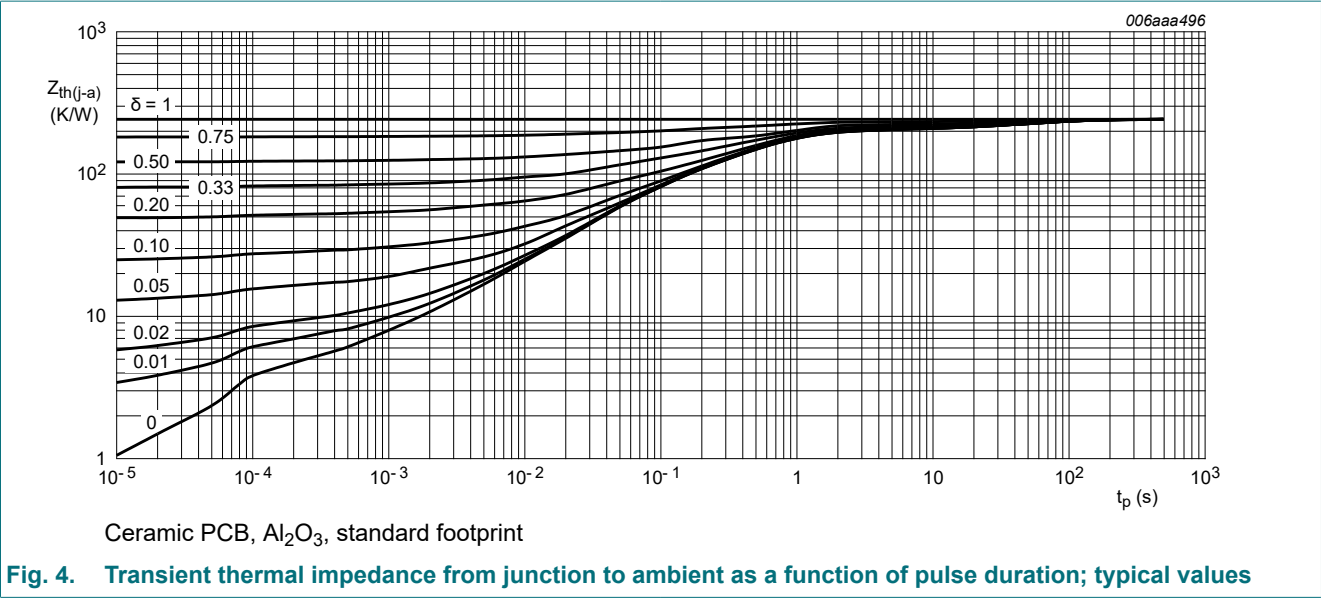


Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

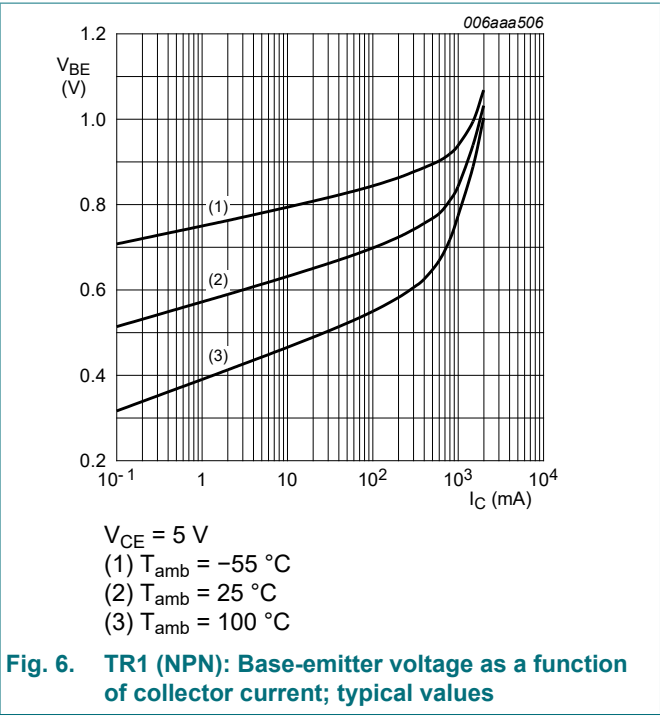
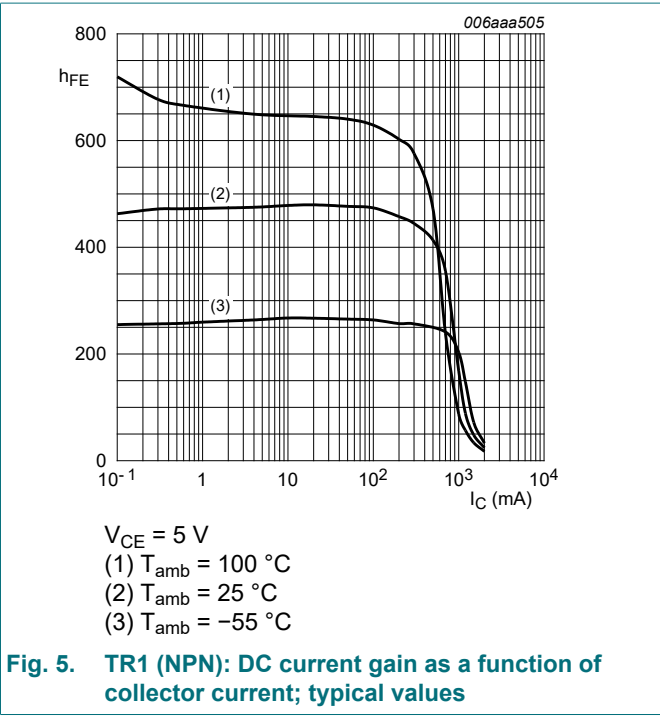


10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor unless otherwise specified; for the PNP transistor with negative polarity							
I _{CBO}	collector-base cut-off current	V _{CB} = 60 V; I _E = 0 A; T _{amb} = 25 °C		-	-	100	nA
		V _{CB} = 60 V; I _E = 0 A; T _j = 150 °C		-	-	50	µA
I _{CES}	collector-emitter cut-off current	V _{CE} = 60 V; V _{BE} = 0 V; T _{amb} = 25 °C		-	-	100	nA
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A; T _{amb} = 25 °C		-	-	100	nA
TR1 (NPN)							
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 1 mA; T _{amb} = 25 °C		250	500	-	
		V _{CE} = 5 V; I _C = 500 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		200	420	-	
		V _{CE} = 5 V; I _C = 1 A; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		100	180	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = 100 mA; I _B = 1 mA; T _{amb} = 25 °C		-	90	110	mV
		I _C = 500 mA; I _B = 50 mA; T _{amb} = 25 °C		-	115	140	mV
		I _C = 1 A; I _B = 100 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	200	250	mV
R _{CEsat}	collector-emitter saturation resistance			-	200	250	mΩ
V _{BEsat}	base-emitter saturation voltage	I _C = 1 A; I _B = 50 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	0.95	1.1	V
V _{BEon}	base-emitter turn-on voltage	V _{CE} = 5 V; I _C = 1 A; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	0.82	0.9	V
t _d	delay time	I _C = 0.5 A; I _{Bon} = 25 mA; I _{Boff} = -25 mA; T _{amb} = 25 °C		-	11	-	ns
t _r	rise time			-	78	-	ns
t _{on}	turn-on time			-	90	-	ns
t _s	storage time			-	340	-	ns
t _f	fall time			-	160	-	ns
t _{off}	turn-off time			-	500	-	ns
f _T	transition frequency	V _{CE} = 10 V; I _C = 50 mA; f = 100 MHz; T _{amb} = 25 °C		150	220	-	MHz
C _c	collector capacitance	V _{CB} = 10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C		-	5.5	10	pF
TR2 (PNP)							
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -1 mA; T _{amb} = 25 °C		200	350	-	
		V _{CE} = -5 V; I _C = -500 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		150	250	-	
		V _{CE} = -5 V; I _C = -1 A; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		100	160	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -100 mA; I _B = -1 mA; T _{amb} = 25 °C		-	-110	-165	mV
		I _C = -500 mA; I _B = -50 mA; T _{amb} = 25 °C		-	-120	-175	mV
		I _C = -1 A; I _B = -100 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	-250	-330	mV
R _{CEsat}	collector-emitter saturation resistance			-	250	330	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BEsat}	base-emitter saturation voltage	$I_C = -1\text{ A}$; $I_B = -50\text{ mA}$; pulsed; $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-0.95	-1.1	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -5\text{ V}$; $I_C = -1\text{ A}$; pulsed; $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	-0.82	-0.9	V
t_d	delay time	$I_C = -0.5\text{ A}$; $I_{Bon} = -25\text{ mA}$; $I_{Boff} = 25\text{ mA}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	11	-	ns
t_r	rise time		-	30	-	ns
t_{on}	turn-on time		-	41	-	ns
t_s	storage time		-	205	-	ns
t_f	fall time		-	55	-	ns
t_{off}	turn-off time		-	260	-	ns
f_T	transition frequency	$V_{CE} = -10\text{ V}$; $I_C = -50\text{ mA}$; $f = 100\text{ MHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$	150	185	-	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	9	15	pF



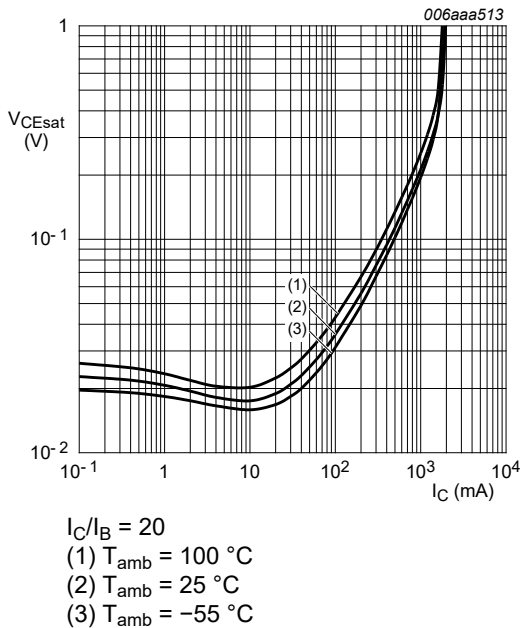


Fig. 7. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

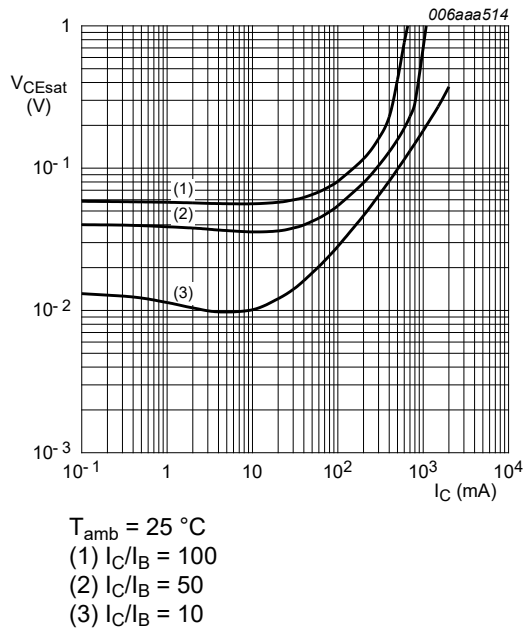


Fig. 8. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

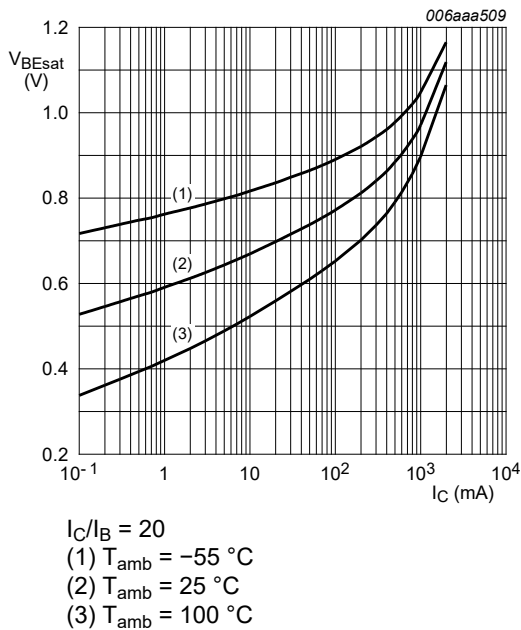


Fig. 9. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values

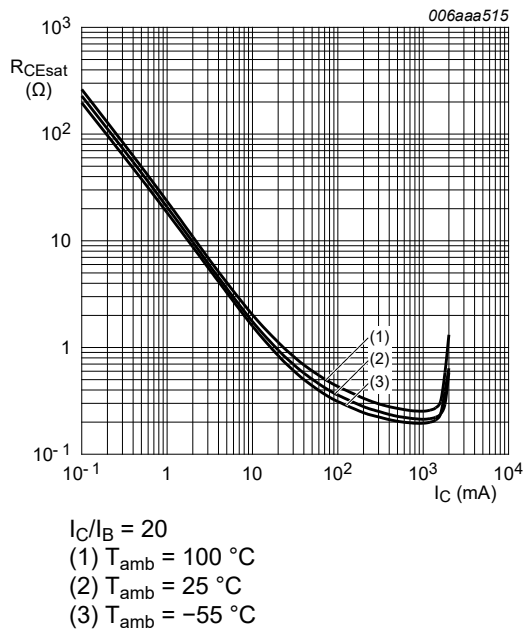


Fig. 10. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values

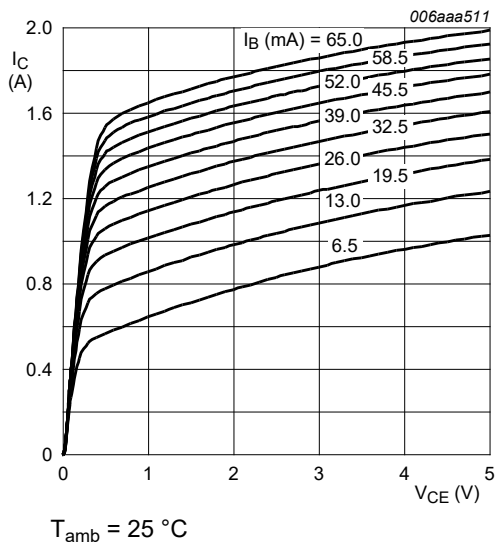


Fig. 11. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values

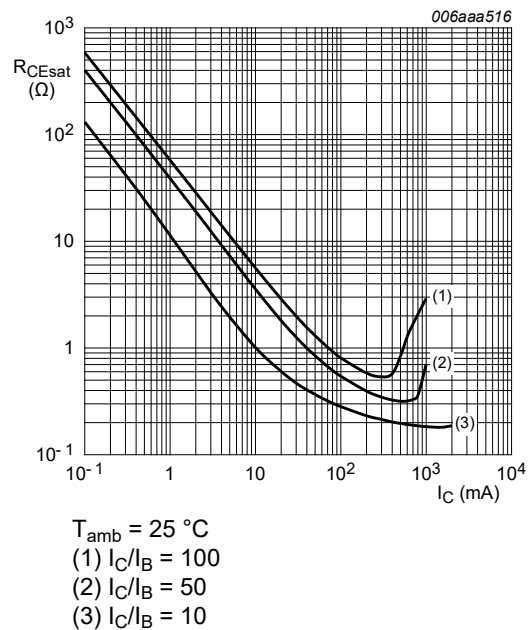


Fig. 12. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values

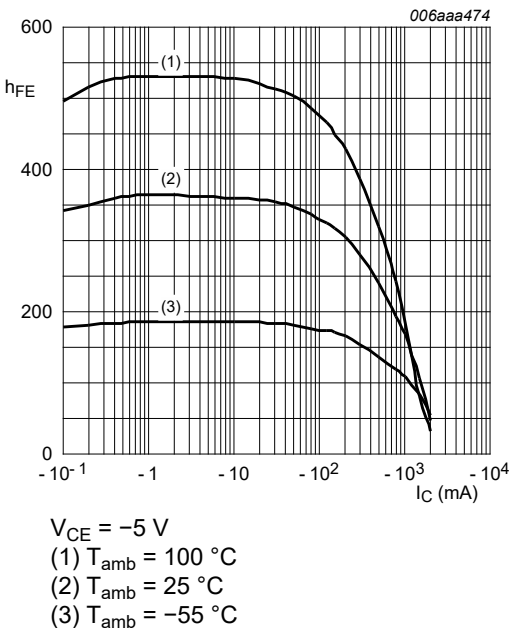


Fig. 13. TR2 (PNP): DC current gain as a function of collector current; typical values

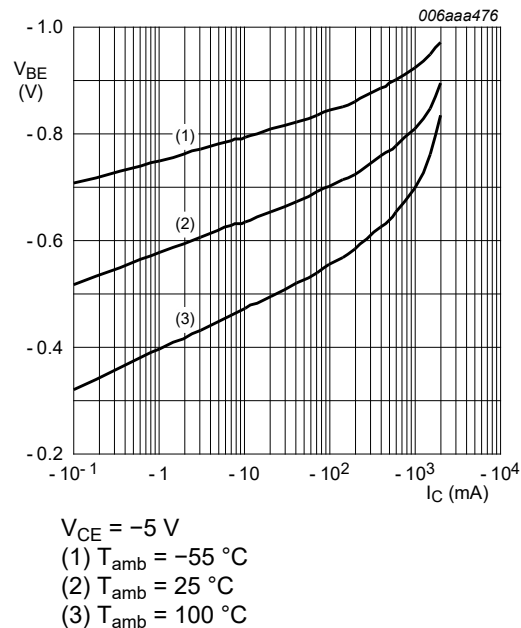


Fig. 14. TR2 (PNP): Base-emitter voltage as a function of collector current; typical values

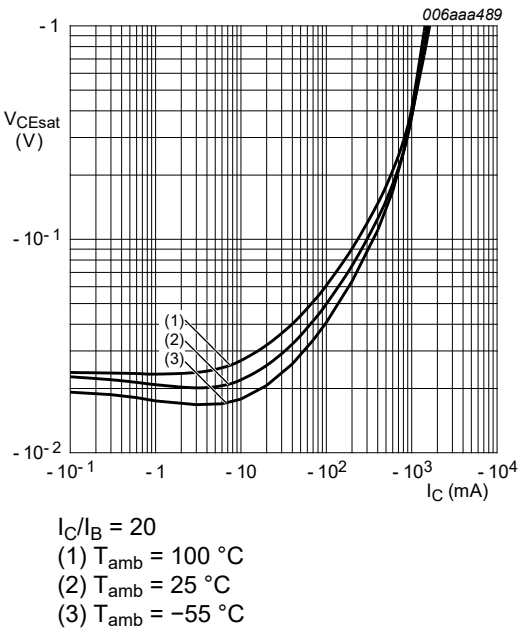


Fig. 15. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

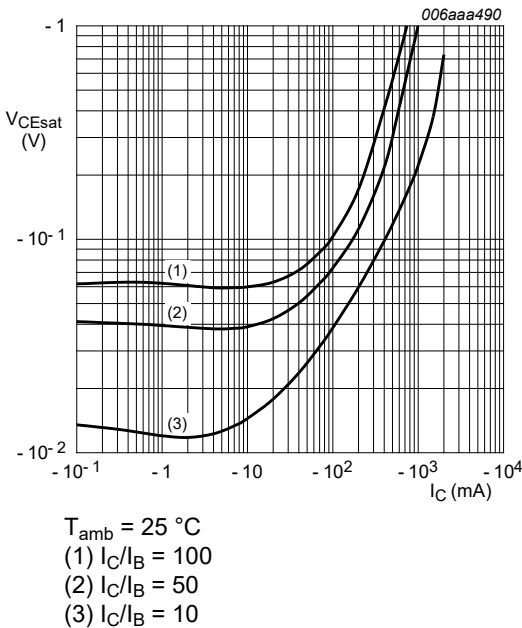


Fig. 16. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

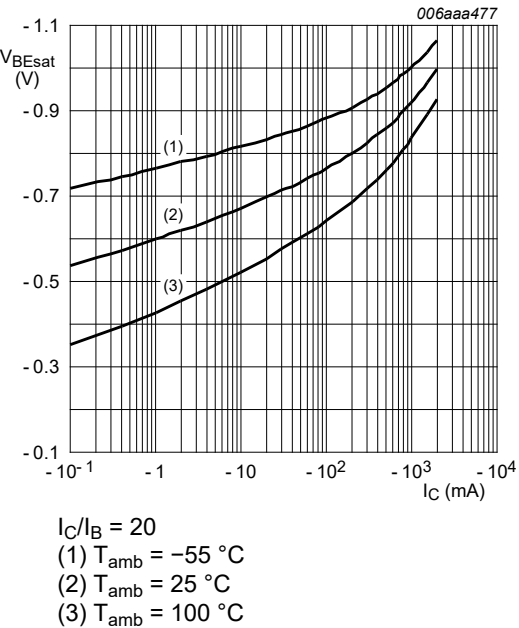


Fig. 17. TR2 (PNP): Base-emitter saturation voltage as a function of collector current; typical values

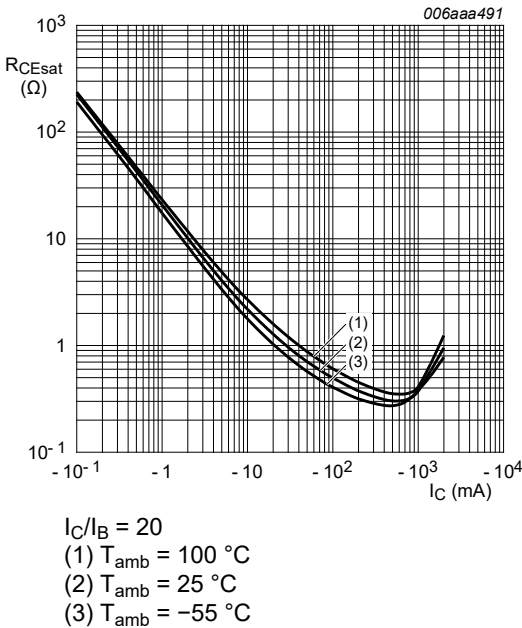


Fig. 18. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

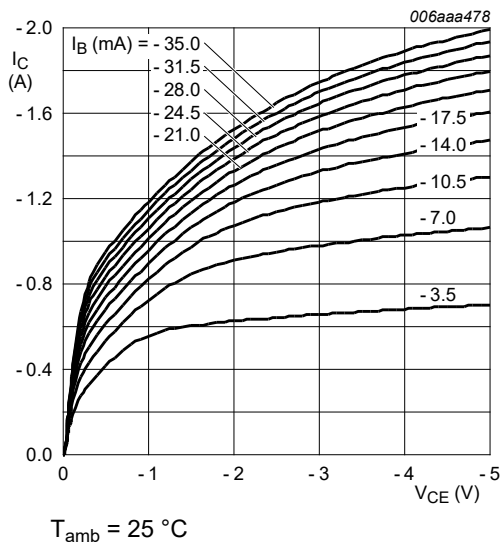


Fig. 19. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values

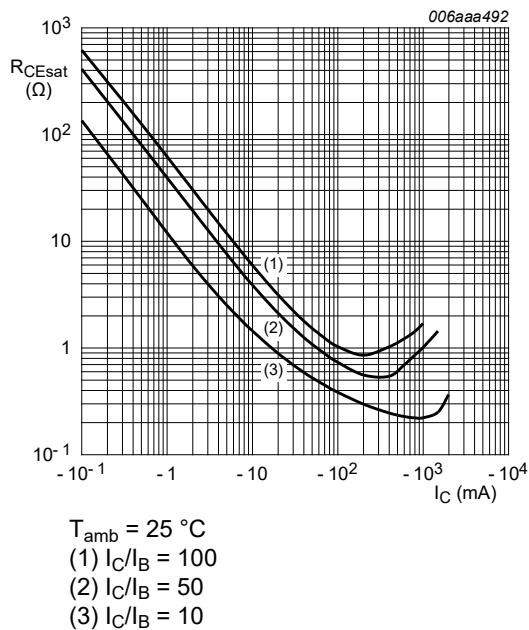


Fig. 20. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

11. Test information

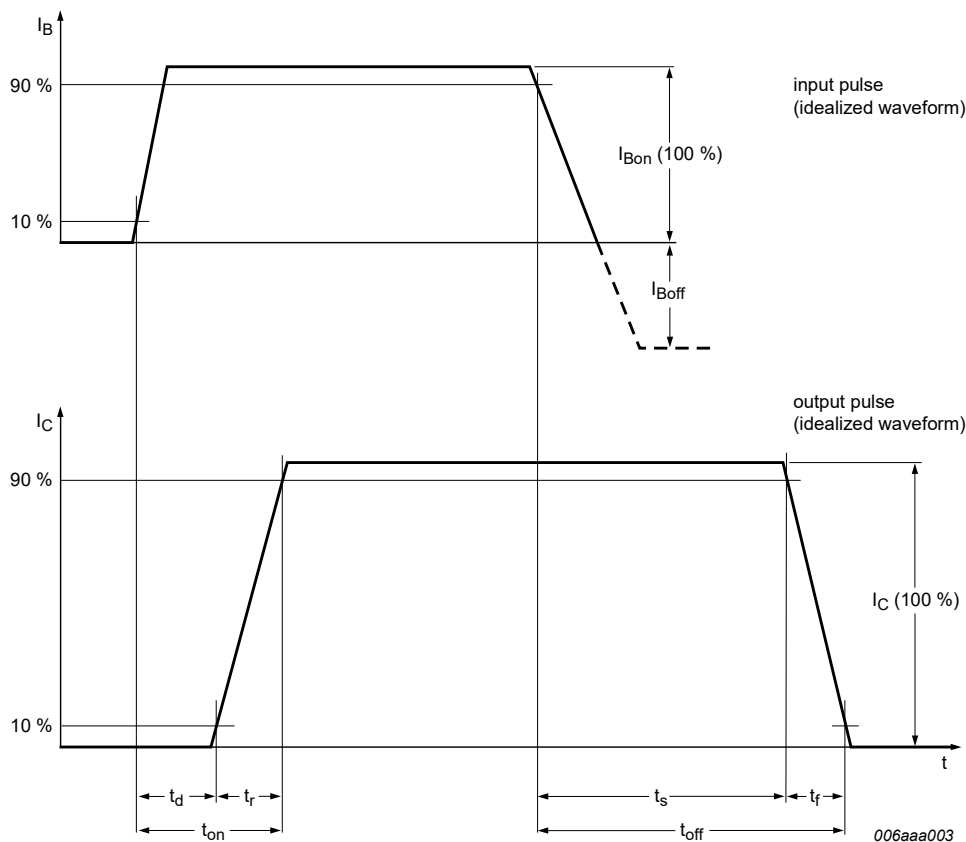


Fig. 21. TR1 (NPN): BISS transistor switching time definition

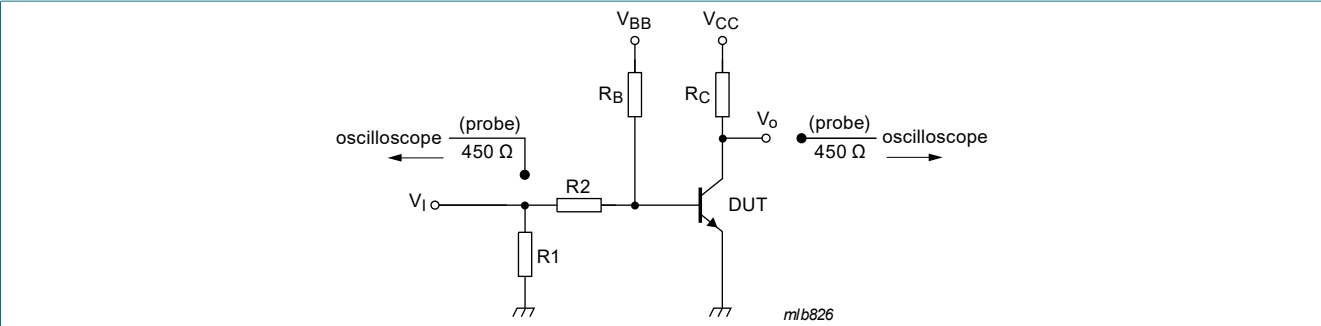


Fig. 22. TR1 (NPN): Test circuit for switching times

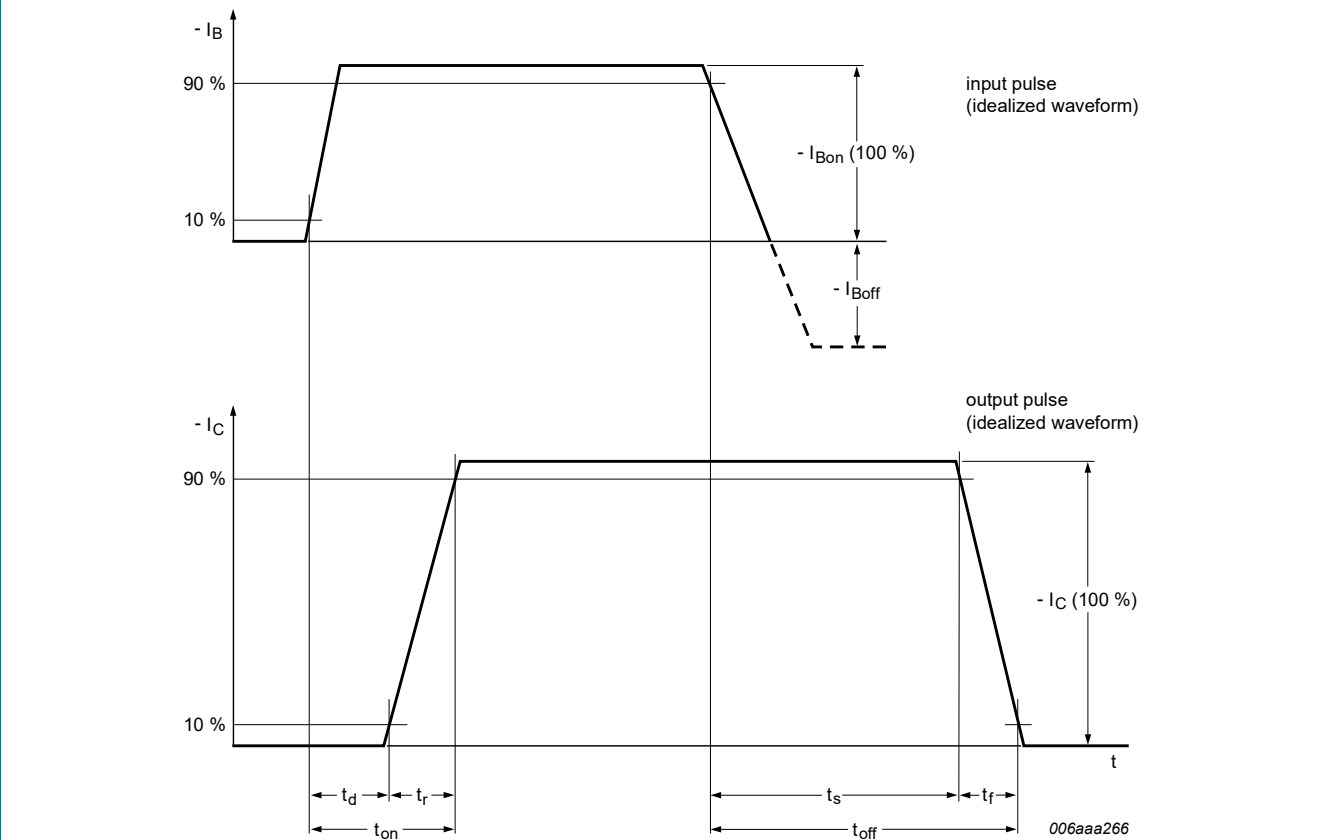


Fig. 23. TR2 (PNP): BISS transistor switching time definition

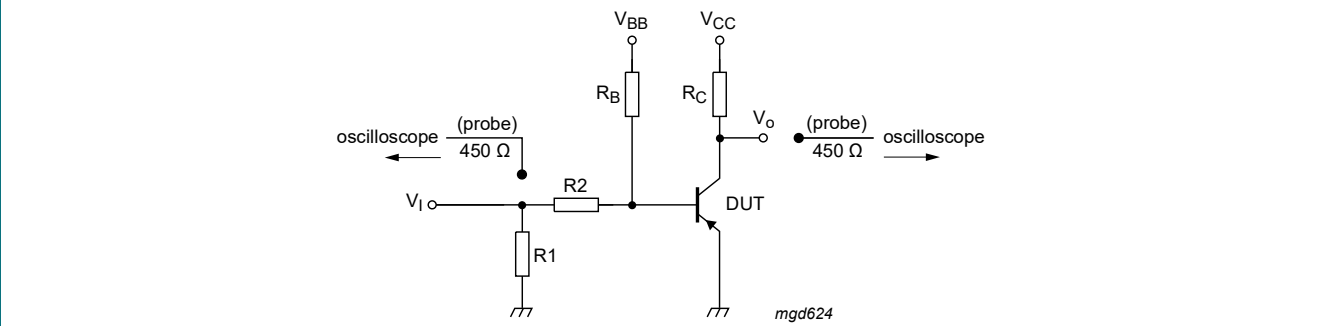


Fig. 24. TR2 (PNP): Test circuit for switching times

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

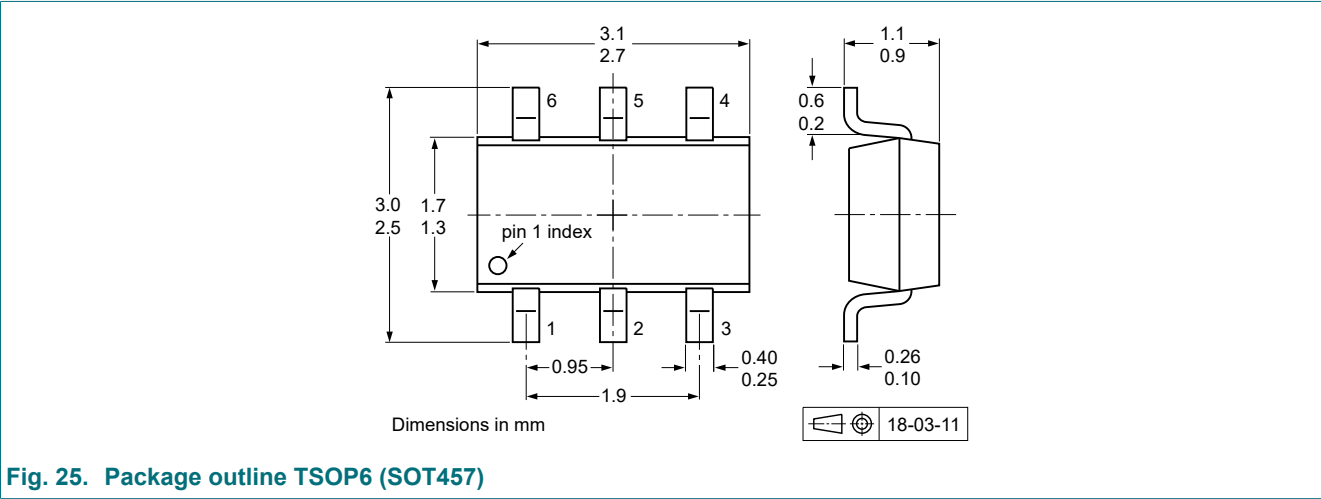
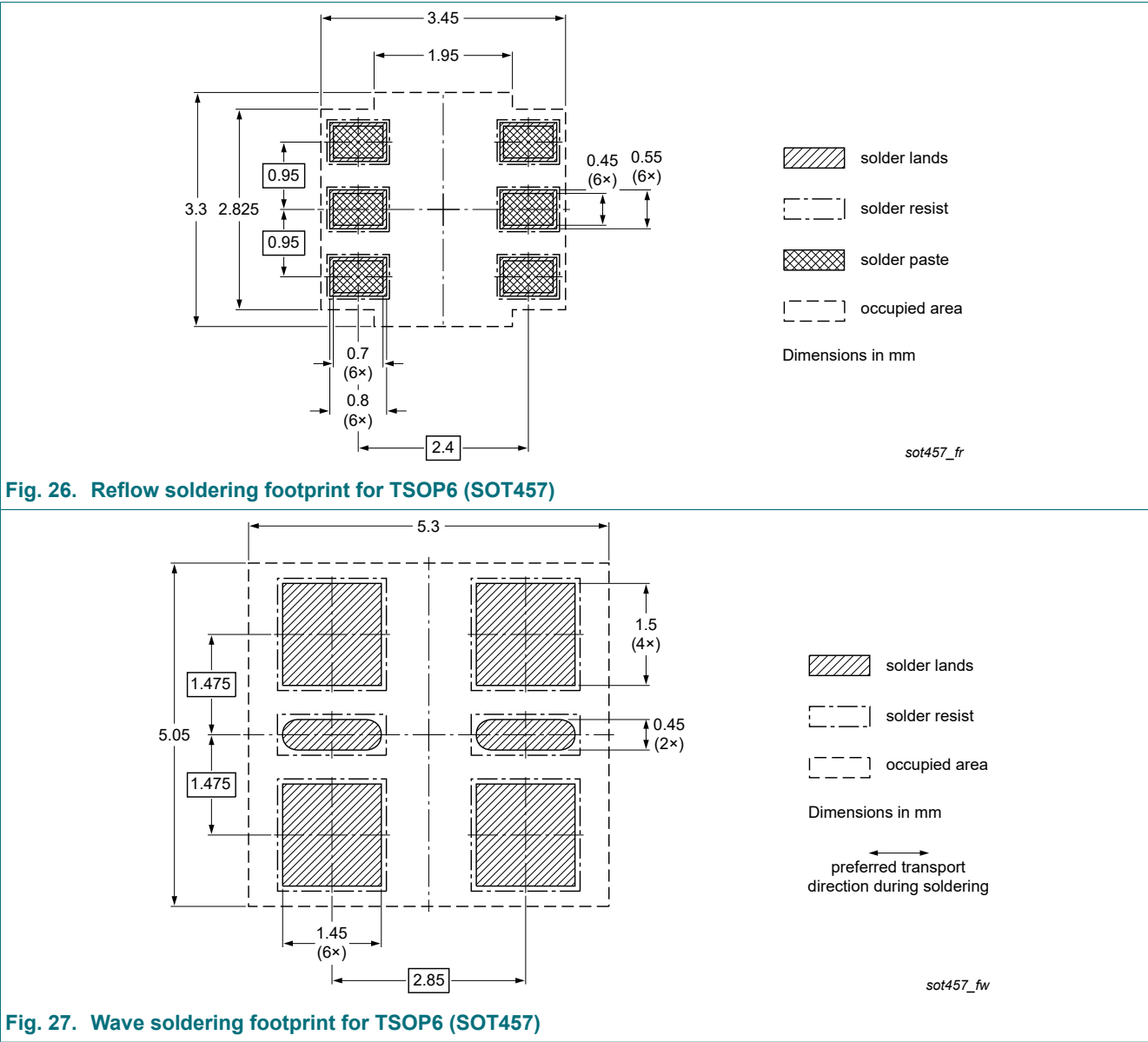


Fig. 25. Package outline TSOP6 (SOT457)

13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4160DPN v.4	YYYYMMDD	Product data sheet		PBSS4160DPN_3
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.Section "Packing information" removed.			
PBSS4160DPN_3	20091211	Product data sheet		PBSS4160DPN_2
PBSS4160DPN_2	20050714	Product data sheet	-	PBSS4160DPN_1
PBSS4160DPN_1	20040603	Objective data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com

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