NID5100

1.2 V to 5.5 V, 1.5 A input polarity protected, low quiescent current ideal diode

Rev. 1 — 26 July 2024 Product data sheet

1. General description

The NID5100 is an integrated ideal diode capable of replacing traditional diodes in low voltage systems unable to tolerate the high voltage drops of conventional Schottky components.

When enabled and forward biased, the device regulates the voltage between the IN and OUT pins resulting in a forward voltage drop, V_{REG}, approximately an order of magnitude smaller than similarly rated Schottky diodes. When OUT voltage is higher than IN voltage, the NID5100 becomes reverse biased with very low leakage current.

Integrated Reverse-Polarity Protection (RPP) prevents damage to components connected to the OUT pin in the event of a supply voltage reversal.

The enable pin, $\overline{EN}$ determines if NID5100 operates in forward regulation mode or body-diode mode.

A variety of power OR-ing configurations are supported for system flexibility:

- Two, or more, NID5100 devices in combination
- NID5100s and conventional Schottky diodes
- An NID5100 and an external PMOS

An open-drain status pin, ST, is high-impedance when NID5100 is enabled and in forward conduction and low when disabled or in a reverse biased condition. The ST pin can be used to control an external PMOS to OR an additional supply, or connected to a microcontroller to indicate the status condition of NID5100.

The NID5100 is available in a standard TSSOP6 (SOT363-2) with 2.1 mm x 1.25 mm x 0.95 mm body package compatible with industry SC88/SC70-6 packages providing a small PCB footprint compared to conventional low-current diodes.

2. Features and benefits

- Low loss replacement for power OR-ing diodes
- Automatic transition between OR-ed supplies
- Operating voltage range: 1.2 V to 5.5 V
- Reverse voltage protection V_{IN}: -6 V absolute maximum
- Supports forward current up to 1.5 A
- Forward regulation voltage, V_{REG} : 31 mV (typ) at I_{OUT} = 10 mA, V_{IN} = 3.3 V
- Active LOW control pin, $\overline{EN}$
- Output status indication, ST
- Low current consumption:
  - 3.3 V shutdown current, $I_{IN(SD)}$: 170 nA (typ)
  - 3.3 V quiescent current, $I_{IN(Q)}$: 240 nA (typ)
- Specified over T_{amb} -40 °C to +125 °C

3. Applications

- Building automation
- Smart meters
- OR-ed primary and battery backup

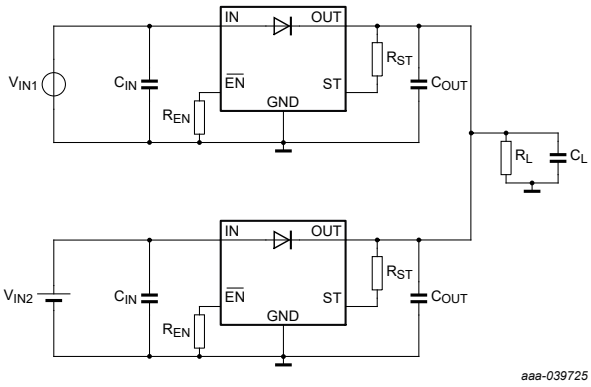


Fig. 1. Simplified application

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NID5100GW	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2

5. Marking

Table 2. Marking code

Type number	Marking code
NID5100GW	u1

6. Pin configuration and description

6.1. Pin configuration

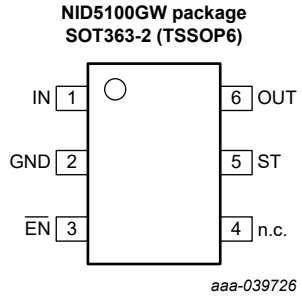


Fig. 2. Pin configuration SOT363-2 (SC-88)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	I/O	Description
IN	1	I	Device input. Analogous to the "anode" pin of a diode.
GND	2	-	Device ground.
$\overline{EN}$	3	I	Active-low enable input. Drive $\overline{EN}$ low to enable the device. Drive high to disable the device. Drive this pin to a valid high or low level. Do not leave this pin floating.
n.c.	4	-	Not internally connected. Can be tied to GND or left floating. Must be soldered to PCB pad for mechanical reliability.
ST	5	O	Active-low output. High-Z when chip is enabled and regulating IN to OUT voltage, V_{REG}. Pulled low when the chip is disabled, or reverse current blocking. Connect to GND or leave floating if not used.
OUT	6	O	Device output. Analogous to the "cathode" pin of a diode.

7. Specifications

7.1. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	supply voltage		- 6.0	+ 6.0	V
V_{OUT}	output voltage		- 0.3	+ 6.0	V
$V_{\overline{EN}}$	enable pin voltage		- 0.3	+ 6.0	V
V_{ST}	status pin voltage		- 0.3	+ 6.0	V
$I_{SW(MAX)}$	continuous switch current		-	+ 1.5	A
$I_{SW(PLS)}$	maximum pulsed switch current	≤120 ms, 2% Duty Cycle	-	+ 2.5	A
$I_{D(PLS)}$	maximum pulsed body diode current	≤0.1 ms, 0.2% Duty Cycle	-	+ 2.5	A
I_{ST}	status pin current		- 1.0	-	mA
T_j	junction temperature		- 40	150	ºC
T_{stg}	storage temperature		- 65	150	ºC
T_{lead}	lead temperature	(10 s soldering time)	-	300	ºC

7.2. ESD ratings

Table 5. ESD ratings

Symbol	Parameter	Conditions	Value	Unit
V_{ESD}	electrostatic discharge	HBM: ANSI/ESDA/JEDEC JS-001 class 2	±2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C2a	±500	V

7.3. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	supply voltage		1.2	5.5	V
V_{OUT}	output voltage	V_{IN} ≥ 1.2 V	0.5	5.5	V
V_{ST}	status pin voltage		0	5.5	V
$V_{\overline{EN}}$	enable pin voltage		0	5.5	V
Δt/ΔV	enable pin input transition rise and fall rate	V_{IN} = 1.2 to 5.5 V; $V_{\overline{EN}}$ = 0 to V_{IN} or V_{IN} to 0 V	0	200	ms/V

7.4. Recommended components

Table 7. Recommended components

Nominal component values, not including derating factors.

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
C_{IN}	capacitance on IN		0.1	1	-	µF
C_{OUT}	capacitance on OUT	An output capacitor is required for proper operation.	0.1	0.47	100	µF
$R_{\overline{EN}}$	resistor on $\overline{EN}$	Connected to GND [1]	0	50	100	kΩ
$R_{\overline{ST}}$	resistor on $\overline{ST}$		25	50	100	kΩ

[1] If the $\overline{EN}$ pin is driven by a microcontroller, the value of $R_{\overline{EN}}$ should be chosen in accordance with the microcontrollers I/O pin drive capability (V_{OH} and V_{OL}).

7.5. Thermal information

Table 8. Thermal information

Thermal resistance according to JEDEC51-5 and -7

Symbol	Parameter	*SOT363-2*	Unit
$R_{\Theta JA}$	junction-to-ambient thermal resistance	256	°C/W
$R_{\Theta JC(TOP)}$	junction-to-case (top) thermal resistance	177	°C/W
Ψ_{JT}	junction-to-top characterization parameter	78	°C/W

7.6. Electrical characteristics

Table 9. Static characteristics

C_{IN} = 0.1 µF in parallel with 1 µF, C_{OUT} = 0.1 µF, $V_{\overline{EN}}$ = 0 V, 1.5 V ≤ V_{IN} ≤ 5.5 V. Typical values are at T_{amb} = 25 °C with an input voltage of 3.3 V (unless otherwise noted).

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
Input supply (IN)								
$I_{IN(SD)}$	shutdown current	V_{OUT} = V_{IN} = $V_{\overline{EN}}$ = 3.3 V I_{OUT} = 0 A (V_{OUT} = open)		T_{amb} = 25°C	-	0.17	0.24	µA
				T_{amb} = -40°C to 125°C	-	-	0.30	
$I_{IN(Q)}$	quiescent current	V_{OUT} = V_{IN}; $V_{\overline{EN}}$ = 0 V I_{OUT} = 0 A (V_{OUT} = open)		T_{amb} = 25°C	-	0.24	0.35	µA
				T_{amb} = -40°C to 125°C	-	-	0.40	
Forward voltage regulation, V_{REG}								
V_{REG}	forward regulation voltage V_{REG} = V_{IN} - V_{OUT}	V_{IN} = 5 V, or V_{IN} = 3.3 V	$V_{\overline{EN}}$ = 0 V I_{OUT} = 10 mA	T_{amb} = -40°C to 125°C	7	31	50	mV
ON-resistance (R_{ON}). See Fig. 26.								
R_{ON}	on-state resistance	transistor fully enhanced	V_{IN} = 3.3 V I_{OUT} = - 500 mA $V_{\overline{EN}}$ = 0 V	T_{amb} = 25°C	-	115	-	mΩ
Reverse Current Blocking (RCB) and body diode characteristics								
V_{RCB_R}	reverse current blocking activation voltage	(V_{OUT} - V_{IN}), V_{OUT} rising above V_{IN} $V_{\overline{EN}}$ = 0 V		T_{amb} = 25°C	-	30.5	-	mV
V_{RCB_F}	reverse current blocking deactivation voltage	(V_{OUT} - V_{IN}), V_{OUT} falling below V_{IN} $V_{\overline{EN}}$ = 0 V		T_{amb} = 25°C	-	- 33.5	-	mV
V_{FWD}	body diode forward voltage	I_{OUT} = 10 mA $V_{\overline{EN}}$ = V_{IN}		T_{amb} = -40°C to 125°C	0.3	0.5	0.9	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Leakage currents							
$I_{OUT-IN(REV)}$	OUT to IN leakage current (current out of IN, reverse biased) device enabled	V_{IN} = 3.3 V; V_{OUT} = 4 V; $V_{\overline{EN}}$ = 0 V	T_{amb} = 25°C	-	130	180	nA
			T_{amb} = -40°C to 85°C	-200	-	200	nA
			T_{amb} = -40°C to 125°C	-220	-	220	nA
		V_{IN} = 3.3 V; V_{OUT} = 5 V; $V_{\overline{EN}}$ = 0 V	T_{amb} = 25°C	-	130	180	nA
			T_{amb} = -40°C to 85°C	-200	-	200	nA
			T_{amb} = -40°C to 125°C	-220	-	220	nA
		V_{IN} = 2 V; V_{OUT} = 5.5 V; $V_{\overline{EN}}$ = 0 V	T_{amb} = -40°C to 85°C	-220	130	220	nA
$I_{OUT(REV)}$	current into OUT (reverse biased) device enabled	V_{IN} = 3.3 V; V_{OUT} = 4 V; $V_{\overline{EN}}$ = 0 V	T_{amb} = 25°C	-	330	410	nA
			T_{amb} = -40°C to 85°C	-	-	500	nA
			T_{amb} = -40°C to 125°C	-	-	800	nA
		V_{IN} = 3.3 V; V_{OUT} = 5 V; $V_{\overline{EN}}$ = 0 V	T_{amb} = 25°C	-	420	500	nA
			T_{amb} = -40°C to 85°C	-	-	600	nA
			T_{amb} = -40°C to 125°C	-	-	1000	nA
		V_{IN} = 2 V; V_{OUT} = 5.5 V; $V_{\overline{EN}}$ = 0 V	T_{amb} = -40°C to 85°C	-	530	700	nA
$I_{OUT-IN(DIS)}$	OUT to IN leakage current (current out of IN, reverse biased) device disabled	V_{IN} = $V_{\overline{EN}}$ = 4.5 V; V_{OUT} = 5.5 V	T_{amb} = 25°C	-	150	500	nA
			T_{amb} = -40°C to 85°C	-	-	800	nA
			T_{amb} = -40°C to 125°C	-	-	825	nA
		V_{IN} = $V_{\overline{EN}}$ = 1.5 V; V_{OUT} = 5.5 V	T_{amb} = -40°C to 85°C	-	-	3300	nA
			T_{amb} = -40°C to 125°C	-	-	3500	nA
		V_{IN} = $V_{\overline{EN}}$ = 0 V; V_{OUT} = 5.5 V	T_{amb} = -40°C to 85°C	-	-	1500	nA
			T_{amb} = -40°C to 125°C	-	-	1650	nA
Enable ($\overline{EN}$)							
V_{IL}	LOW-level input voltage	device enabled	T_{amb} = -40°C to 125°C	-	-	0.4	V
V_{IH}	HIGH-level input voltage	device disabled	T_{amb} = -40°C to 125°C	1.2	-	-	V
V_{HYS}	enable pin hysteresis		T_{amb} = 25°C	-	45	-	mV
I_{IL}	LOW-level input current	$V_{\overline{EN}}$ = 0 V	T_{amb} = 25°C	-30	0	30	nA
			T_{amb} = -40°C to 125°C	-100	-	100	nA
I_{IH}	HIGH-level input current	V_{IN} = 3.3 V $V_{\overline{EN}}$ = 3.3 V	T_{amb} = 25°C	-	15	-	nA
			T_{amb} = -40°C to 125°C	-	-	150	nA
	HIGH-level input current ($V_{\overline{EN}}$ > V_{IN})	V_{IN} = 3.3 V $V_{\overline{EN}}$ = 5 V	T_{amb} = 25°C	-	20	-	nA
			T_{amb} = -40°C to 125°C	-	-	150	nA
Status indication (ST)							
$V_{OL(ST)}$	LOW-level output	I_{ST} = 1 mA; V_{IN} ≥ 1.8 V	T_{amb} = -40°C to 125°C	-	-	0.1	V
		I_{ST} = 0.1 mA; V_{IN} < 1.8 V	T_{amb} = -40°C to 125°C	-	-	0.1	V
I_{ST}	ST pin leakage current	V_{ST} = V_{IN} $V_{\overline{EN}}$ = 0 V	T_{amb} = -40°C to 125°C	-150	-	150	nA

7.7. Dynamic characteristics

Table 10. Dynamic characteristics

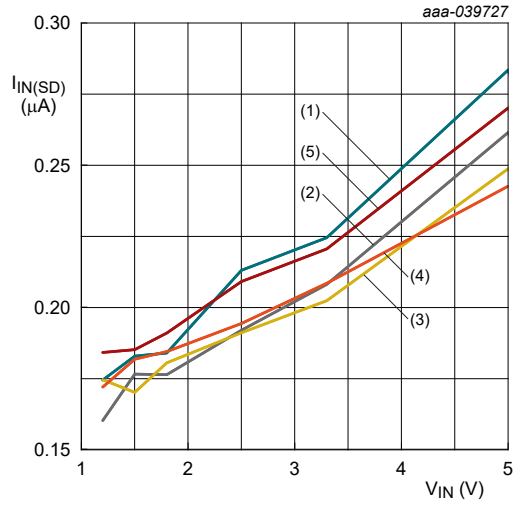
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); typical values at T_{amb} = 25 °C; C_{IN} = 0.1 µF in parallel with 1 µF; and a load of C_L = 100 nF in parallel with R_L = 1 kΩ. See Fig. 22 and Fig. 23.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ON}	turn-on time	V_{IN} = 1.5 V	-	90	-	µs
		V_{IN} = 1.8 V	-	100	-	µs
		V_{IN} = 2.5 V	-	130	-	µs
		V_{IN} = 3.3 V	-	165	-	µs
		V_{IN} = 5 V	-	240	-	µs
t_{OFF}	turn-off time	V_{IN} = 1.5 V	-	60	-	µs
		V_{IN} = 1.8 V	-	50	-	µs
		V_{IN} = 2.5 V	-	38	-	µs
		V_{IN} = 3.3 V	-	30	-	µs
		V_{IN} = 5 V	-	10	-	µs
t_{FALL}	output FALL time	V_{IN} = 1.5 V	-	35	-	µs
		V_{IN} = 1.8 V	-	25	-	µs
		V_{IN} = 2.5 V	-	20	-	µs
		V_{IN} = 3.3 V	-	15	-	µs
		V_{IN} = 5 V	-	10	-	µs
t_{STLZ}	status, ST pin, delay time: low to high-impedance $\overline{EN}$ transitions from high to low R_{ST} = 50 kΩ to IN	V_{IN} = 1.5 V	-	80	-	µs
		V_{IN} = 1.8 V	-	90	-	µs
		V_{IN} = 2.5 V	-	125	-	µs
		V_{IN} = 3.3 V	-	160	-	µs
		V_{IN} = 5 V	-	220	-	µs
t_{STZL}	status, ST pin, delay time: high-impedance to low $\overline{EN}$ transitions from low to high R_{ST} = 50 kΩ to IN	V_{IN} = 1.5 V	-	38	-	µs
		V_{IN} = 1.8 V	-	33	-	µs
		V_{IN} = 2.5 V	-	25	-	µs
		V_{IN} = 3.3 V	-	18	-	µs
		V_{IN} = 5 V	-	1	-	µs

7.8. Typical Characteristics

V_{IN} = 3.3 V, GND = 0 V, $V_{\overline{EN}}$ = 0 V, C_{IN} = 0.1 + 1 µF, C_{OUT} + C_L = 0.1 + 1 µF to GND. Typical values at T_{amb} = 25 C, unless otherwise noted.

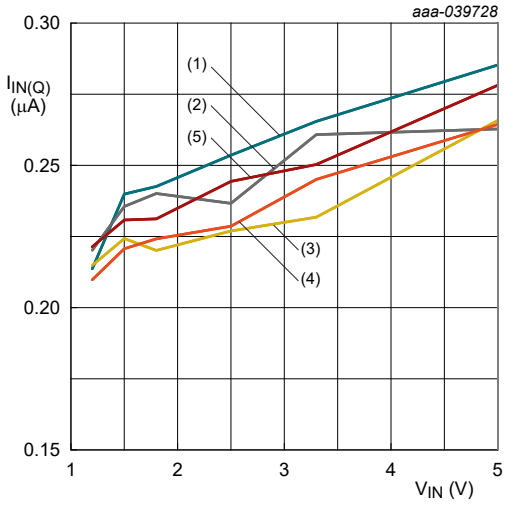
Table 11. Typical Characteristics



$V_{\overline{EN}}$ = V_{IN}

-40 °C	25 °C	85 °C	105 °C	125 °C
(1)	(2)	(3)	(4)	(5)

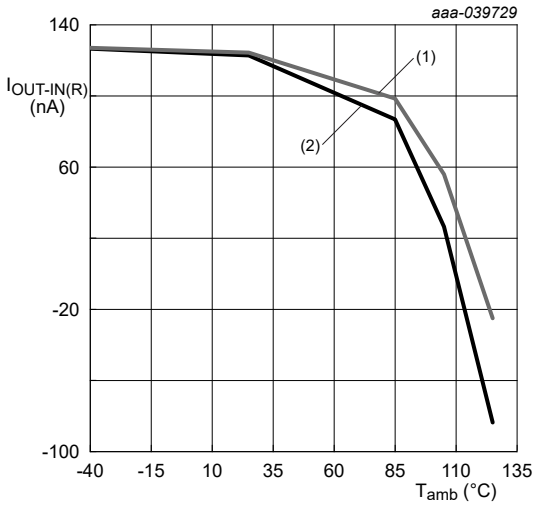
Fig. 3. Shutdown current versus input voltage



$V_{\overline{EN}}$ = 0 V

-40 °C	25 °C	85 °C	105 °C	125 °C
(1)	(2)	(3)	(4)	(5)

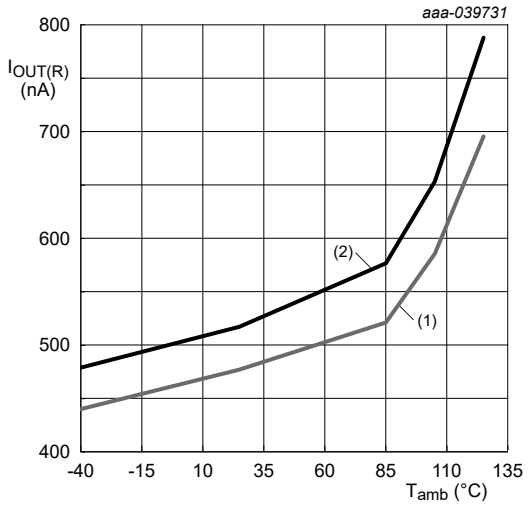
Fig. 4. Quiescent supply current versus input voltage



$V_{\overline{EN}}$ = 0 V

V_{OUT} = 5 V; V_{IN} = 3.3 V	V_{OUT} = 5.5 V; V_{IN} = 2 V
(1)	(2)

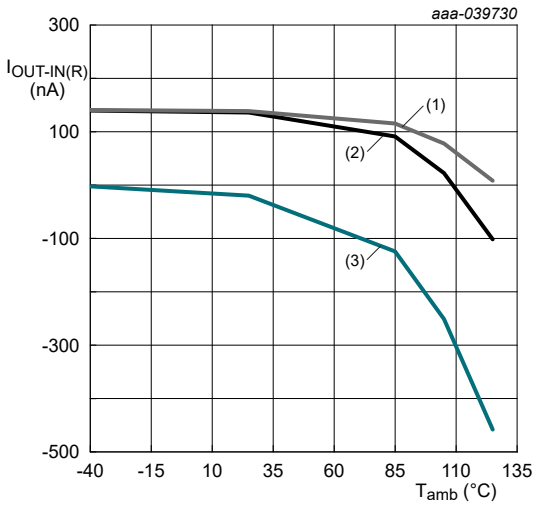
Fig. 5. OUT to IN leakage current (enabled, blocking) versus junction temperature



$V_{\overline{EN}}$ = 0 V

V_{OUT} = 5 V; V_{IN} = 3.3 V	V_{OUT} = 5.5 V; V_{IN} = 2 V
(1)	(2)

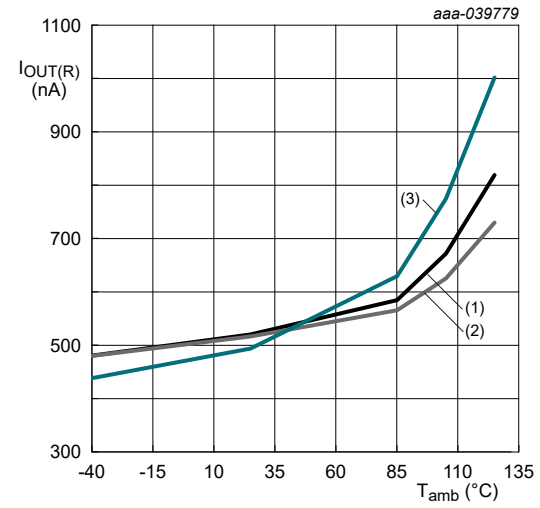
Fig. 6. OUT current (enabled, blocking) versus junction temperature



$V_{\overline{EN}} = V_{IN}$

V_{OUT} = 5 V; V_{IN} = 4.5 V	V_{OUT} = 5.5 V; V_{IN} = 1.5 V	V_{OUT} = 5.5 V; V_{IN} = 0 V
(1)	(2)	(3)

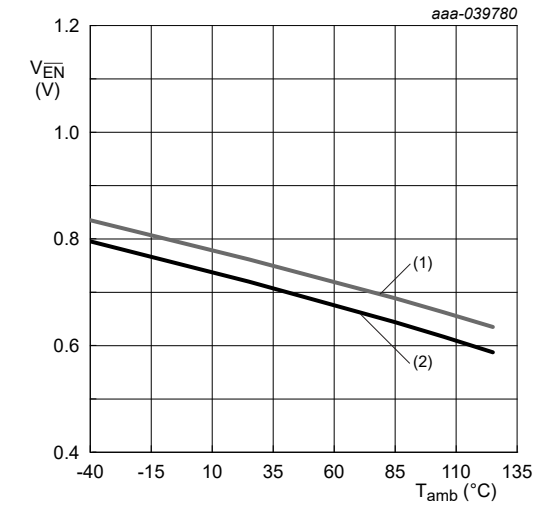
Fig. 7. OUT to IN leakage current (disabled, blocking) versus junction temperature



$V_{\overline{EN}} = V_{IN}$

V_{OUT} = 5 V; V_{IN} = 4.5 V	V_{OUT} = 5.5 V; V_{IN} = 1.5 V	V_{OUT} = 5.5 V; V_{IN} = 0 V
(1)	(2)	(3)

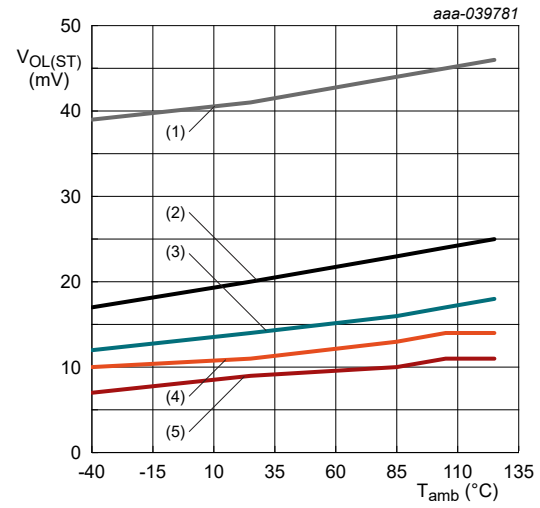
Fig. 8. OUT current (disabled, blocking) versus junction temperature



V_{IN} = 1.2 to 5 V

$V_{\overline{EN}}$ rising	$V_{\overline{EN}}$ falling
(1)	(2)

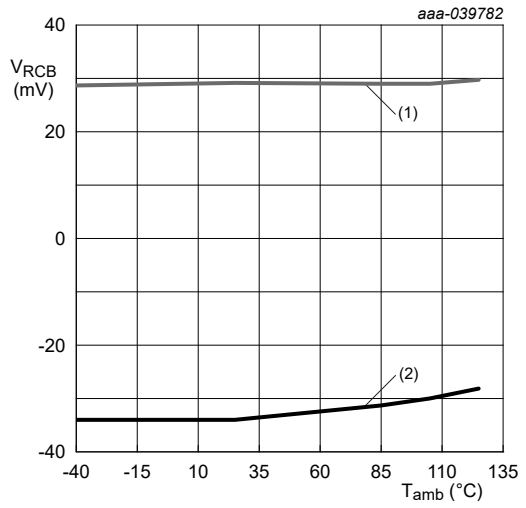
Fig. 9. Enable threshold voltage versus temperature



$V_{\overline{EN}} = V_{IN}$

$I_{OL(ST)}$ = 0.1 mA	$I_{OL(ST)}$ = 1 mA			
1.2 V	1.8 V	2.5 V	3.3 V	5 V
(1)	(2)	(3)	(4)	(5)

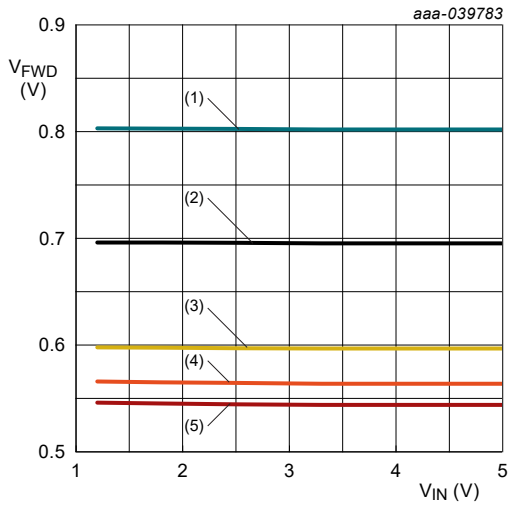
Fig. 10. Status pin output low level voltage



V_{IN} = $V_{\overline{EN}}$ = 1.2 to 5 V; V_{OUT} - V_{IN}

V_{RCB_R} (enable)	V_{RCB_F} (disable)
(1)	(2)

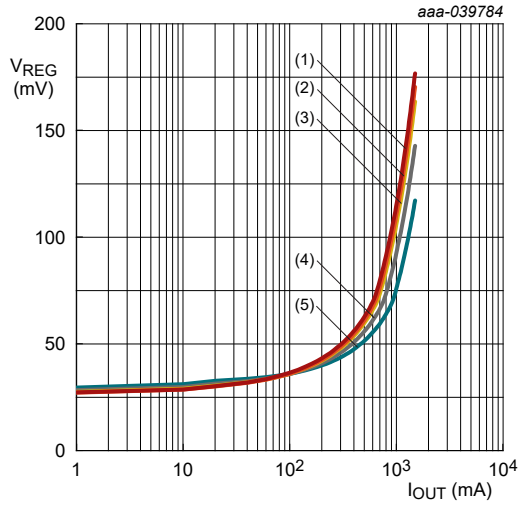
Fig. 11. Reverse current blocking threshold voltage versus temperature



$V_{\overline{EN}}$ = V_{IN}

-40 °C	25 °C	85 °C	105 °C	125 °C
(1)	(2)	(3)	(4)	(5)

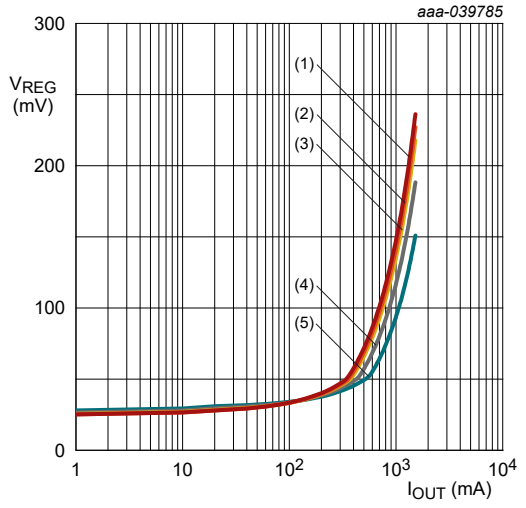
Fig. 12. Body diode forward voltage versus input voltage



V_{IN} = 5 V; $V_{\overline{EN}}$ = 0 V; C_L = 100 nF

-40 °C	25 °C	85 °C	105 °C	125 °C
(1)	(2)	(3)	(4)	(5)

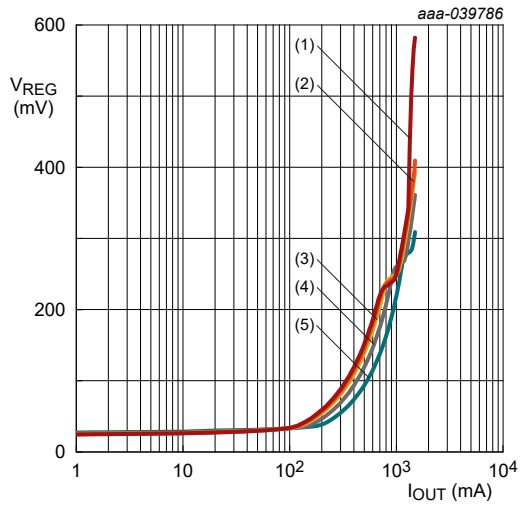
Fig. 13. Forward regulation voltage vs output current



V_{IN} = 3.3 V; $V_{\overline{EN}}$ = 0 V; C_L = 100 nF

-40 °C	25 °C	85 °C	105 °C	125 °C
(1)	(2)	(3)	(4)	(5)

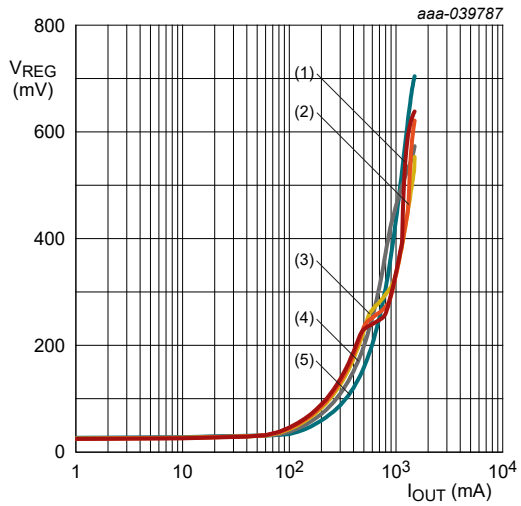
Fig. 14. Forward regulation voltage vs output current



V_{IN} = 1.8 V; V_{EN} = 0 V; C_L = 100 nF

-40 °C	25 °C	85 °C	105 °C	125 °C
(1)	(2)	(3)	(4)	(5)

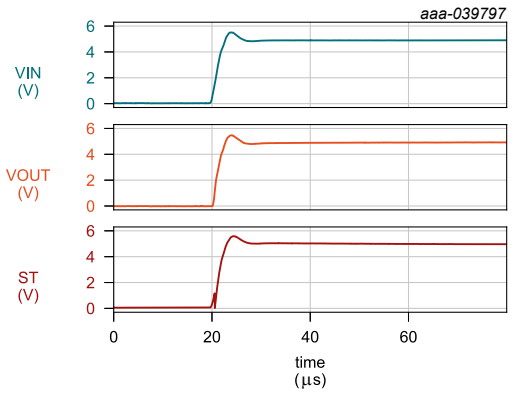
Fig. 15. Forward regulation voltage vs output current



V_{IN} = 1.5 V; $V_{\overline{EN}}$ = 0 V; C_L = 100 nF

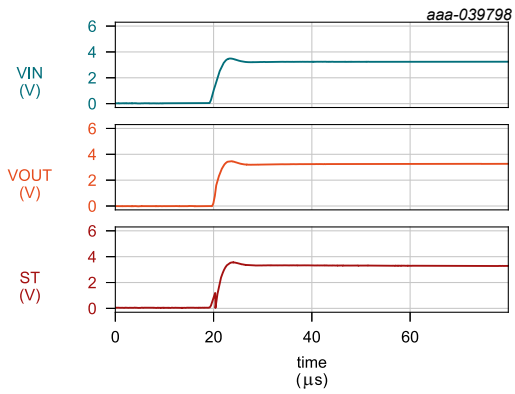
-40 °C	25 °C	85 °C	105 °C	125 °C
(1)	(2)	(3)	(4)	(5)

Fig. 16. Forward regulation voltage vs output current



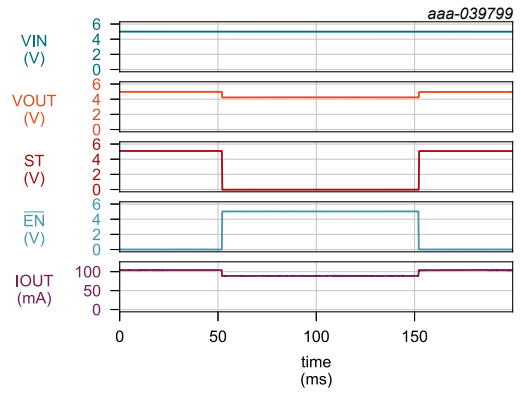
V_{IN} = 5 V; V_{EN} = 0 V; C_L = 100 nF; R_L = 1 kΩ

Fig. 17. Power up response



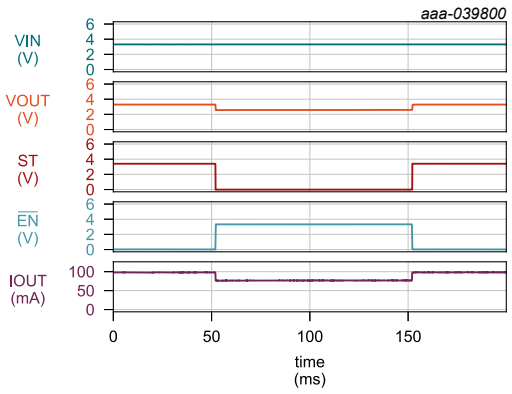
V_{IN} = 3.3 V; V_{EN} = 0 V; C_L = 100 nF; R_L = 1 kΩ

Fig. 18. Power up response



V_{IN} = 5 V; $V_{\overline{EN}}$ = 0 to V_{IN}; C_L = 100 nF; R_L = 47 Ω

Fig. 19. Enable and disable response



V_{IN} = 3.3 V; $V_{\overline{EN}}$ = 0 to V_{IN}; C_L = 100 nF; R_L = 33 Ω

Fig. 20. Enable and disable response

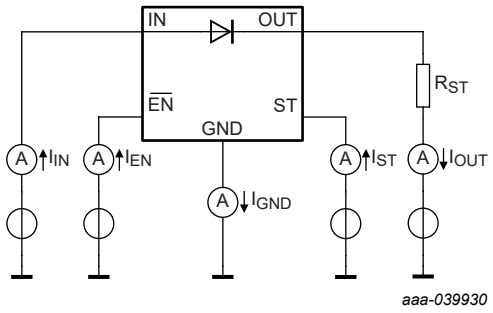


Fig. 21. Current measurement test circuit

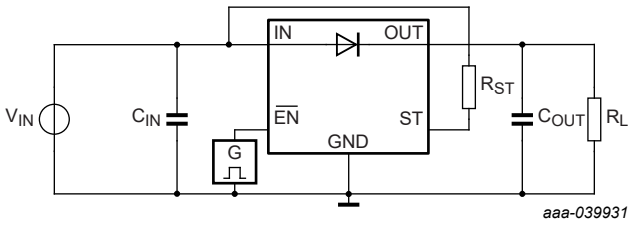


Fig. 22. Timing response measurement circuit

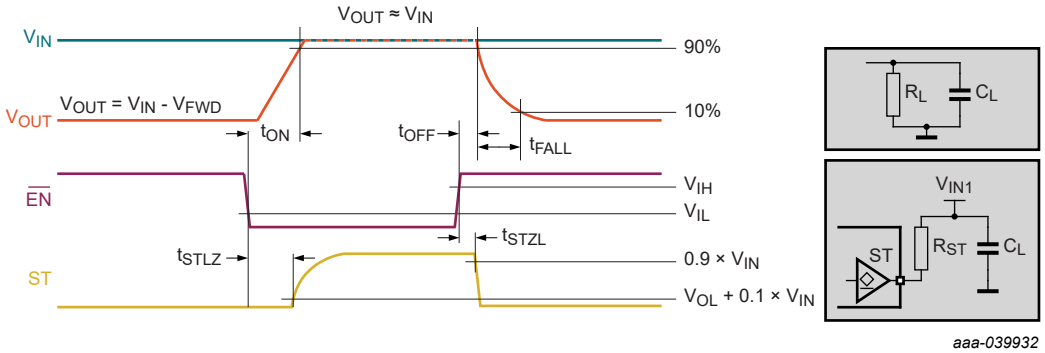


Fig. 23. Timing diagram

8. Functional Description

8.1. Functional diagram

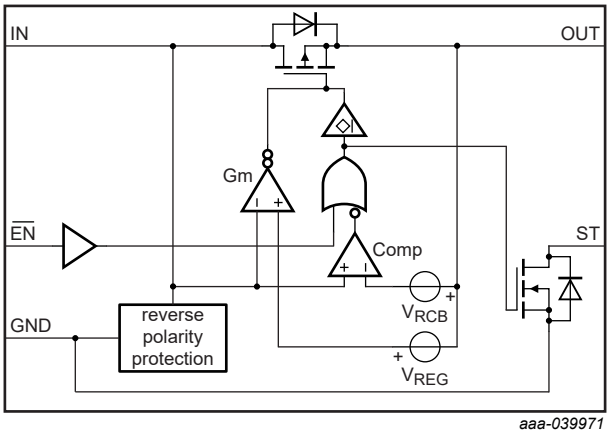


Fig. 24. Functional diagram

8.2. Overview

The NID5100 consists of an internal PMOS transistor with its body diode oriented from IN (anode) to OUT (cathode); reverse current protection; reverse polarity protection; gate regulation amplifier; control logic and a status flag, ST. The device conducts from IN to OUT when enabled and forward biased and blocks when reverse biased. It mimics the behavior of low voltage Schottky diodes with a fraction of the forward voltage drop and significantly lower reverse leakage current. It is designed to operate from a 1.2 to 5.5 V supply making it suitable for use in a variety of low voltage applications.

OR-ing: The NID5100 supports a variety of power supply OR-ing, or redundant power backup, scenarios:

1. Low loss using "2 to n" NID5100s
2. Low loss dual OR-ing circuit consisting of one NID5100 and an external PMOS
3. Hybrid with one, or more, NID5100(s) in combination with Schottky diodes
4. Paralleling two or more NID5100s for high current loads

See application information sections for suggested implementations.

8.3. Feature Description

8.3.1. Enable, control logic and ST pin

The enable pin, $\overline{EN}$, determines if the NID5100 operates in regulated conduction mode, $V_{\overline{EN}} \leq V_{IL}$, or body diode mode, $V_{\overline{EN}} \geq V_{IH}$.

When the $\overline{EN}$ pin voltage, $V_{\overline{EN}} \leq V_{IL}$, the gate amplifier and control logic are operational and the device consumes low quiescent current, $I_{Q(EN)}$.

The open-drain status, ST, pin provides real-time indication of the internal PMOS. See functional modes. When NID5100 is enabled, the ST pin indicates high when the internal PMOS is conducting. It indicates low when reverse biased and blocking. The ST pin is low when NID5100 is disabled. ST can be connected to a MCU input to provide status information or control an external PMOS in a low-loss dual OR-ing application. If the ST pin is unused, connect to ground.

8.3.2. Device functional modes

Table 12 summarizes the device operating modes.

Table 12. Device functional modes

$\overline{EN}$	State	IN-to-OUT	Power Dissipation	Status PIN State
HIGH	OFF	Diode	$I_{OUT} \times V_{FWD}$	L
LOW	ON	Forward conduction	$I_{OUT} \times (V_{IN} - V_{OUT})$	high-Z
LOW	RCB	Diode	$I_{OUT(REV)} \times V_{OUT}$ [1]	L

[1] OUT current is leakage into device when reverse biased. See electrical characteristics tables.

8.3.3. Reverse Polarity Protection (RPP)

Reverse polarity conditions can occur when a power source's terminals are connected with opposite polarity, or a battery is inserted incorrectly. Lossy power diodes and complicated ground connected discrete PMOS transistor circuits have historically been used to protect sensitive downstream circuits from polarity reversal conditions.

The NID5100 operates similarly. If a negative input voltage is applied to an unpowered NID5100, the PMOS will remain off and prevent reverse current flow protecting downstream components. If the NID5100 is initially powered on and subsequently experiences an input polarity reversal, the internal PMOS will turn off preventing the load from negative voltage. RPP is active regardless of the state of the $\overline{EN}$ pin.

For autonomous operation with RPP, the $\overline{EN}$ pin must be tied to GND. A pull-down resistor, R_{EN}, is optional, but recommended. If the ST pin is used for monitoring, it should be connected via a resistor, R_{ST}, to OUT or another voltage source immune to reverse polarity conditions. R_{ST} should be sized to prevent exceeding the ST pin leakage current (see I_{ST}). Fig. 25 provides an application example.

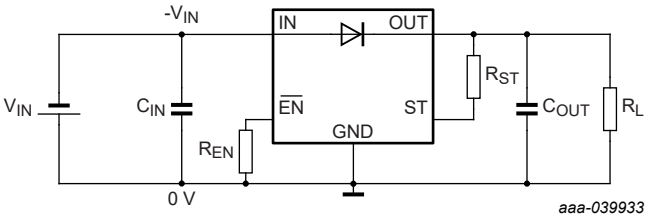


Fig. 25. Single supply reverse polarity protection circuit

8.3.4. Gate regulation amplifier

When the NID5100 is enabled and forward biased, the gate regulation amplifier adjusts the internal PMOS gate voltage to maintain the IN to OUT voltage, V_{REG}. When operating in the forward voltage regulation region, the voltage drop is approximately ten times smaller than a conventional Schottky diode aiding in the reduction of system power losses. At light loads, the forward voltage drop from IN to OUT is maintained at V_{REG}. As load current increases, the PMOS eventually becomes fully enhanced and the IN to OUT voltage drop becomes proportional to the on-resistance of the PMOS multiplied by the load current. See right side inset of Fig. 26.

8.3.5. Reverse Current Blocking (RCB)

Reverse current blocking (RCB) protection is always active, regardless of the state of $\overline{EN}$.

When $\overline{EN}$ is low and the output, OUT, is forced above the input, IN, the internal PMOS will switch off to stop the reverse current. When the IN to OUT differential returns below V_{RCB_F}, the device will turn back on and regulate IN to OUT at V_{REG}.

When $\overline{EN}$ pin voltage is high, the internal PMOS is turned off and reverse current blocking (RCB) occurs through body diode action when V_{OUT} is greater than V_{IN} + V_{FWD}. Forward conduction through the PMOS body diode resumes when V_{IN} + V_{FWD} is greater than V_{OUT}.

The NID5100 blocks reverse current via two mechanisms when enabled:

1. The V_{REG} amplifier responds to common transients by naturally increasing the PMOS transistor resistance as the IN to OUT voltage differential decreases. When V_{OUT} nears and becomes larger than V_{IN} the amplifier is regulating the transistor gate and R_{DSON} well below full enhancement increasing the impedance from OUT to IN until the PMOS becomes full disabled.
2. In the event of an extremely fast transition to a reverse biased condition, such as a shorted input, the fast trip RCB comparator reacts disabling the PMOS when V_{OUT} - V_{IN} = V_{RCB_R} to limit reverse current.

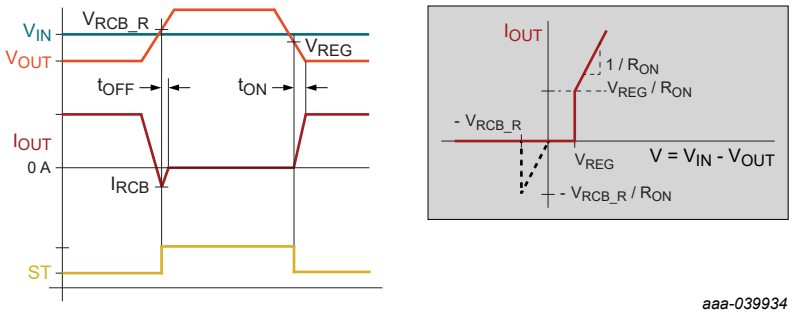


Fig. 26. Reverse current blocking overview

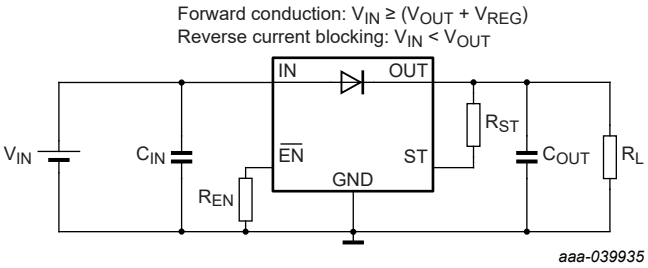


Fig. 27. Reverse current blocking

9. Application information

Note: Application implementation information in the following sections is not part of the Nexperia component specification. Nexperia's device users are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

The NID5100 ideal diode is a versatile device suitable for protecting circuits from reverse polarity connections, reverse current conditions, OR-ing and simple power multiplexing. The following sections provide application examples to aid the design of products using NID5100.

9.1. Reverse polarity protection

Universal DC power supplies are often used to replace an OEM wall charger which has been lost or broken. Commonly these supplies are capable of reversing voltage polarity and if the user does not take care to ensure proper universal power supply polarity setup, negative voltages could be applied to the device being powered causing it to be damaged. The NID5100 senses reverse polarity connections and protects downstream components from exposure to negative voltages.

When reverse polarity protection is used, the ST pin should be connected to OUT or left floating. Connecting ST to IN may result in device malfunction during supply reversal.

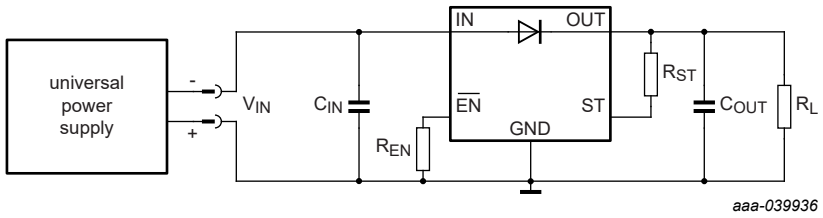


Fig. 28. Single supply reverse polarity protection scenario

Fig. 29 demonstrates the operation of NID5100 in the event of a positive to negative polarity reversal. V_{IN} is initially 5 V, then rapidly reverses to -5 V. V_{OUT} drops to 0 V and the ST pin transitions from high to low.

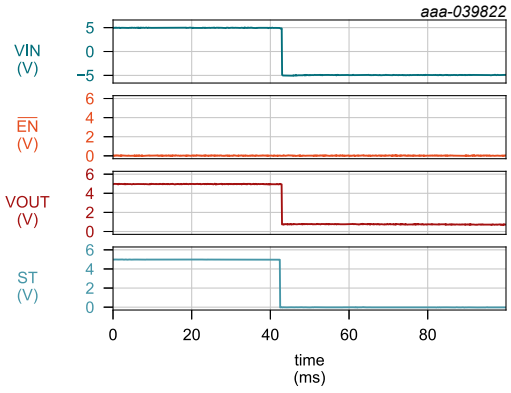


Fig. 29. 5 V to -5 V reverse polarity transition

Reverse polarity conditions can also occur in dual supply scenarios. Fig. 30 illustrates a situation in which a wall supply is providing power with an incorrectly installed backup battery. So long as the OUT to IN conditions in limiting values are be observed, the NID5100 can be use as shown without additional protection. For applications requiring a higher OUT to IN differential, an external PMOS can be added in the power path, or paths, where reversal may occur - see Fig. 31 .

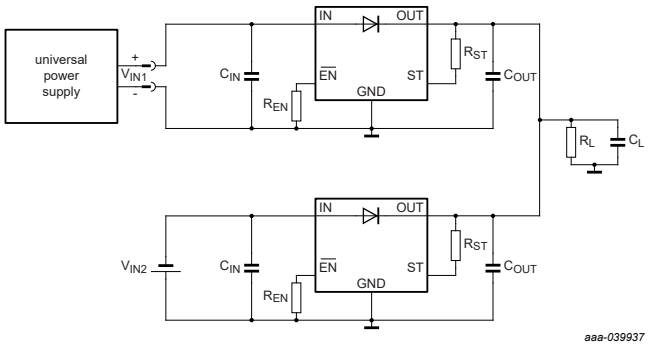


Fig. 30. Dual supply reverse polarity protection scenario: $|V_{IN1}| \leq 3$ V and $|V_{IN2}| \leq 3$ V

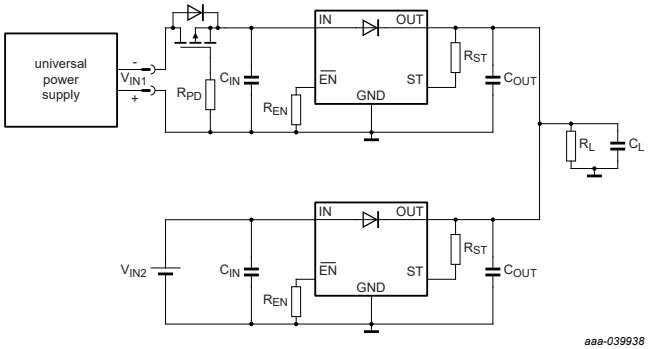


Fig. 31. Dual supply reverse polarity protection with PMOS: $|V_{IN1}| \leq 5$ V and $|V_{IN2}| \leq 3$ V

9.2. OR-ing examples

9.2.1. n+1 OR-ing using ideal diodes

There is no specific limitation to the number of NID5100 ideal diodes used for power OR-ing. The example below illustrates a common two power supply scenario with smooth transitions between supplies.

Some devices operate from a fixed power supply such as a standard 5 V USB port output in normal conditions but must quickly transition to a 3 V battery backup when the power supply is disabled or unplugged. Using two NID5100 devices in a power OR-ing configuration, the downstream load remains uninterrupted when either the DC supply or the backup battery are disconnected.

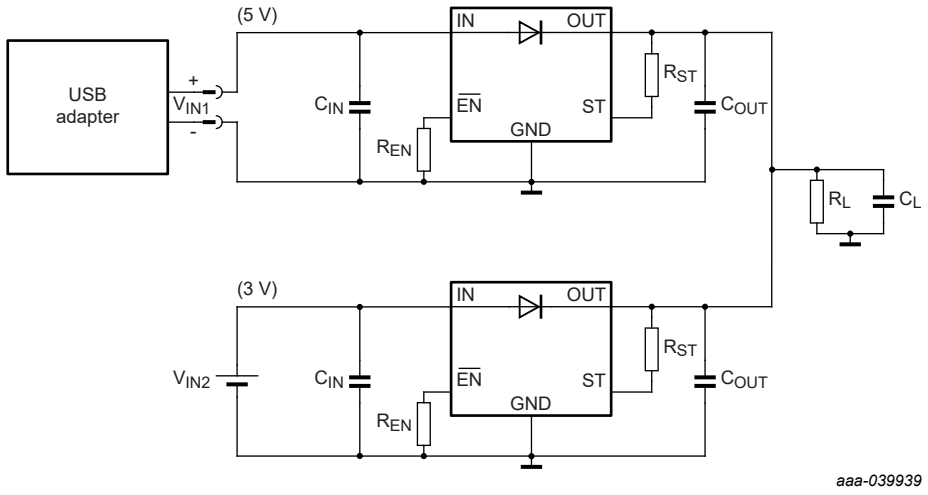


Fig. 32. OR-ing power supply and battery

The scope capture shows the output voltage (V_{OUT}) being initially powered by V_{IN1} at 5 V. When V_{IN1} is removed, V_{IN2} at 3.3 V powers V_{OUT}. When V_{IN1} is reconnected, V_{OUT} is once again powered by V_{IN1}. The ST pins of the NID5100's transition to indicate which ideal diode is supplying the load.

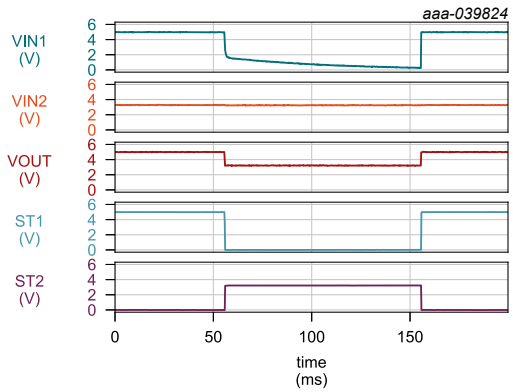


Fig. 33. OR-ed output transitions

9.2.2. OR-ing similar supply voltages

Some applications may require the OR-ing of supplies with similar voltages. Refer to Fig. 34 and Fig. 35. In this example, the primary DC supply is 3.3 V with a 3 V battery backup. Consider the scenario where V_{IN1} is suppling the load, is removed and subsequently restored.

Schottky circuit: As the two supplies differ by only 300mV, when V_{IN1} is restored, there may not be enough forward voltage, V_F, across the diode in the V_{IN1} path to forward bias it until the battery voltage depletes sufficiently wasting energy in the backup source.

NID5100 circuit: When V_{IN1} is restored, the reverse current blocking deactivation threshold, V_{RCB_F}, of the 3.3 V supplied NID5100 is easily exceeded allowing the 3.3 V supply to carry the full load. As the OUT is approximately 300 mV above V_{IN2}, the 3 V supplied NID5100 becomes reverse biased and the battery drain is minimized.

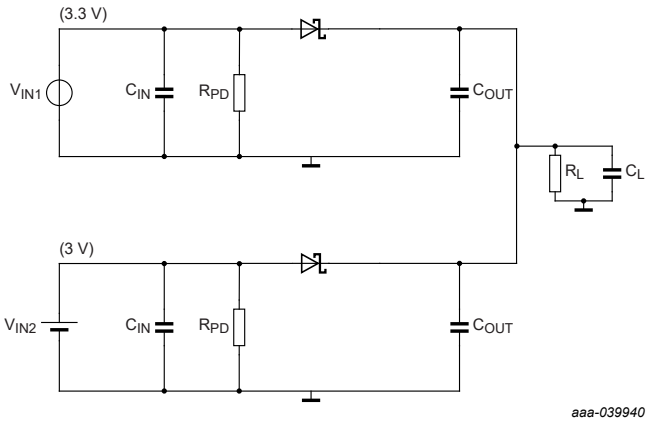


Fig. 34. OR-ing supplies of similar voltages: Schottky

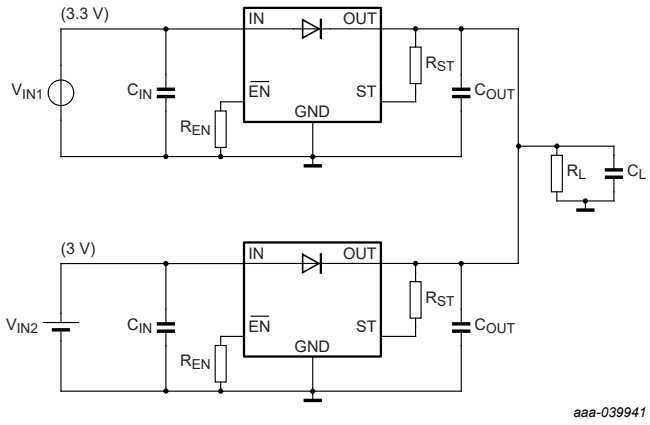
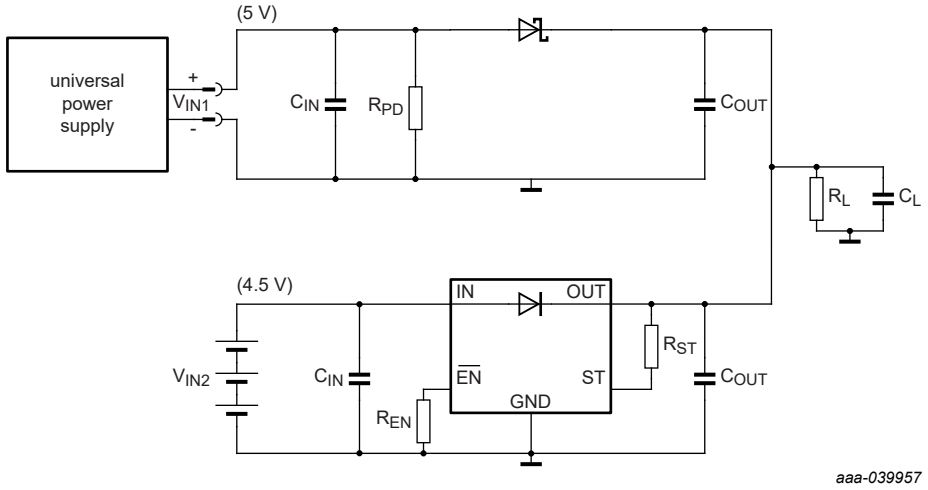


Fig. 35. OR-ing supplies of similar voltages: NID5100

9.2.3. n+1 OR-ing using ideal and conventional diodes

When voltage drops and electrical losses of one of two power sources is not of concern, a combination of ideal diodes and conventional diodes can be implemented as shown in Fig. 36. In this example the AC-DC adapter is the primary power source supplying 5 V to the system with three alkaline cells providing a 4.5 V backup. As stated in the OR-ing similar supply voltages section, consideration should be given to the V_F rating of the Schottky diode as well as worst case tolerances of the supply voltages to ensure seamless transitions.

A resistor, R_{PD}, connected to ground in the Schottky diode path is recommended to prevent diode reverse leakage during blocking conditions from charging C_{IN1} and raising V_{IN1}.



R_L = 47 Ω

Fig. 36. OR-ing with a combination of ideal and Schottky diodes

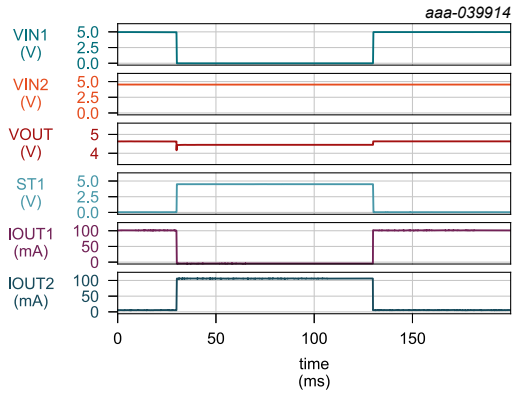


Fig. 37. OR-ing NID5100 with Schottky (PMEG4010) output transitions

9.2.4. Paralleling NID5100 for thermal and sustained high current considerations

As with using any power semiconductor component, thermal ratings must be observed to maintain device reliability. Refer to the thermal information table. System thermal analysis should be performed to ensure the device junction temperature, T_j, remains below 150 °C under all operating conditions. If analyses of using a single NID5100 indicate a thermal violation, two NID5100 can be paralleled to share the load current and lower internal power dissipation Fig. 38.

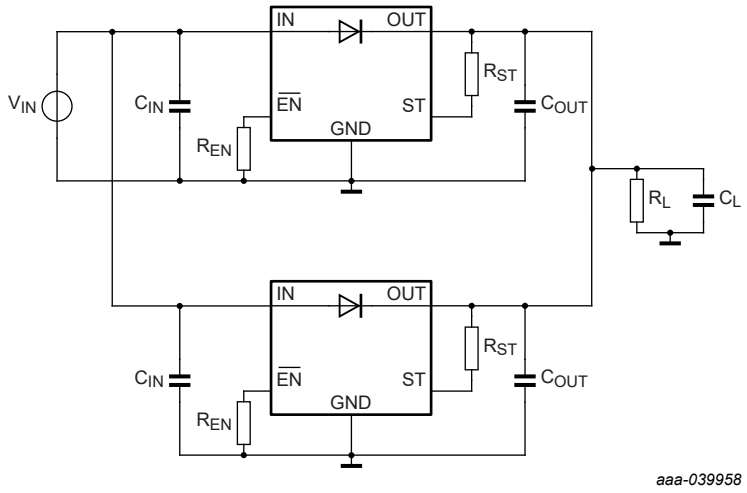


Fig. 38. Paralleling two NID5100 ideal diodes for high current

Fig. 39 shows two NID5100's supporting a combined 2 A load current with 1 A current flowing in each NID5100.

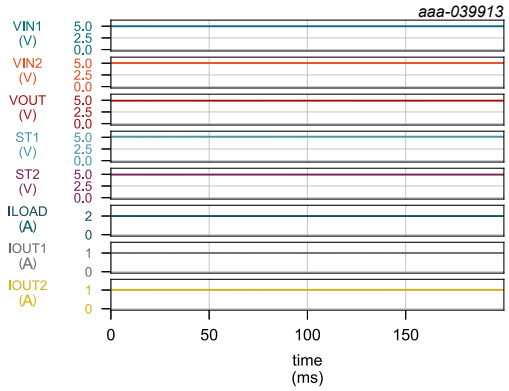


Fig. 39. Load sharing using two NID5100 ideal diodes

9.2.5. Priority OR-ing

More sophisticated systems may contain a microcontroller able to perform basic power management housekeeping functions such as power source selection from supplies with similar voltages. In the example of figure Fig. 40, two NID5100 ideal diodes are connected in an OR-ing configuration from similar 5 V sources.

Refer to the device functional modes table for operation of the ST pin. In this application example, the ST pin of NID5100 U1 is connected via a pull-up resistor to V_{IN1} and the $\overline{EN}$ of NID5100 U2 providing a polarity inversion of the GPIO signal. When device U1 is enabled, device U2 is disabled, and vice-versa allowing the MCU to select which supply sources the load.

When the microcontroller drives the GPIO low, NID5100 U1 is enabled sourcing V_{IN1} to OUT while U2 is disabled. Conversely if the GPIO is driven high, NID5100 U2 is enabled sourcing V_{IN2} to OUT and NID5100 U1 is disabled. In either scenario the RCB circuity remains active disabling the device with a low $\overline{EN}$ if V_{RCB_R} is exceeded.

R_{EN} is recommended to be of high enough resistance to prevent loading the MCU GPIO output while ensuring $\overline{EN}$ is actively driven in the event the GPIO is in a high impedance condition.

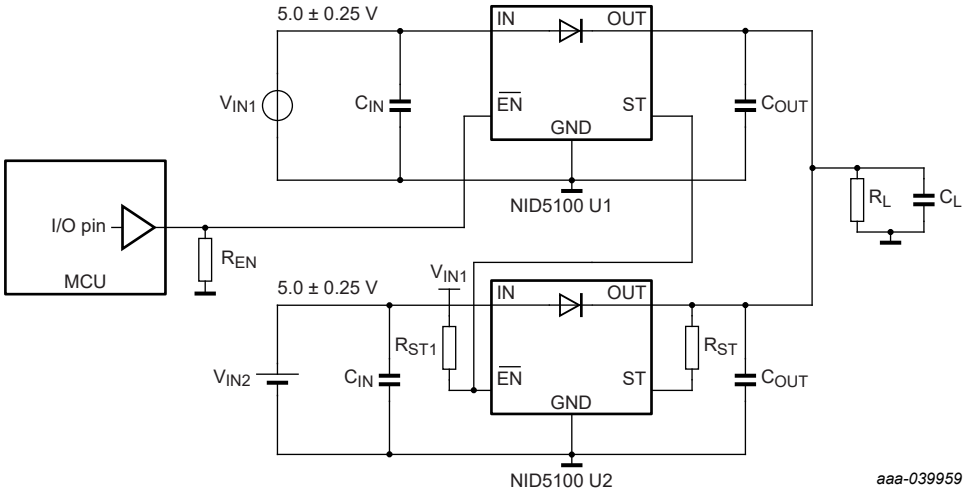
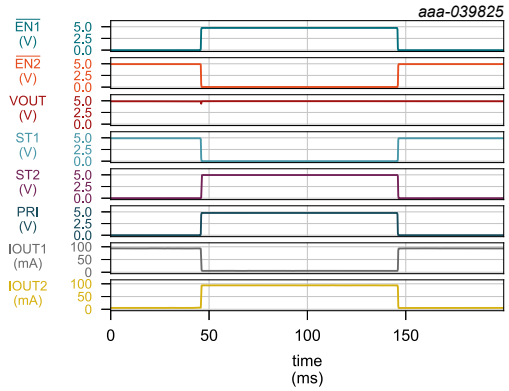


Fig. 40. Priority OR-ing using microcontroller

The scope capture shows $\overline{EN1}$, $\overline{EN2}$, V_{OUT}, ST1, ST2, GPIO priority signal (PRI) connected to $\overline{EN1}$, and the OUT1 and OUT2 currents.

Initially PRI is driven low pulling $\overline{EN1}$ low, enabling NID5100 U1. V_{OUT} is approximately equal to V_{IN1}. Load is supplied from OUT1. ST1, connected to $\overline{EN2}$ is pulled above the V_{IH} of NID5100 U2 with ST2 low indicating the device is disabled.

Next, $\overline{EN1}$ is driven high, disabling NID5100 U1 causing ST1 to transition low, enabling NID5100 U2.



R_L = 47 Ω

Fig. 41. Priority OR-ing output transitions

9.2.6. OR-ing with discrete MOSFET

In this application, the $\overline{EN}$ pin of the NID5100 is always grounded "enabling" the device. When both the 5 V and 3.3 V supplies are present, OUT is initially 5 V and the ST pin is high-Z with the R_{ST} resistor pulled up to V_{IN1}, keeping the gate of the external PFET high.

- If V_{IN1} is quickly removed, the ST pin output will transition low, enhancing the external PMOS. The load is then supplied from V_{IN2}.
- If V_{IN1} is a slowly discharging battery, OUT will transition from being supplied by the NID5100 OUT pin to being supplied by the external PMOS when V_{IN1} decreases below V_{IN2} by $V_{FWD(ext\_PMOS)}$. Conversely, if V_{IN1} is slowly recharged, OUT will be supplied from the PMOS until $V_{IN1} + V_{REG} \geq V_{IN2} + V_{RDSON(ext\_PMOS)}$

  Note: The supply to the NID5100 (V_{IN1}) should be the higher of the two supplies when both V_{IN1} and V_{IN2} are present.

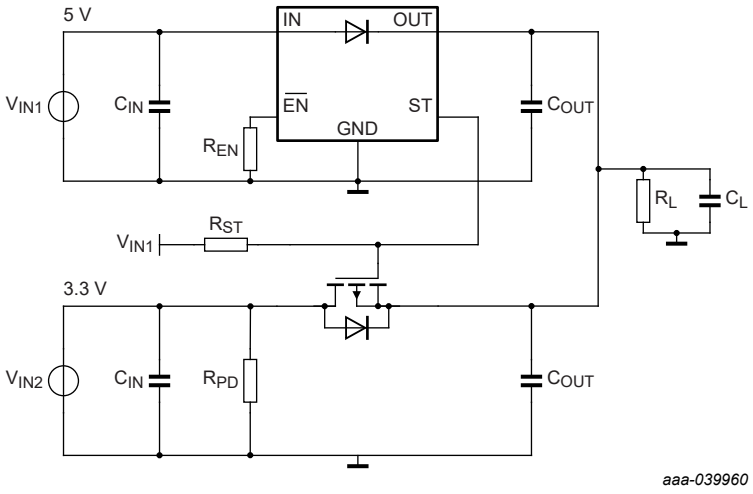
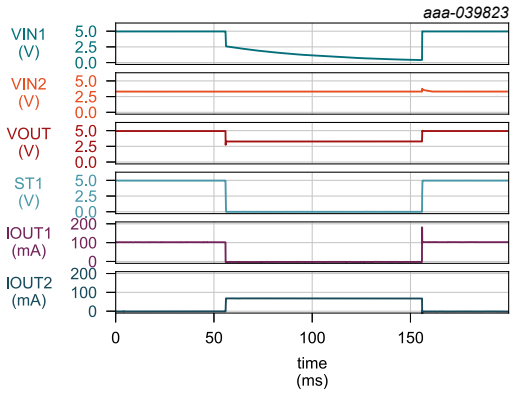


Fig. 42. OR-ing with external PMOS

The figures below show the switchover performance between V_{IN1} and V_{IN2}. A resistor, R_{PD}, to ground is recommended to prevent any reverse leakage from charging the 3.3 V C_{IN} capacitor and raising the V_{IN2} voltage in the event the 3.3 V supply is disconnected.



R_L = 47 Ω

Fig. 43. Switchover from V_{IN1} (5 V)to V_{IN2} (3.3 V) back to V_{IN1} (5 V)

10. Power supply recommendations

The device is designed to operate with a V_{IN} range of 1.2 V to 5.5 V. The V_{IN} power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps.

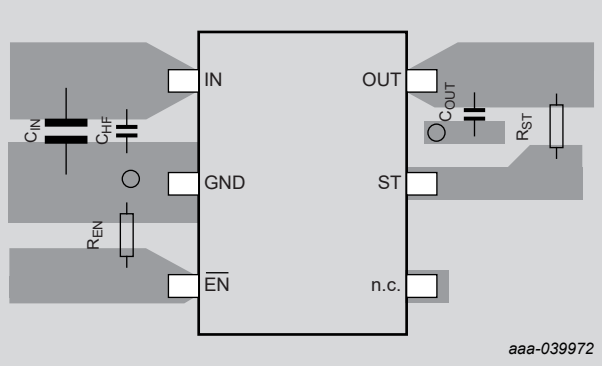
In most situations, using an input capacitance (C_{IN}) of 0.1 + 1 µF is sufficient to prevent the supply voltage from drooping. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

An effective capacitance of ≥ 0.1 µF, after applying voltage and temperature derating factors, is required on the OUT pin to ensure stability of the control loop Gm amplifier. NID5100 does not have over current protection and the maximum output capacitance should not exceed approximately 100 µF.

11. Layout

Layout guidelines

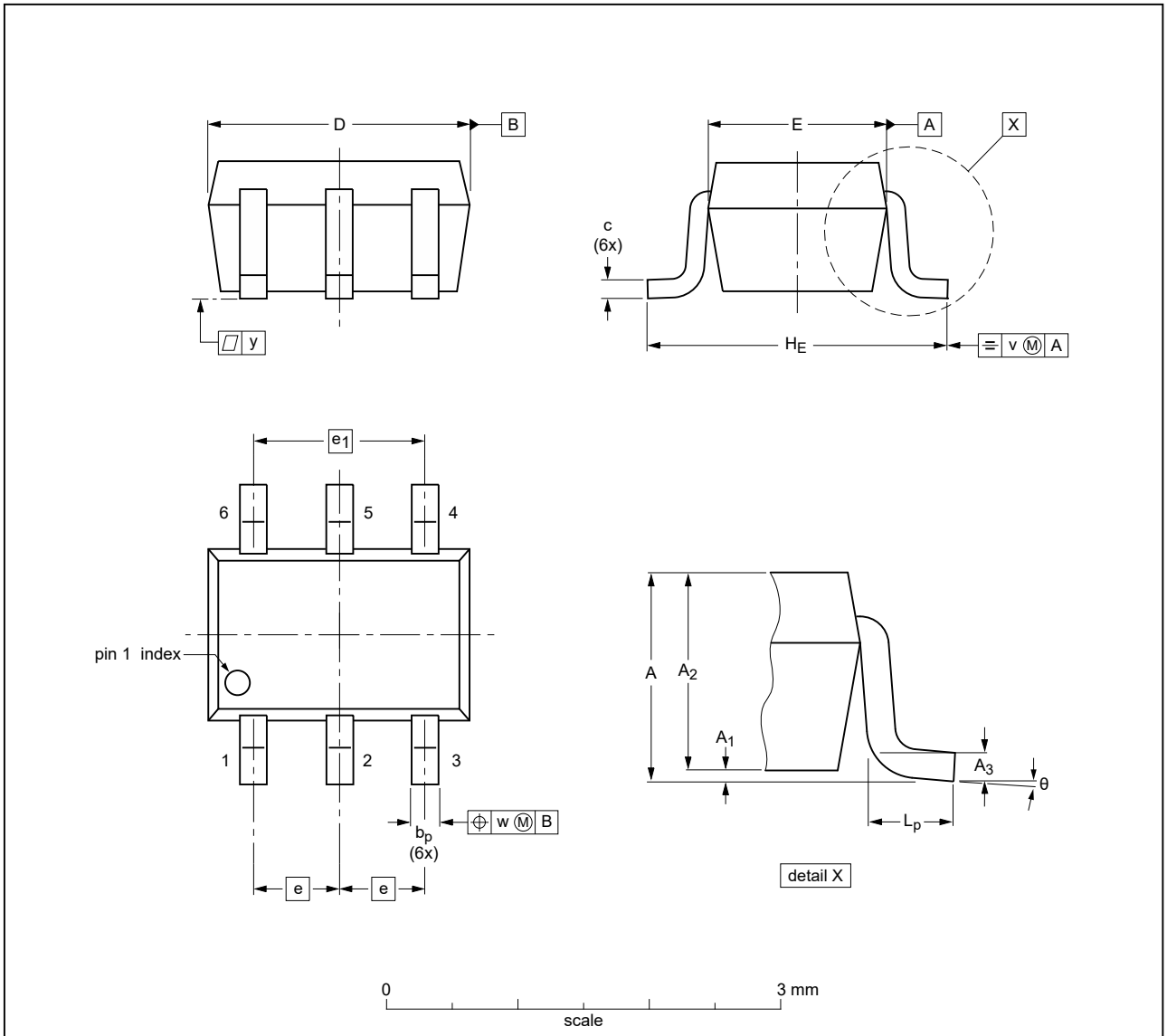
For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT} and GND helps minimize the parasitic electrical effects.



12. Package information

12.1. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm **SOT363-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot363-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT363-2		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 44. Package outline SOT363-2 (TSSOP6)

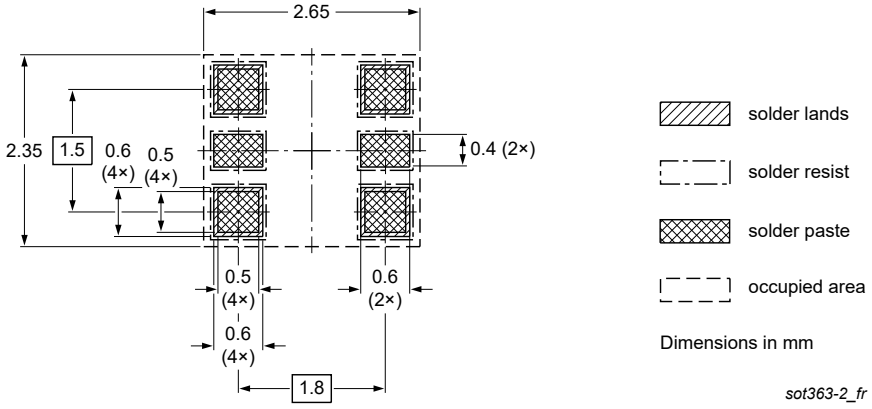


Fig. 45. Reflow soldering footprint SOT363-2 (TSSOP6)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
IEC	International Electrotechnical Commission
JEDEC	Joint Electron Device Engineering Council
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PMOS	P-channel Metal-Oxide Semiconductor

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NID5100 v.1	20240726	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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