

PESD18VF1BLS-Q

Ultra-low capacitance bidirectional ESD protection diode

13 January 2023

Product data sheet

1. General description

Ultra-low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a DFN1006BD-2 (SOD882BD) leadless ultra small Surface-Mounted Device (SMD) plastic package, designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Ultra low diode capacitance C_d = 0.31 pF
- High reverse standoff voltage V_{RWM} = 18 V
- Very small voltage dependency of the capacitance
- ESD protection up to ±10 kV according to IEC 61000-4-2, level 4
- · Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- NFC antenna protection
- Protection of high-speed data lines

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C	-	-	18	V
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	-	0.31	0.45	pF

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5. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)		
2	K2	cathode (diode 2)		к1 🕢 К2
			Transparent top view	sym045
			DFN1006BD-2 (SOD882BD)	

6. Ordering information

Table 3. Ordering information Type number	Package				
	Name	Description	Version		
PESD18VF1BLS-Q		Leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.47 mm body	SOD882BD		

7. Marking

Table 4. Marking codes	
Type number	Marking code
PESD18VF1BLS-Q	ZIZ

8. Limiting values

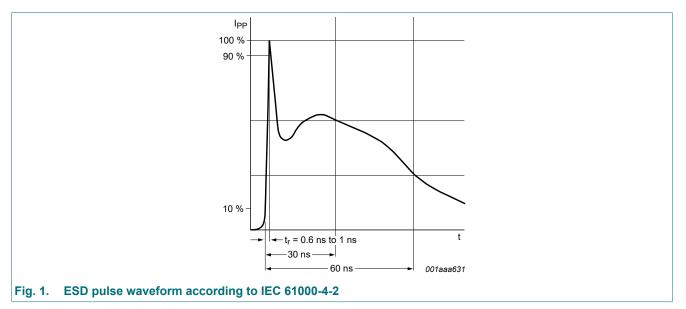
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximu	ım ratings					
V _{ESD}	electrostatic discharge	IEC 61000-4-2; contact discharge	[1] [2]	-	10	kV
	voltage	IEC 61000-4-2; air discharge	[1] [2]	-	15	kV

[1] Measured from pin 1 to pin 2.

[2] Device stressed with ten non-repetitive ESD pulses.

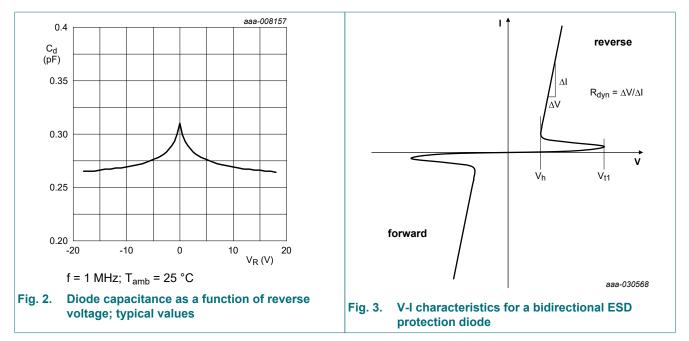


9. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	18	V
V _{BR}	breakdown voltage	I _R = 10 mA; T _{amb} = 25 °C		19	24	-	V
I _{RM}	reverse leakage current	V _R = 18 V; T _{amb} = 25 °C		-	1	30	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	0.31	0.45	pF
V _{CL}	clamping voltage	I _{TLP} = 8 A; t _p = 100 ns; T _{amb} = 25 °C	[1] [2]	-	17.5	-	V
		I _{TLP} = 16 A; t _p = 100 ns; T _{amb} = 25 °C	[1] [2]	-	20	-	V
R _{dyn}	dynamic resistance	I _R = 7.5 A; t _p = 100 ns; T _{amb} = 25 °C	[1] [2]	-	0.8	-	Ω

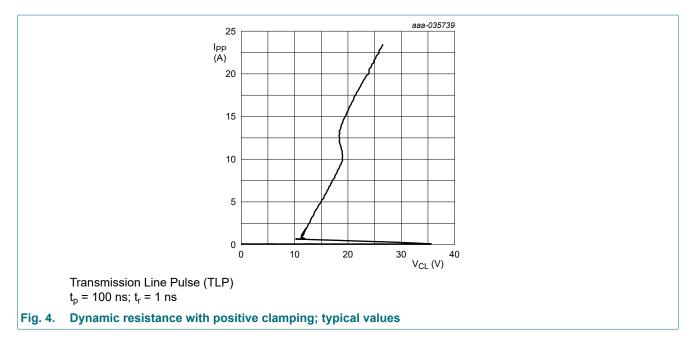
[1] Measured from pin 1 to pin 2.

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.



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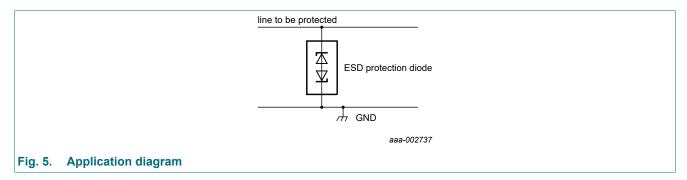
Ultra-low capacitance bidirectional ESD protection diode



10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

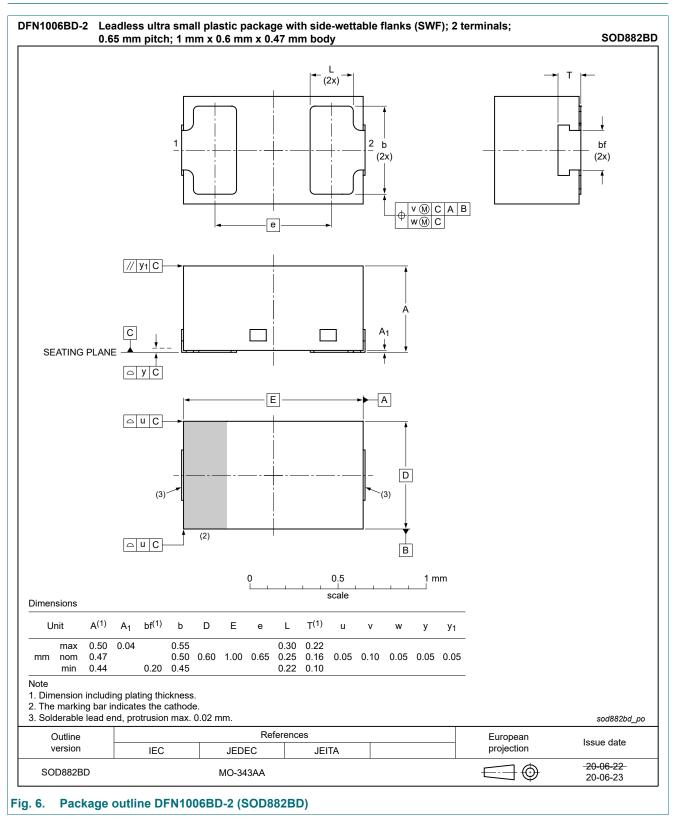
- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- **3.** Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

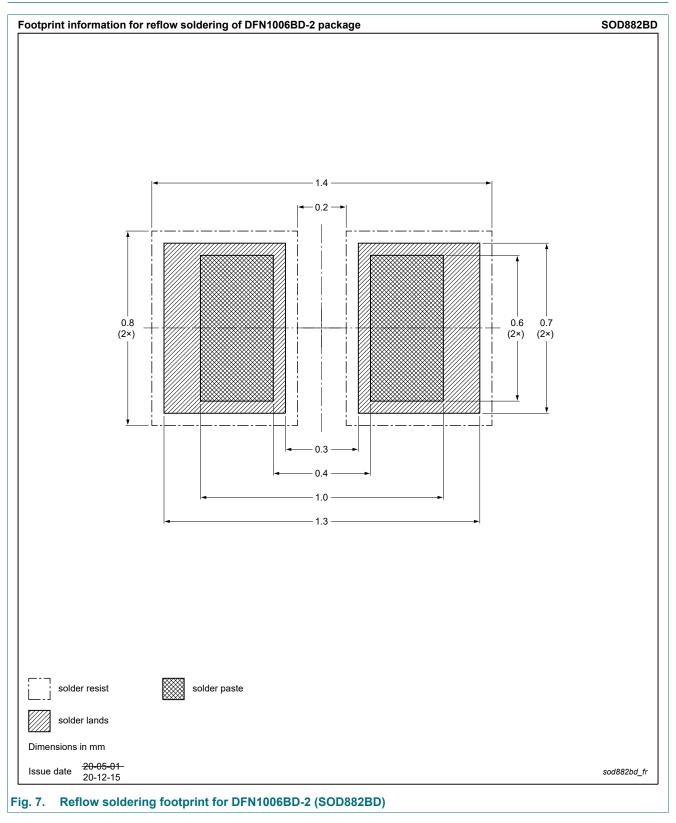
12. Package outline



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13. Soldering



14. Revision history

Table 7. Revision history					
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes	
PESD18VF1BLS-Q v.1	20230113	Product data sheet	-	-	

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <u>https://www.nexperia.com</u>.

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