NCA9535-Q100

Low-voltage 16-bit I²C and SMBus low-power I/O expander with interrupt output and configuration registers

Rev. 1 — 31 March 2023 Product data sheet

1. General description

The NCA9535-Q100 provides 16 bits of General Purpose Input/Output (GPIO) expansion for I²C-bus/SMBus applications. It is designed for a wide voltage range of 1.65 V to 5.5 V with interrupt. Nexperia GPIO expanders provide an elegant solution when additional IOs are needed while keeping the interconnections to a minimum, for example, in ACPI power switches, sensors, push buttons, LEDs and fan control. The NCA9535-Q100 contains a set of 8 bit input, output, configuration and polarity inversion registers. At power up all IOs default to inputs. Each IO can be configured as either input or output by changing the corresponding bit in the configuration register. The data for each input or output is stored in the corresponding input or output register. The polarity inversion register can be programmed to invert the polarity of the input register. The NCA9535-Q100 has an open-drain interrupt output which is activated when any one of the GPIO changes from its corresponding input port register state. The power on reset sets the registers to default values and initializes the device state machine. The NCA9535-Q100 has three address pins A0, A1 and A2 which can be used to configure the I²C bus slave address of the device. It allows up-to eight devices to share the same I²C-bus/SMBus.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

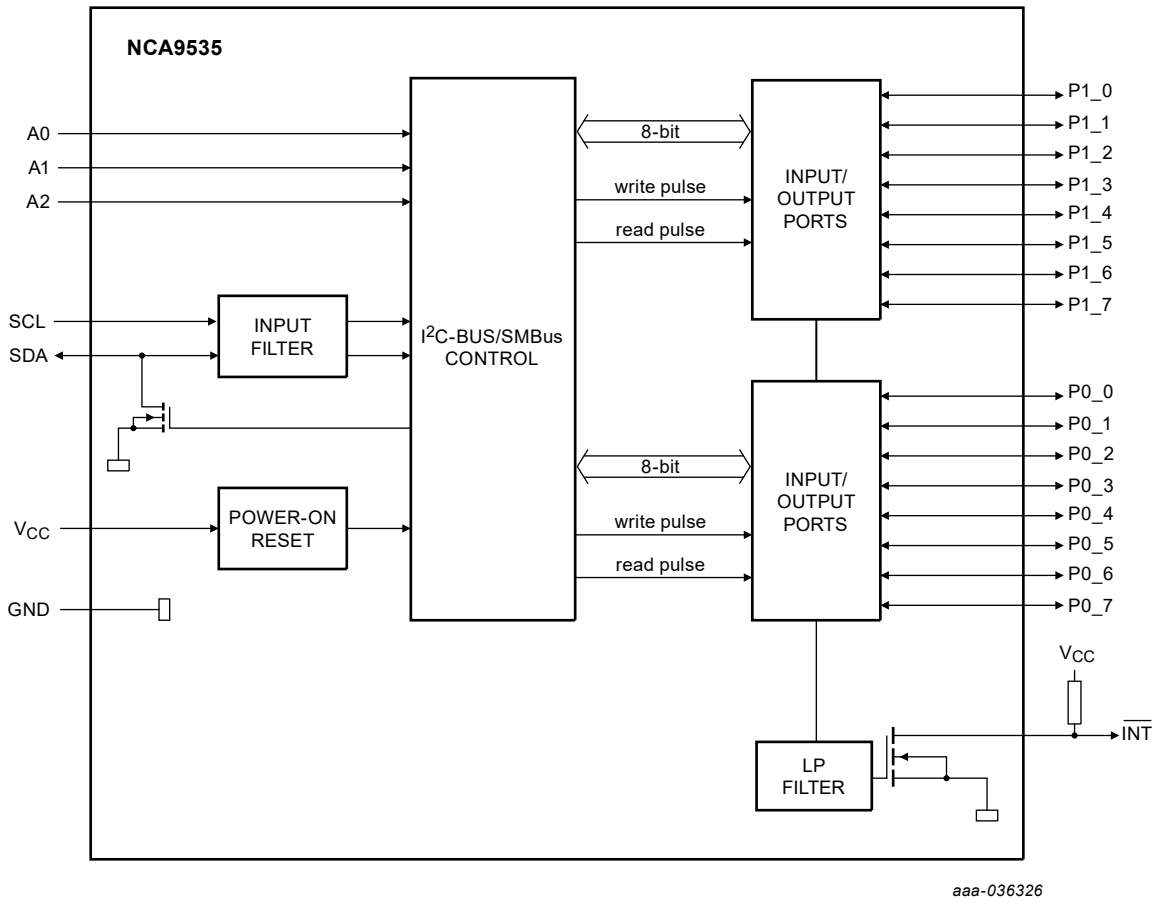
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +125 °C
- I²C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current consumption:
  - 4 µA (maximum)
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - V_{hys} = 0.10 × V_{CC} (typical)
  - Noise filter on SCL and SDA inputs
- 5 V tolerant I/Os
- 16 I/O pins which power up configured in input state
- Open-drain active LOW interrupt output ($\overline{INT}$)
- 400 kHz Fast-mode I²C-bus
- Internal power-on reset
- No glitch on power-up
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD78, Class II
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 1000 V
- Package offered: TSSOP24

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NCA9535PW-Q100	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

4. Block diagram



Remark: All I/Os are set to inputs at reset.

Fig. 1. Block diagram of NCA9535-Q100

5. Pinning information

5.1. Pinning

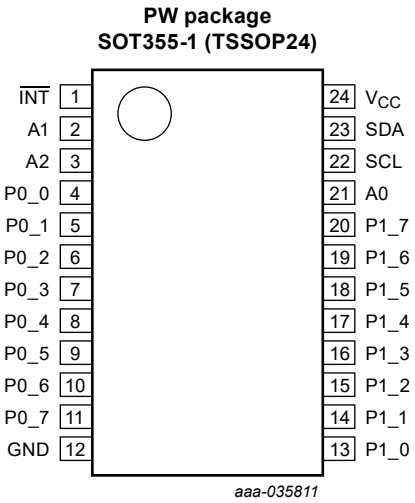


Fig. 2. Pin configuration SOT355-1 (TSSOP24)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
$\overline{INT}$	1	O	Interrupt output. Connect to V_{CC} through a pull-up resistor
A1	2	I	Address input 1. Connect directly to V_{CC} or GND
A2	3	I	Address input 2. Connect directly to V_{CC} or GND
P0_0 [1]	4	I/O	Parallel port I/O. Push-pull driver. At power on, P0_0 is configured as input
P0_1 [1]	5	I/O	Parallel port I/O. Push-pull driver. At power on, P0_1 is configured as input
P0_2 [1]	6	I/O	Parallel port I/O. Push-pull driver. At power on, P0_2 is configured as input
P0_3 [1]	7	I/O	Parallel port I/O. Push-pull driver. At power on, P0_3 is configured as input
P0_4 [1]	8	I/O	Parallel port I/O. Push-pull driver. At power on, P0_4 is configured as input
P0_5 [1]	9	I/O	Parallel port I/O. Push-pull driver. At power on, P0_5 is configured as input
P0_6 [1]	10	I/O	Parallel port I/O. Push-pull driver. At power on, P0_6 is configured as input
P0_7 [1]	11	I/O	Parallel port I/O. Push-pull driver. At power on, P0_7 is configured as input
GND	12	power	Ground
P1_0 [2]	13	I/O	Parallel port I/O. Push-pull driver. At power on, P1_0 is configured as input
P1_1 [2]	14	I/O	Parallel port I/O. Push-pull driver. At power on, P1_1 is configured as input
P1_2 [2]	15	I/O	Parallel port I/O. Push-pull driver. At power on, P1_2 is configured as input
P1_3 [2]	16	I/O	Parallel port I/O. Push-pull driver. At power on, P1_3 is configured as input
P1_4 [2]	17	I/O	Parallel port I/O. Push-pull driver. At power on, P1_4 is configured as input
P1_5 [2]	18	I/O	Parallel port I/O. Push-pull driver. At power on, P1_5 is configured as input
P1_6 [2]	19	I/O	Parallel port I/O. Push-pull driver. At power on, P1_6 is configured as input
P1_7 [2]	20	I/O	Parallel port I/O. Push-pull driver. At power on, P1_7 is configured as input
A0	21	I	Address input 0. Connect directly to V_{CC} or GND

Symbol	Pin	Type	Description
SCL	22	I	Serial clock bus. Connect to V_{CC} through a pull-up resistor
SDA	23	I/O	Serial data bus. Connect to V_{CC} through a pull-up resistor.
V_{CC}	24	power	Supply voltage.

[1] Pins P0_0 to P0_7 correspond to bits P0.0 to P0.7. At power-up, all I/O are configured as high-impedance inputs.
[2] Pins P1_0 to P1_7 correspond to bits P1.0 to P1.7. At power-up, all I/O are configured as high-impedance inputs.

6. Functional description

For the block diagram of the NCA9535-Q100 see Fig. 1.

6.1. Device address

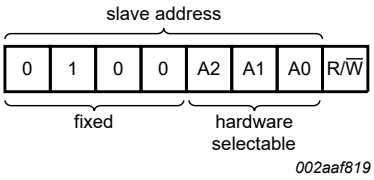


Fig. 3. NCA9535-Q100 device address

A2, A1 and A0 are the hardware address package pins and are held to either HIGH (logic 1) or LOW (logic 0) to assign one of the eight possible slave addresses. The last bit of the slave address (R/$\overline{W}$) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

6.2. Registers

6.2.1. Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the address pointer register of the NCA9535-Q100. The lower three bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register is write only.

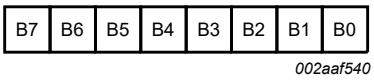


Fig. 4. Pointer register bits

Table 3. Command byte

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx [1]
0	0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx
0	0	0	0	0	0	1	0	02h	Output port 0	read/write byte	1111 1111
0	0	0	0	0	0	1	1	03h	Output port 1	read/write byte	1111 1111
0	0	0	0	0	1	0	0	04h	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	0	0	1	0	1	05h	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	0	0	1	1	0	06h	Configuration port 0	read/write byte	1111 1111
0	0	0	0	0	1	1	1	07h	Configuration port 1	read/write byte	1111 1111

[1] The default value 'X' is determined by the externally applied logic level.

6.2.2. Input port register pair (00h, 01h)

The Input port registers (registers 0 and 1) reflect the logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in Section 7.2.

Table 4. Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 5. Input port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

6.2.3. Output port register pair (02h, 03h)

The Output port registers (registers 2 and 3) define the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. A register pair write is described in Section 7.1 and a register pair read is described in Section 7.2.

Table 6. Output port 0 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 7. Output port 1 register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

6.2.4. Polarity inversion register pair (04h, 05h)

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the Input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained. A register pair write is described in Section 7.1 and a register pair read is described in Section 7.2.

Table 8. Polarity inversion port 0 register (address 04h)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 9. Polarity inversion port 1 register (address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

6.2.5. Configuration register pair (06h, 07h)

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register pair write is described in Section 7.1 and a register pair read is described in Section 7.2.

Table 10. Configuration port 0 register (address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

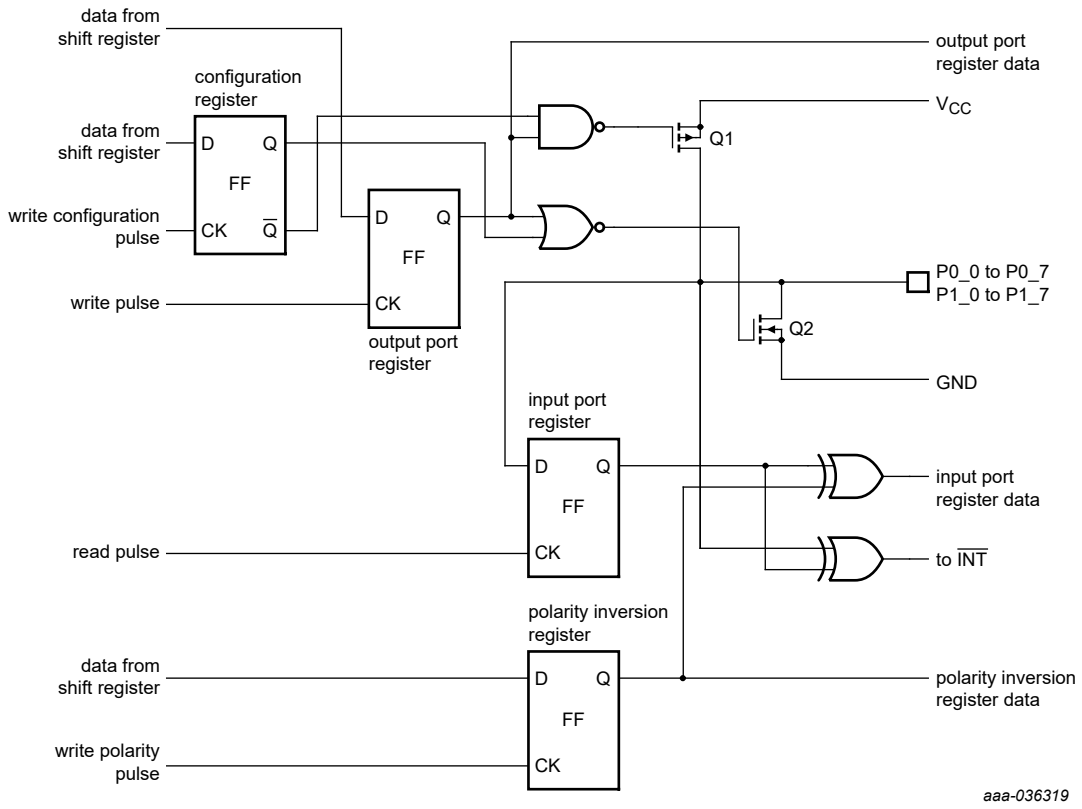
Table 11. Configuration port 1 register (address 07h)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

6.3. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



At power-on reset, all registers return to default values.

Fig. 5. Simplified schematic of the I/Os (P0_0 to P0_7, P1_0 to P1_7)

6.4. Power-on reset

When power (from 0 V) is applied to V_{CC} and starts rising, an internal power-on reset holds the NCA9535-Q100 in a reset condition until V_{CC} has reached V_{PORR}. At that time, the reset condition is released and the NCA9535-Q100 registers and I²C-bus/SMBus state machine initializes to their default states. After that, V_{CC} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle. See Section 8.2.

6.5. Interrupt output

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time $t_{v(INT)}$, the signal $\overline{INT}$ is valid. The interrupt is reset when data on the port changes back to the original value or when data is read form the port that generated the interrupt (see Fig. 9 and Fig. 10). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

7. Bus transactions

The NCA9535-Q100 is an I²C-bus slave device. Data is exchanged between the master and NCA9535-Q100 through write and read commands using I²C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1. Writing to the port registers

Data is transmitted to the NCA9535-Q100 by sending the start condition, device address and setting the read-write bit to a logic 0 (see Fig. 3). The command byte is sent after the address and determines which register will receive the data following the command byte.

Eight registers within the NCA9535-Q100 are configured to operate as four register pairs. The four pairs are input port, output port, polarity inversion, configuration registers. After sending data to one register, the next data byte is sent to the other register in the pair (see Fig. 6 and Fig. 7). For example, if the first byte is sent to output port 1 (register 3), the next byte is stored in output port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register pair independently of the other registers, or the host can simply update a single register.

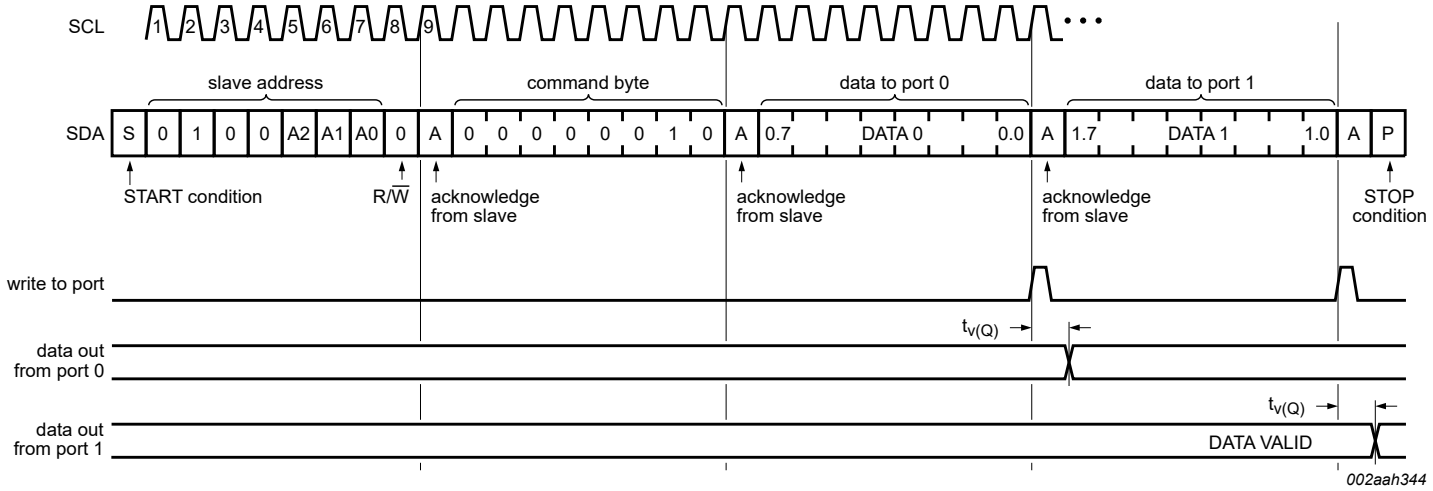


Fig. 6. Write to output port registers

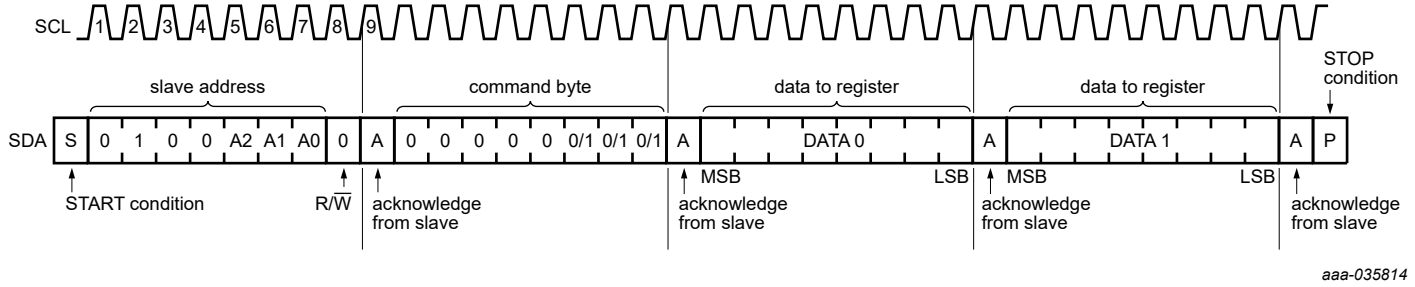
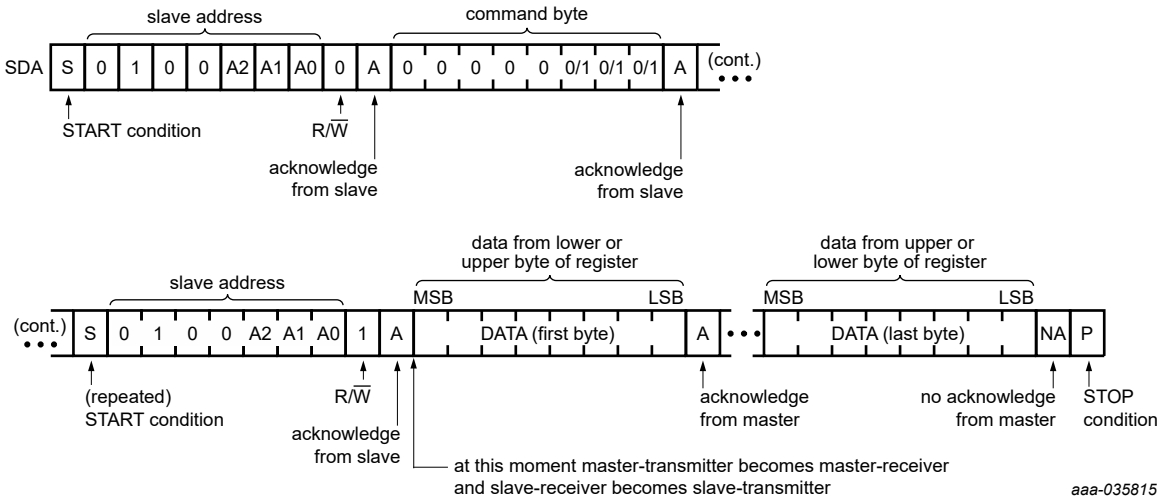


Fig. 7. Write to Control registers

7.2. Reading the port registers

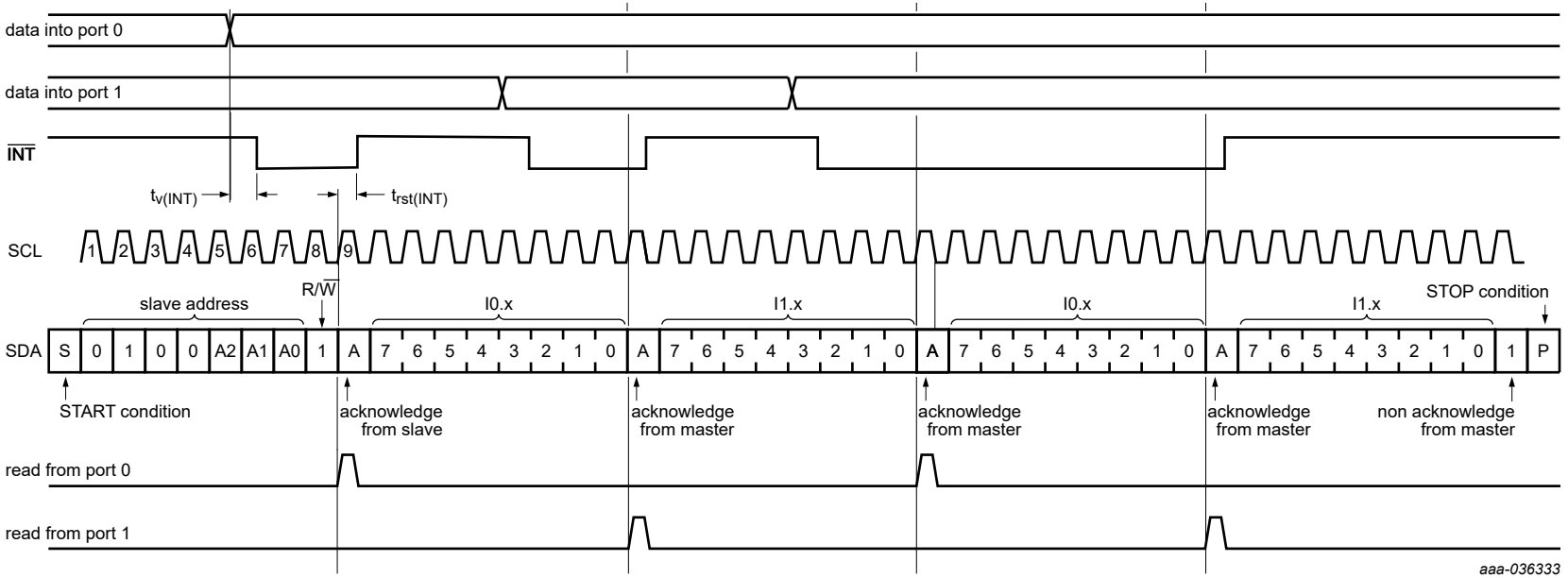
In order to read data from the NCA9535-Q100, the bus master must first send the start condition, NCA9535-Q100 address with the read-write bit set to a logic 0 (see Fig. 3). The command byte is sent after the address and determines which register will be accessed. After a start or restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte is sent by the NCA9535-Q100 (see Fig. 8, Fig. 9 and Fig. 10). Data is clocked into the register on the rising edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

After a subsequent start or restart, the command byte contains the value of the next register to be read in the pair. For example, if Input Port 1 was read last before the restart, the register that is read after the restart is the Input Port 0.



Remark: Transfer can be stopped at any time by a STOP condition.

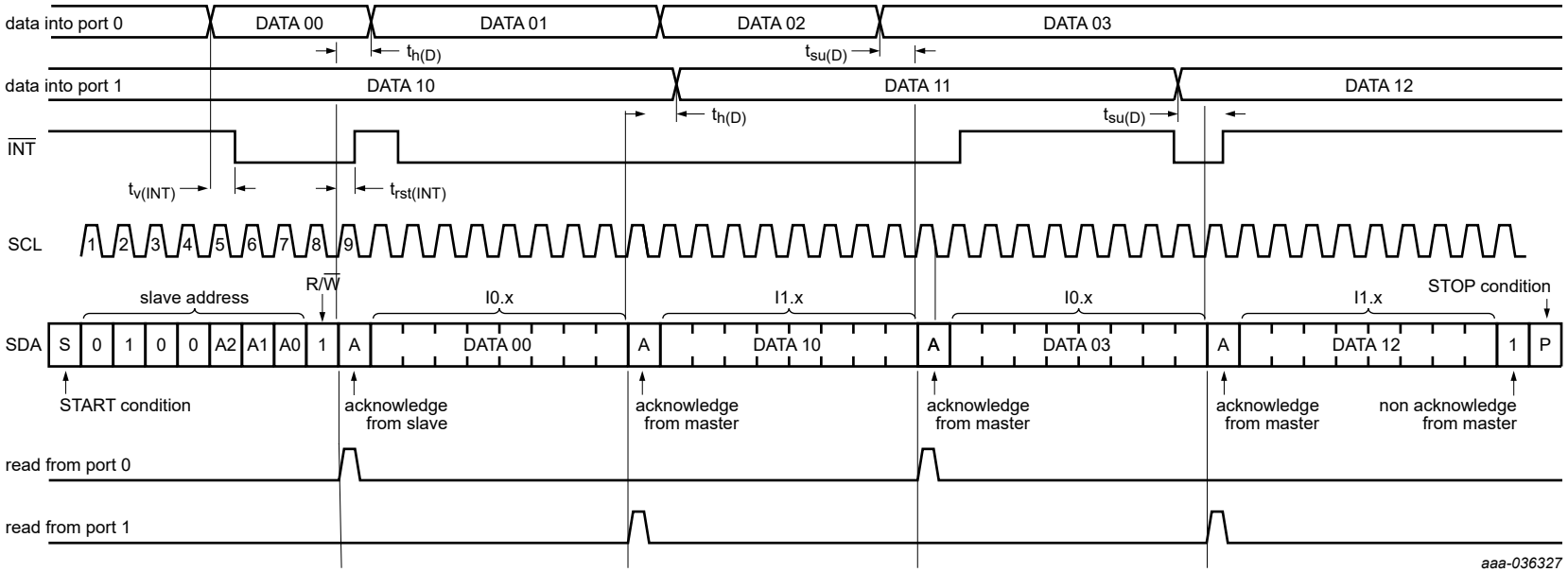
Fig. 8. Read from register



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00h' (read input port register).

This figure eliminates the command byte transfer and a restart between the initial slave address call and the actual data transfer from P port (see Fig. 8).

Fig. 9. Read input port register, scenario 1

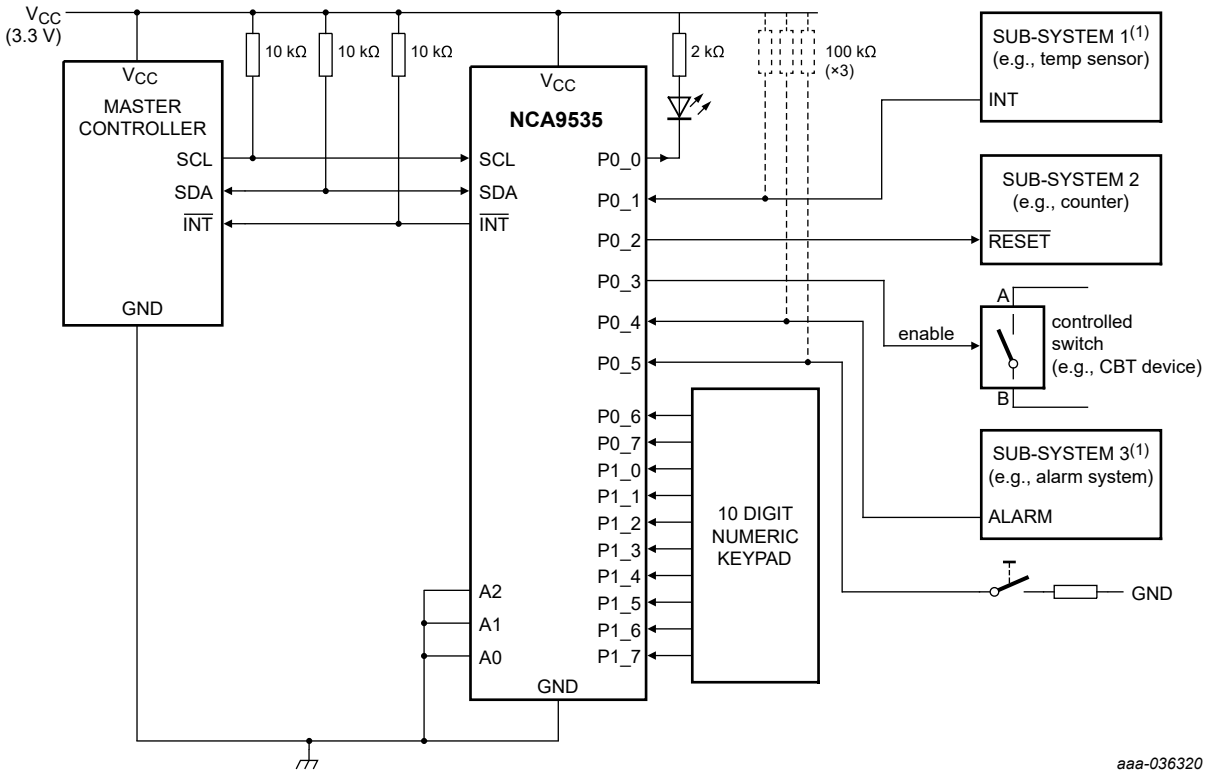


Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00h' (read input port register).

This figure eliminates the command byte transfer and a restart between the initial slave address call and the actual data transfer from P port (see Fig. 8).

Fig. 10. Read input port register, scenario 2

8. Application design-in information



Device address configured as 0100 000X for this example.
P0_0, P0_2, P0_3 configured as outputs.
P0_1, P0_4, P0_5 configured as inputs.
P0_6, P0_7 and (P1_0 to P1_7) configured as inputs.

(1) External pull-up and pull-down resistors are required for inputs IO P ports that may float. If a driver to an input will never let the input float, a resistor is not needed. If an output in the P port is configured as a push-pull output there is no need for external pull-up resistors. If an output in the P port is configured as an open-drain output, external pull-up resistors are required.

Fig. 11. Typical application

8.1. Minimizing I_{CC} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{CC} through a resistor as shown in Fig. 11. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{CC}. The supply current, I_{CC}, increases as V_I becomes lower than V_{CC}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{CC} when the LED is off. Fig. 12 shows a high value resistor in parallel with the LED. Fig. 13 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{CC} and prevents additional supply current consumption when the LED is off.

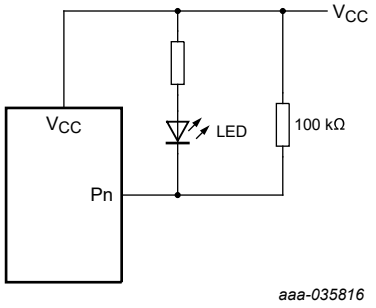


Fig. 12. High value resistor in parallel with the LED

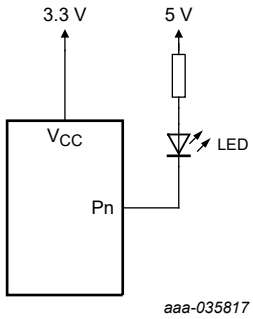


Fig. 13. Device supplied by a lower voltage

8.2. Power-on reset requirements

In the event of a glitch or data corruption, NCA9535-Q100 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Fig. 14 and Fig. 15.

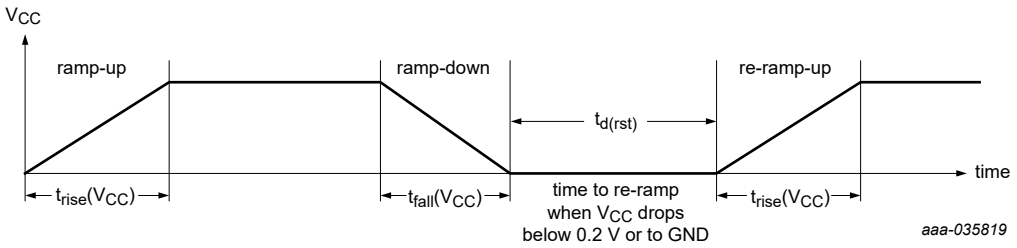


Fig. 14. V_{CC} is lowered below 0.2 V or to 0 V and then ramped up to V_{CC}

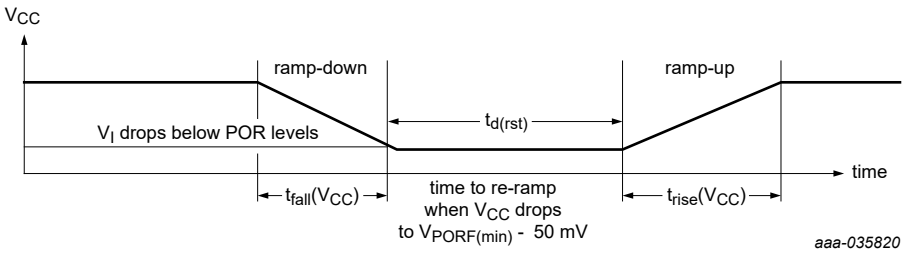


Fig. 15. V_{CC} is lowered below the POR threshold, then ramped back up to V_{CC}

Table 12 specifies the performance of the power-on reset feature for NCA9535-Q100 for both types of power-on reset.

Table 12. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition	T_{amb} = 25 °C			Unit
			Min	Typ	Max	
$t_{rise(V_{CC})}$	supply ramp up time	Fig. 14	0.1	-	2000	ms
$t_{fall(V_{CC})}$	supply ramp down time	Fig. 14	0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Fig. 14; re-ramp time when V_{CC} drops below 0.2 V or to GND	1	-	-	µs
		Fig. 15; re-ramp time when V_{CC} drops to $V_{POR(min)}$ - 50 mV	1	-	-	µs
$\Delta V_{CC(gl)}$	glitch supply voltage difference	Fig. 16	-	-	1	V
$V_{CC\_MIN(gl)}$	minimum glitch supply voltage	minimum voltage that V_{CC} can glitch down to, but not cause functional disruption when $t_{w(gl)V_{CC}}$ Fig. 16	1.5	-	-	V
$t_{w(gl)V_{CC}}$	supply voltage glitch pulse width	Fig. 16	-	-	10	µs

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)V_{CC}}$) and glitch height ($\Delta V_{CC(gl)}$) are dependent on each other. The glitch on power supply should never go below $V_{CC\_MIN(gl)}$ in order to properly guarantee functionality. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Fig. 16 and Table 12 provide more information on how to measure these specifications.

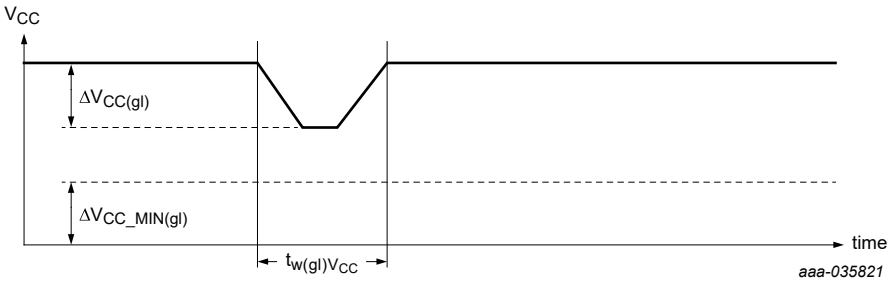


Fig. 16. Glitch width and glitch height

V_{PORR} and V_{PORF} are critical to the power-on reset. V_{PORR} is the voltage level of V_{CC} at which the reset condition is released and all the registers and the I²C-bus/SMBus state machine are initialized to their default states. V_{PORF} is the voltage level of V_{CC} below which NCA9535-Q100 enters reset state. Fig. 17 and Section 12 provide more details on this specification.

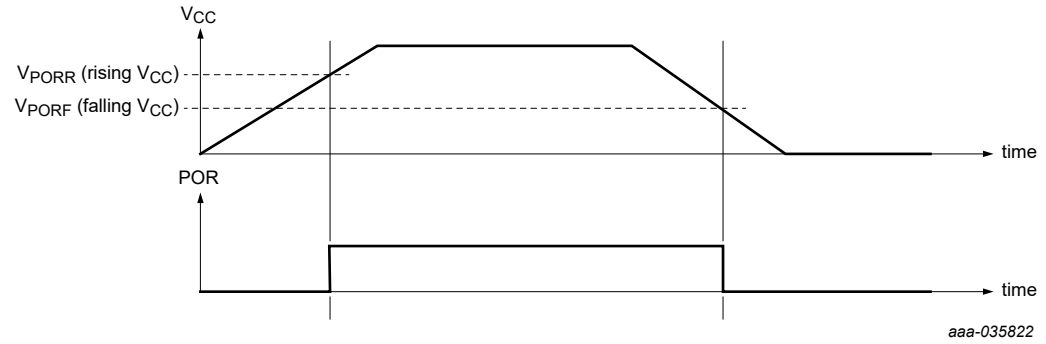


Fig. 17. Power-on reset voltage (V_{POR})

9. Limiting values

Table 13. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	6	V
V_I	input voltage	[1]	-0.5	6	V
V_O	output voltage	[1]	-0.5	6	V
I_{IK}	input clamping current	A0, A1, A2, SCL; $V_I < 0$ V	-	-20	mA
I_{OK}	output clamping current	$\overline{INT}$; $V_O < 0$ V	-	-20	mA
I_{IOK}	input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{CC}$	-	±20	mA
		SDA; $V_O < 0$ V	-	-20	mA
I_{OL}	LOW-level output current	continuous; I/O port	-	50	mA
		continuous; SDA, $\overline{INT}$	-	25	mA
I_{OH}	HIGH-level output current	continuous; P port	-	25	mA
I_{CC}	supply current		-	160	mA
I_{GND}	ground supply current		-	250	mA
P_{tot}	total power dissipation		-	200	mW
T_{stg}	storage temperature		-65	+150	°C
$T_{j(max)}$	maximum junction temperature		-	135	°C
T_{amb}	ambient temperature	operating in free air	-40	+125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

10. Recommended operating conditions

Table 14. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA	$0.7 \times V_{CC}$	5.5	V
		P1_7 to P0_0	$0.7 \times V_{CC}$	5.5	V
		A0, A1, A2,	$0.7 \times V_{CC}$	V_{CC}	V
V_{IL}	LOW-level input voltage	SCL, SDA	-0.5	$0.3 \times V_{CC}$	V
		A0, A1, A2, P1_7 to P0_0	-0.5	$0.3 \times V_{CC}$	V
I_{OH}	HIGH-level output current	P1_7 to P0_0	-	10	mA
I_{OL}	LOW-level output current	P1_7 to P0_0	-	25	mA

11. Thermal characteristics

Table 15. Thermal characteristics

Symbol	Parameter	Conditions	Max	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	TSSOP24 package [1]	100	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

12. Static characteristics

Table 16. Static characteristics

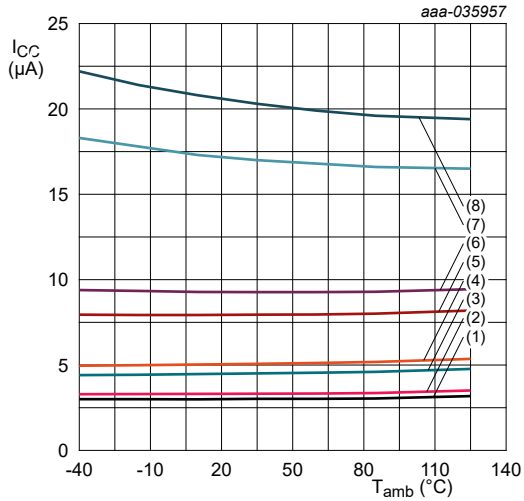
V_{CC} = 1.65 V to 5.5 V; unless otherwise specified.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ [1]	Max	
V_{IK}	input clamping voltage	I_I = -18 mA	-1.2	-	-	V
V_{PORF}	power-on reset trip voltage; V_{CC} falling	V_I = V_{CC} or GND; I_O = 0 mA	0.8	1.1	-	V
V_{PORR}	power-on reset trip voltage; V_{CC} rising	V_I = V_{CC} or GND; I_O = 0 mA	-	1.25	1.6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{CC} = 1.65 V to 5.5 V				
		SDA	3	-	-	mA
		$\overline{INT}$	3	28 [2]	-	mA
		P port				
		V_{OL} = 0.5 V; V_{CC} = 1.65 V [3]	8	-	-	mA
		V_{OL} = 0.7 V; V_{CC} = 1.65 V [3]	9	-	-	mA
		V_{OL} = 0.5 V; V_{CC} = 2.3 V [3]	8	-	-	mA
		V_{OL} = 0.7 V; V_{CC} = 2.3 V [3]	10	-	-	mA
		V_{OL} = 0.5 V; V_{CC} = 3.0 V [3]	8	-	-	mA
		V_{OL} = 0.7 V; V_{CC} = 3.0 V [3]	10	-	-	mA
		V_{OL} = 0.5 V; V_{CC} = 4.5 V [3]	8	-	-	mA
		V_{OL} = 0.7 V; V_{CC} = 4.5 V [3]	10	-	-	mA
V_{OH}	HIGH-level output voltage	P port				
		I_{OH} = -8 mA; V_{CC} = 1.65 V [4]	1.2	-	-	V
		I_{OH} = -10 mA; V_{CC} = 1.65 V [4]	1.05	-	-	V
		I_{OH} = -8 mA; V_{CC} = 2.3 V [4]	2.0	-	-	V
		I_{OH} = -10 mA; V_{CC} = 2.3 V [4]	1.9	-	-	V
		I_{OH} = -8 mA; V_{CC} = 3.0 V [4]	2.6	-	-	V
		I_{OH} = -10 mA; V_{CC} = 3.0 V [4]	2.5	-	-	V
		I_{OH} = -8 mA; V_{CC} = 4.5 V [4]	4.1	-	-	V
		I_{OH} = -10 mA; V_{CC} = 4.5 V [4]	4.0	-	-	V
V_{OL}	LOW-level output voltage	P port; I_{OL} = 8 mA				
		V_{CC} = 1.65 V	-	-	0.45	V
		V_{CC} = 2.3 V	-	-	0.30	V
		V_{CC} = 3.0 V	-	-	0.25	V
		V_{CC} = 4.5 V	-	-	0.2	V
I_I	input current	V_{CC} = 1.65 V to 5.5 V				
		SCL, SDA; V_I = V_{CC} or GND	-	-	1	µA
		A0, A1, A2; V_I = V_{CC} or GND	-	-	±1	µA
I_{IH}	HIGH-level input current	P port; V_I = V_{CC}; V_{CC} = 1.65 V to 5.5 V	-	-	1	µA
I_{IL}	LOW-level input current	P port; V_I = GND; V_{CC} = 1.65 V to 5.5 V	-	-	-1	µA

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ [1]	Max	
I_{CC}	supply current	SDA, P port, A0, A1, A2; V_I on SDA = V_{CC} or GND; V_I on P port and A0, A1, A2 = V_{CC}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz (t_r = 30 ns)				
		V_{CC} = 3.6 V to 5.5 V	-	13	29	µA
		V_{CC} = 2.3 V to 3.6 V	-	6.4	12	µA
		V_{CC} = 1.65 V to 2.3 V	-	3	6.5	µA
		SCL, SDA, P port, A0, A1, A2; V_I on SCL, SDA = V_{CC} or GND; V_I on P port and A0, A1, A2 = V_{CC}; I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz				
		V_{CC} = 3.6 V to 5.5 V	-	1.5	4	µA
		V_{CC} = 2.3 V to 3.6 V	-	0.95	3	µA
		V_{CC} = 1.65 V to 2.3 V	-	0.5	2	µA
		Active mode; P port, A0, A1, A2; V_I on P port, A0, A1, A2 = V_{CC}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz (t_r = 30 ns) continuous register read				
		V_{CC} = 3.6 V to 5.5 V	-	15	60	µA
		V_{CC} = 2.3 V to 3.6 V	-	7.4	27	µA
		V_{CC} = 1.65 V to 2.3 V	-	3.5	11	µA
ΔI_{CC}	additional quiescent supply current	SCL, SDA; one input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND; V_{CC} = 1.65 V to 5.5 V	-	-	10	µA
		P port, A0, A1, A2; one input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND; V_{CC} = 1.65 V to 5.5 V	-	-	18	µA
C_i	input capacitance	V_I = V_{CC} or GND; V_{CC} = 1.65 V to 5.5 V	-	1.5	3.5	pF
C_{io}	input/output capacitance	$V_{I/O}$ = V_{CC} or GND; V_D = 1.65 V to 5.5 V	-	3	5	pF

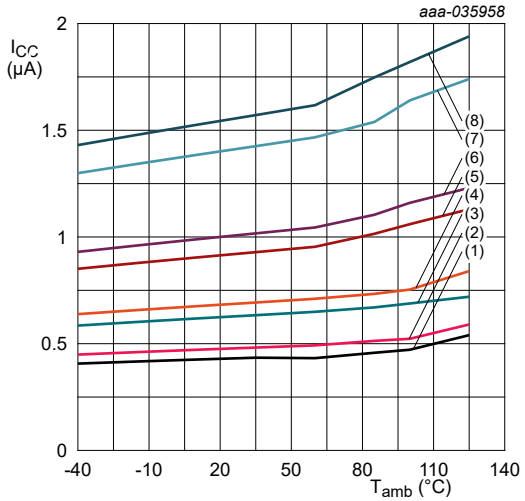
[1] For I_{CC}, all typical values are at nominal supply voltage (1.8 V, 3.3 V or 5 V V_{CC}) and T_{amb} = 25 °C. Except for I_{CC}, the typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
[2] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and V_{CC} = 3.3 V.
[3] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 200 mA.
[4] The total current sourced by all I/Os must be limited to 160 mA.

12.1. Typical characteristics



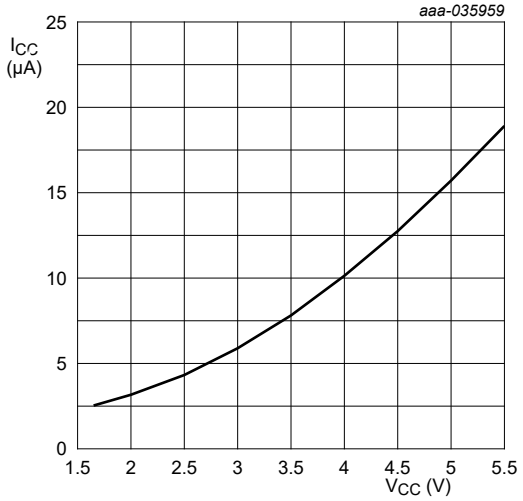
f_{SCL} = 400 kHz
(1) V_{CC} = 1.65 V
(2) V_{CC} = 1.8 V
(3) V_{CC} = 2.3 V
(4) V_{CC} = 2.5 V
(5) V_{CC} = 3.3 V
(6) V_{CC} = 3.6 V
(7) V_{CC} = 5.0 V
(8) V_{CC} = 5.5 V

Fig. 18. Supply current versus ambient temperature



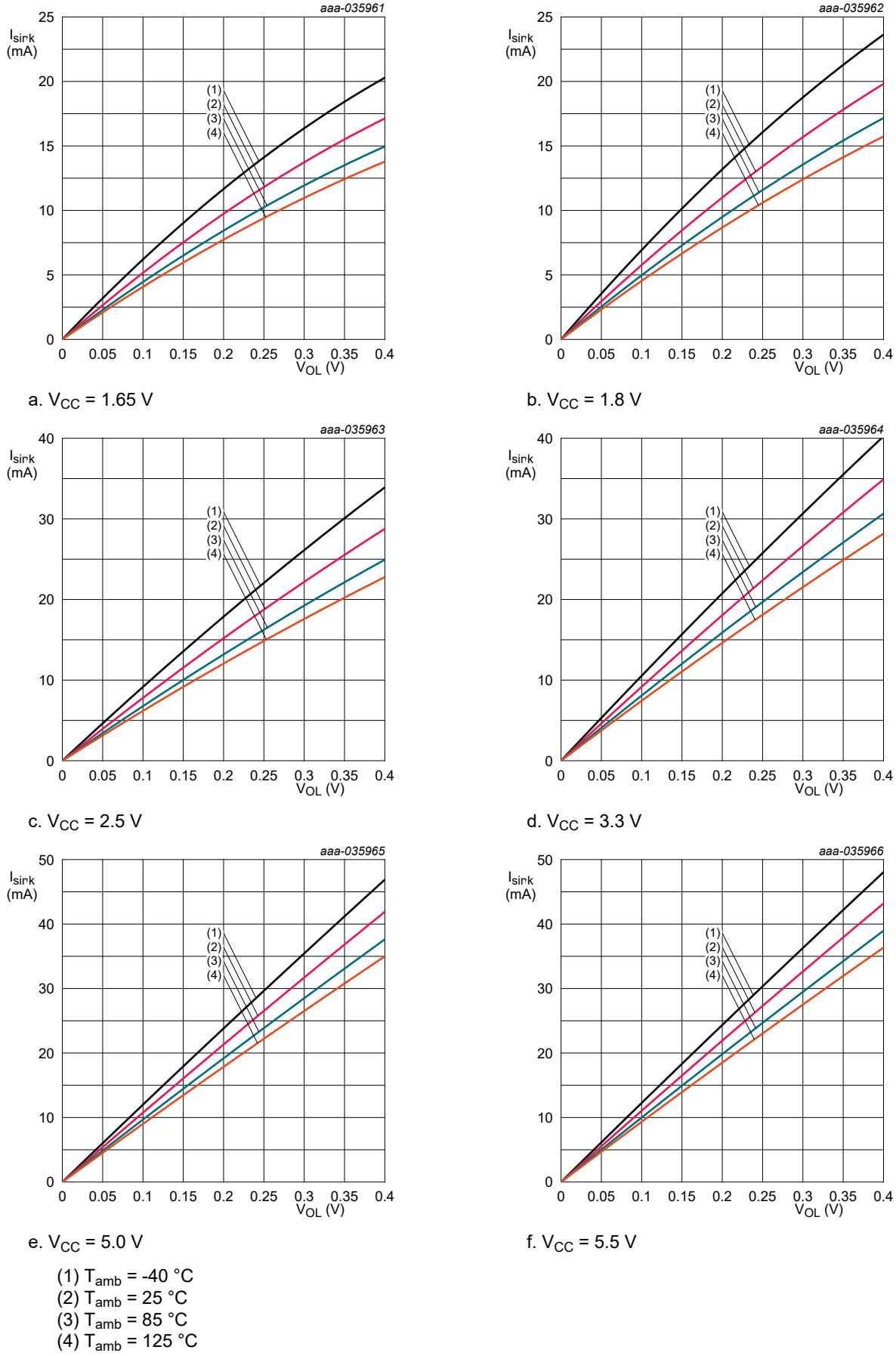
(1) V_{CC} = 1.65 V
(2) V_{CC} = 1.8 V
(3) V_{CC} = 2.3 V
(4) V_{CC} = 2.5 V
(5) V_{CC} = 3.3 V
(6) V_{CC} = 3.6 V
(7) V_{CC} = 5.0 V
(8) V_{CC} = 5.5 V

Fig. 19. Standby supply current versus ambient temperature



T_{amb} = 25 °C; f_{SCL} = 400 kHz

Fig. 20. Supply current versus supply voltage



a. V_{CC} = 1.65 V

b. V_{CC} = 1.8 V

c. V_{CC} = 2.5 V

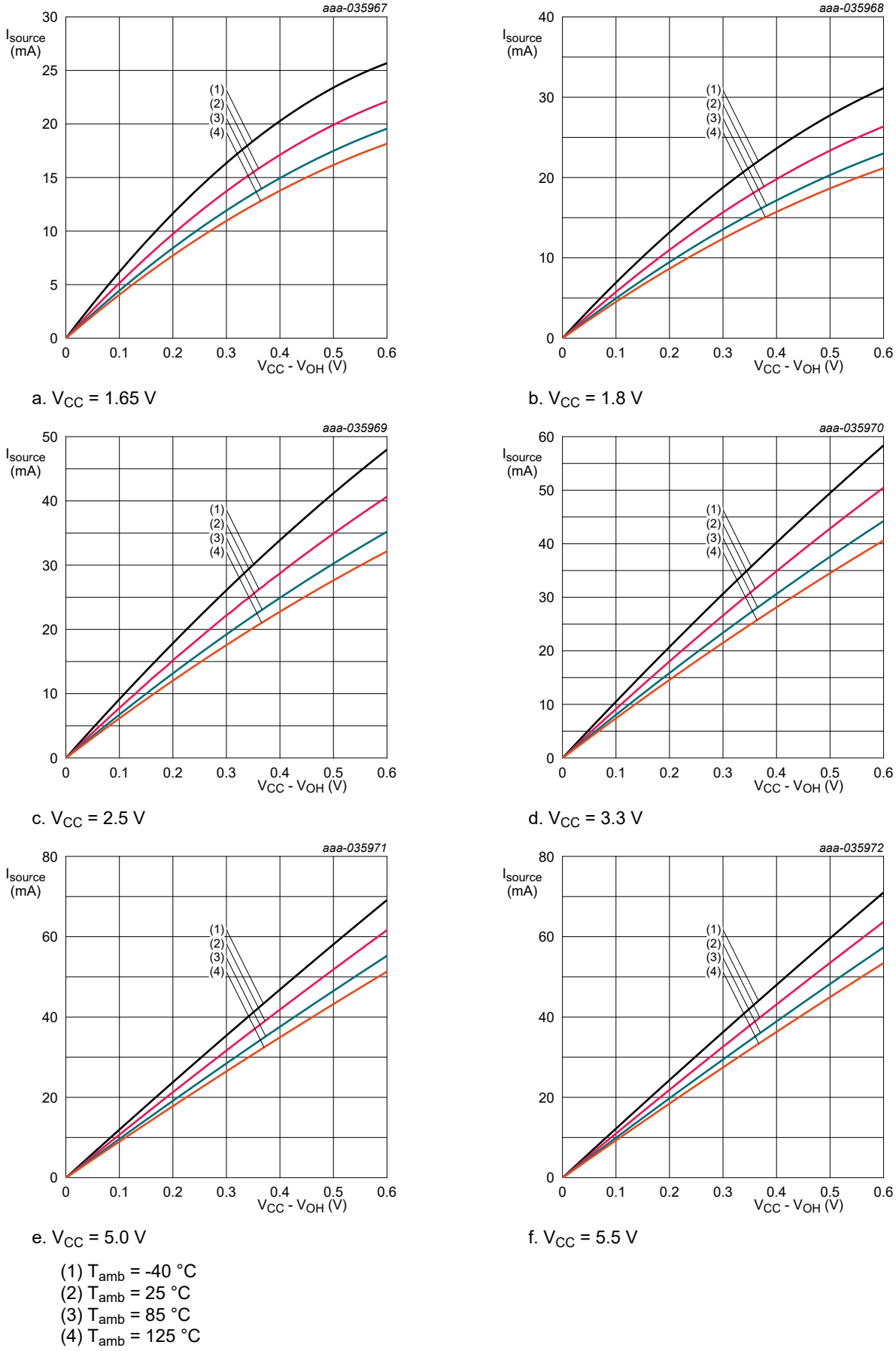
d. V_{CC} = 3.3 V

e. V_{CC} = 5.0 V

f. V_{CC} = 5.5 V

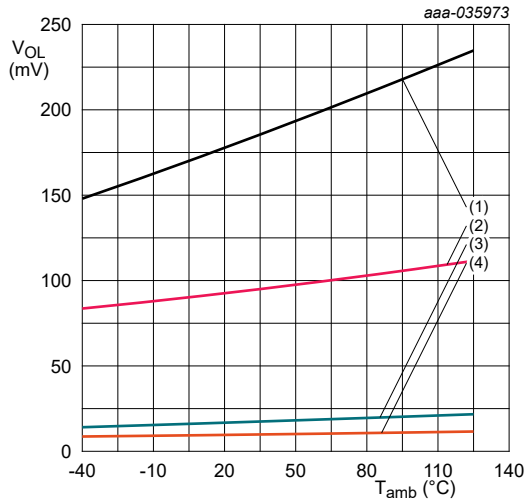
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 85 °C
(4) T_{amb} = 125 °C

Fig. 21. I/O sink current versus LOW-level output voltage



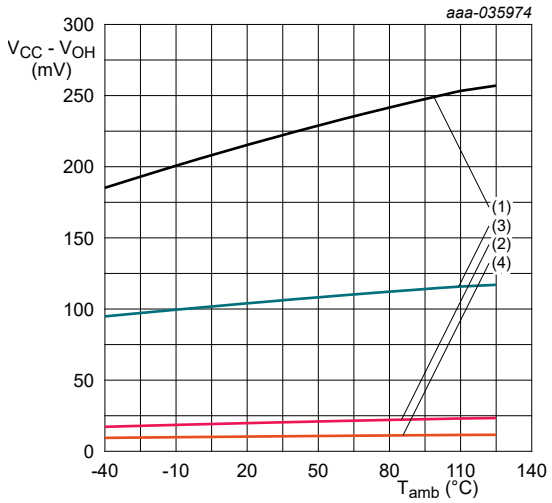
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 85 °C
(4) T_{amb} = 125 °C

Fig. 22. I/O source current versus HIGH-level output voltage



(1) V_{CC} = 1.8 V; I_{sink} = 10 mA
(2) V_{CC} = 5 V; I_{sink} = 10 mA
(3) V_{CC} = 1.8 V; I_{sink} = 1 mA
(4) V_{CC} = 5 V; I_{sink} = 1 mA

Fig. 23. LOW-level output voltage versus temperature



(1) V_{CC} = 1.8 V; I_{source} = -10 mA
(2) V_{CC} = 5 V; I_{source} = -10 mA
(3) V_{CC} = 1.8 V; I_{source} = -1 mA
(4) V_{CC} = 5 V; I_{source} = -1 mA

Fig. 24. I/O high voltage versus temperature

13. Dynamic characteristics

Table 17. I²C-bus interface timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Fig. 25.

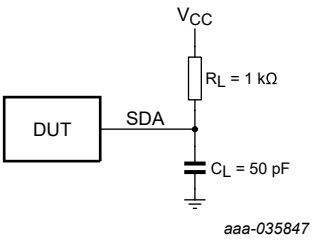
Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{HIGH}	HIGH period of the SCL clock		4	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
t_r	rise time of both SDA and SCL signals		-	1000	20	300	ns
t_f	fall time of both SDA and SCL signals		-	300	20 × (V_{CC}/ 5.5 V)	300	ns
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4	-	0.6	-	µs
$t_{VD;DAT}$	data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	µs

Table 18. Switching characteristics

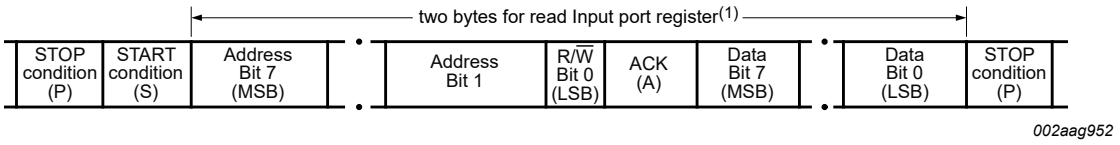
Over recommended operating free air temperature range; $C_L \leq 100$ pF; unless otherwise specified. See Fig. 26.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
$t_{v(INT)}$	valid time on pin $\overline{INT}$	from P port to $\overline{INT}$	-	1	-	1	µs
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	1	-	1	µs
$t_{v(Q)}$	data output valid time	from SCL to P port	-	300	-	300	ns
$t_{su(D)}$	data input set-up time	from P port to SCL	-50	-	-50	-	ns
$t_{h(D)}$	data input hold time	from P port to SCL	240	-	240	-	ns

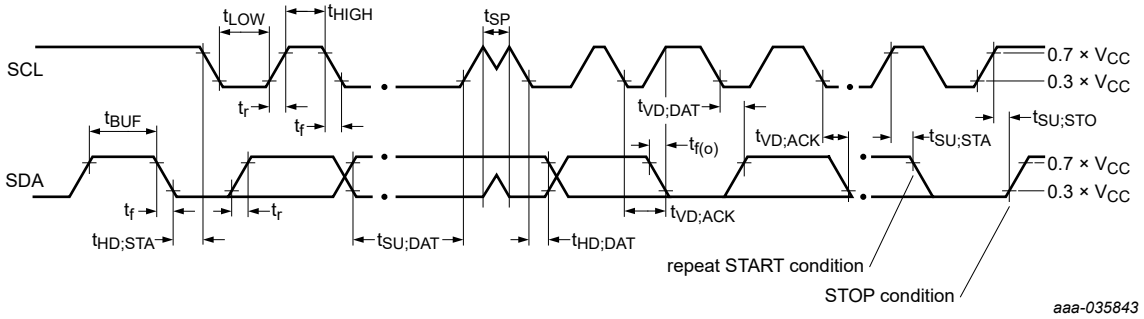
14. Parameter measurement information



a. SDA load configuration



b. Transaction format

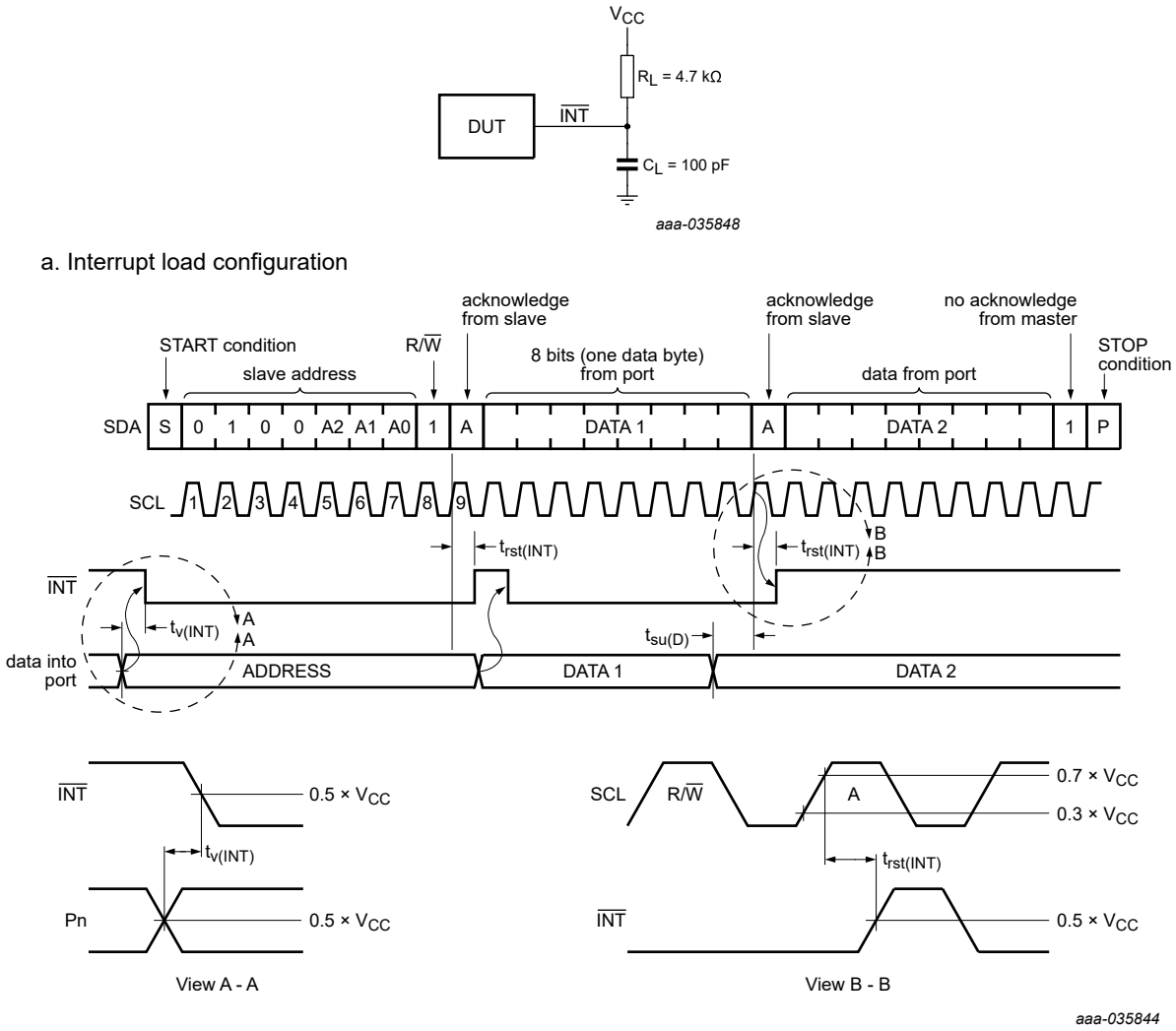


c. Voltage waveforms

C_L includes probe and jig capacitance.
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; $t_r/t_f \leq 30$ ns.
All parameters and waveforms are not applicable to all devices.
Byte 1 = I²C-bus address; Byte 2, byte 3 = P port data.

(1) See Fig. 9.

Fig. 25. I²C-bus interface load circuit and voltage waveforms



a. Interrupt load configuration

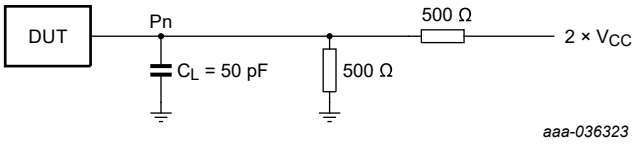
b. Voltage waveforms

C_L includes probe and jig capacitance.

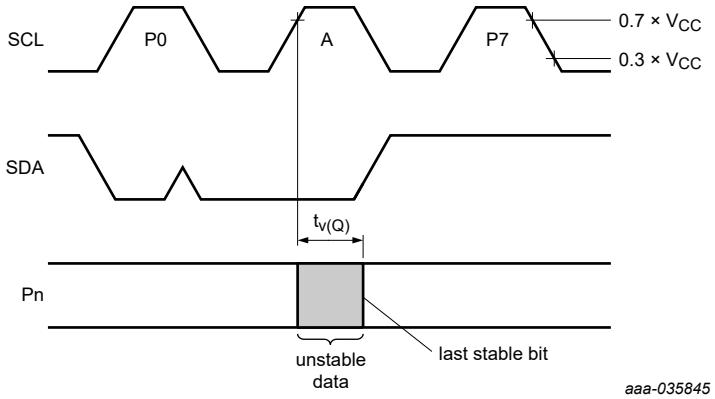
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

All parameters and waveforms are not applicable to all devices.

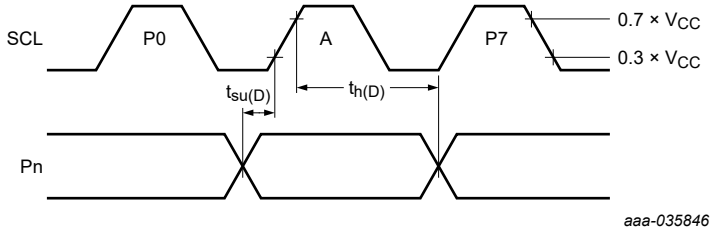
Fig. 26. Interrupt load circuit and voltage waveforms



a. P port load configuration



b. Write mode (R/$\overline{W}$ = 0)



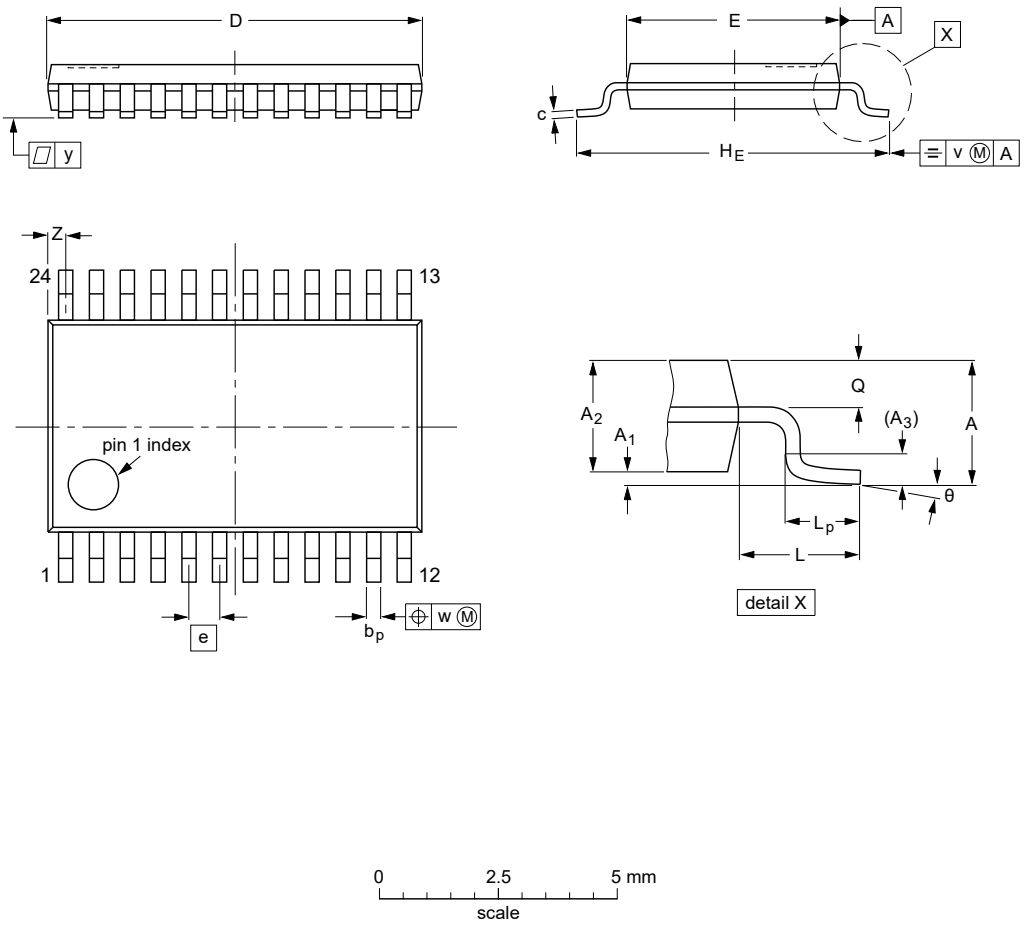
c. Read mode (R/$\overline{W}$ = 1)

C_L includes probe and jig capacitance.
$t_{v(Q)}$ is measured from 0.7 × V_{CC} on SCL to 50 % I/O (Pn) output.
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.
The outputs are measured one at a time, with one transition per measurement.
All parameters and waveforms are not applicable to all devices.

Fig. 27. P port load circuit and voltage waveforms

15. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 28. Package outline SOT355-1 (TSSOP24)

16. Abbreviations

Table 19. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CBT	Cross-Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
FF	Flip-Flop
GPIO	General Purpose Input/Output
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light Emitting Diode
SMBus	System Management Bus

17. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NCA9535_Q100 v.1	20230331	Product data sheet	-	-

18. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This Nexperia product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 31 March 2023

单击下面可查看定价，库存，交付和生命周期等信息

>>Nexperia(安世)