

# 74ABT162245A; 74ABTH162245A

16-bit bus transceiver with 30  $\Omega$  series termination resistors; 3-state

Rev. 7 — 24 June 2024

**Product data sheet** 

### 1. General description

The 74ABT162245A; 74ABTH162245A is a 16-bit transceiver with 30  $\Omega$  termination resistors and 3-state outputs. The device can be used as two 8-bit transceivers or one 16-bit transceiver. The device features two output enables ( $\overline{10E}$  and  $\overline{20E}$ ) each controlling eight outputs, and two send/receive (1DIR and 2DIR) inputs for direction control. A HIGH on  $\overline{n0E}$  causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

Two options are available, 74ABT162245A which does not have the bus hold feature and the 74ABTH162245A which incorporates the bus hold feature.

### 2. Features and benefits

- · 16-bit bidirectional bus interface
- Multiple V<sub>CC</sub> and GND pins minimize switching noise
- 3-state buffers
- Output capability: +12 mA/–32 mA
- 74ABTH162245A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Integrated 30 Ω termination resistors
- Supply voltage range from 4.5 to 5.5 V
- · BiCMOS high speed and output drive
- · Direct interface with TTL levels
- Power-up 3-state
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

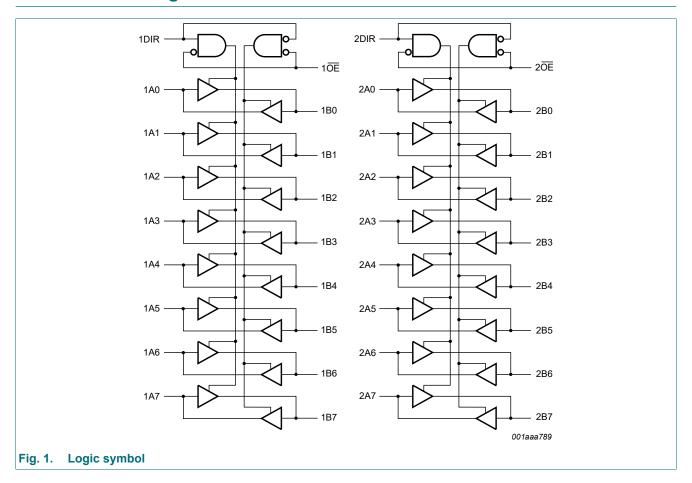
## 3. Ordering information

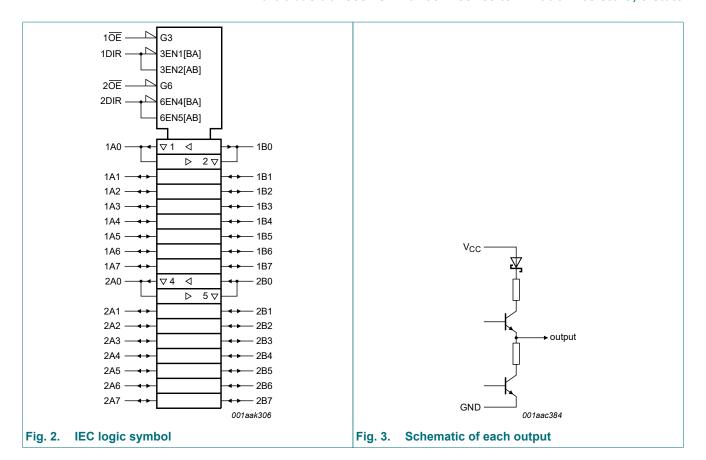
#### **Table 1. Ordering information**

Type number	Package								
	Temperature range	Name	Description	Version					
74ABT162245ADGG 74ABTH162245ADGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1					



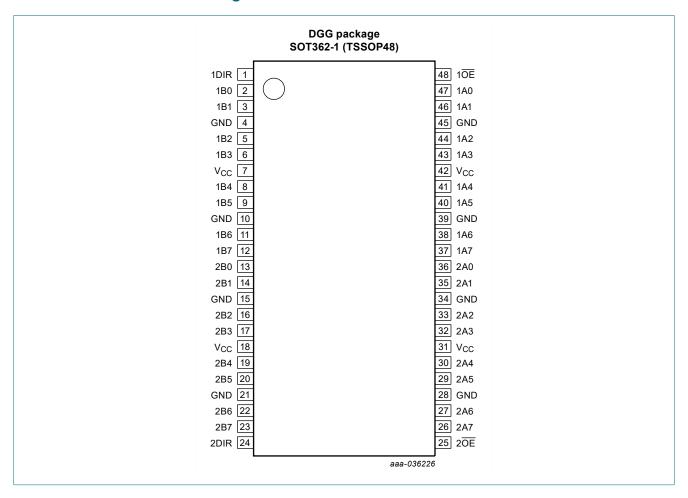
## 4. Functional diagram





## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control input
1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7	13, 14, 16, 17, 19, 20, 22, 23	data input/output
1 <del>OE</del> , 2 <del>OE</del>	48, 25	output enable input
V <sub>CC</sub>	7, 18, 31, 42	supply voltage

## 6. Functional description

#### Table 3. Function table

 $H = HIGH \text{ voltage level}; L = LOW \text{ voltage level}; X = don't care; Z = high-impedance OFF-state.}$ 

Control		Input/output			
n <del>OE</del> nDIR n		nAn	nBn		
L	L	output nAn = nBn	input		
L	Н	input	output nBn = nAn		
Н	X	Z	Z		

## 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7.0	V
VI	input voltage		[1]	-1.2	+7.0	V
Vo	output voltage	output in OFF-state or HIGH-state	[1]	-0.5	+5.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V		-18	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V		-50	-	mA
Io	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-64	-	mA
Tj	junction temperature		[2]	-	150	°C
T <sub>stg</sub>	storage temperature			-65	+150	°C

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 8. Recommended operating conditions

#### **Table 5. Operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		4.5	-	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	V
I <sub>OH</sub>	HIGH-level output current		-32	-	-	mA
I <sub>OL</sub>	LOW-level output current		-	-	12	mA
Δt/ΔV	input transition rise and fall rate		0	-	10	ns/V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C

<sup>[2]</sup> The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 9. Static characteristics

#### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions			25 °C		-40 °C t	o +85 °C	Unit
				Min	Тур	Max	Min	Max	
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-1.2	-0.9	-	-1.2	-	V	
V <sub>IH</sub>	HIGH-level input voltage			2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage			-	-	0.8	-	8.0	V
V <sub>OH</sub>	HIGH-level output voltage	$V_{CC}$ = 4.5 V; $I_{OH}$ = -3 mA; $V_I$ = $V_{IL}$ or $V_{IH}$		2.5	2.9	-	2.5	-	V
		$V_{CC}$ = 5.0 V; $I_{OH}$ = -3 mA; $V_I$ = $V_{IL}$ or $V_{IH}$		3.0	3.4	-	3.0	-	V
		V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = -32 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		2.0	2.4	-	2.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 4.5 V; I <sub>OL</sub> = 8 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		-	0.46	0.65	-	0.65	V
		$V_{CC}$ = 4.5 V; $I_{OL}$ = 12 mA; $V_I$ = $V_{IL}$ or $V_{IH}$		-	0.5	0.8	-	0.8	V
lı	input leakage current	$\overline{OE}$ , nDIR; $V_{CC}$ = 5.5 V; $V_I$ = GND or 5.5 V			±0.01	±1	-	±1	μΑ
I <sub>OFF</sub>	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$		-	±5.0	±100	-	±100	μA
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0.8 V	[1]	50	-	-	50	-	μΑ
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = 2.0 V	[1]	-75	-	-	-75	-	μΑ
I <sub>BHLO</sub>	bus hold LOW overdrive current	$V_{CC} = 5.5 \text{ V}; V_I = 0 \text{ V to } 5.5 \text{ V}$	[1] [2]	500	-	-	-	-	μA
I <sub>внно</sub>	bus hold HIGH overdrive current	$V_{CC} = 5.5 \text{ V}; V_I = 0 \text{ V to } 5.5 \text{ V}$	[1] [2]	-500	-	-	-	-	μΑ
I <sub>O(pu/pd)</sub>	power-up/power-down output current	$V_{CC}$ = 2.0 V; $V_{O}$ = 0.5 V; $V_{I}$ = GND or $V_{CC}$ ; $n\overline{OE}$ = don't care	[3]	-	±5.0	±50	-	±50	μΑ
l <sub>OZ</sub>	OFF-state output	$V_{CC}$ = 5.5 V; $V_I$ = $V_{IL}$ or $V_{IH}$							
	current	V <sub>O</sub> = 5.5 V		-	0.5	10	-	10	μΑ
		V <sub>O</sub> = 0.0 V		-	-0.5	-10	-	-10	μΑ
I <sub>CEX</sub>	output high leakage current	$V_{CC} = 5.5 \text{ V}; V_{O} = 5.5 \text{ V};$ $V_{I} = \text{GND or } V_{CC}$		-	5.0	50	-	50	μΑ
lo	output current	$V_{CC} = 5.5 \text{ V}; V_{O} = 2.5 \text{ V}$	[4]	-50	-92	-180	-50	-180	mA
I <sub>CC</sub>	supply current	$V_{CC}$ = 5.5 V; $V_I$ = GND or $V_{CC}$							
		outputs HIGH		-	0.3	0.7	-	0.7	mA
		outputs LOW		-	10	19	-	19	mA
		outputs 3-state		-	0.3	0.7	-	0.7	mA

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	Unit
			Min	Тур	Max	Min	Max	
ΔI <sub>CC</sub> additional supply current		per input pin; $V_{CC} = 5.5 \text{ V}$ ; [5] one input at 3.4 V, other inputs at $V_{CC}$ or GND						
		outputs enabled	-	400	700	-	700	μΑ
		74ABT162245A; outputs 3-state	-	1.0	50	-	50	μΑ
		74ABTH162245A; outputs 3-state	-	100	250	-	250	μΑ
		nOE, nDIR	-	400	700	-	700	μΑ
Cı	input capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>	-	3	-	-	-	pF
C <sub>I/O</sub>	input/output capacitance	$V_O = 0 \text{ V or } V_{CC}$ ; outputs 3-state	-	7	-	-	-	pF

- [1] Valid for data inputs of bus hold parts only (74ABTH162245A)
- [2] This is the bus hold overdrive current required to force the input to the opposite logic state.
- [3] This parameter is valid for any  $V_{CC}$  between 0 V and 2.1 V with a transition time of up to 10 ms. From  $V_{CC}$  = 2.1 V to  $V_{CC}$  = 4.5 V to 5.5 V a transition time of 100  $\mu$ s is permitted.
- [4] Not more than one output should be tested at a time and the duration of the test should not exceed one second
- [5] This is the increase in supply current for each input at 3.4 V.

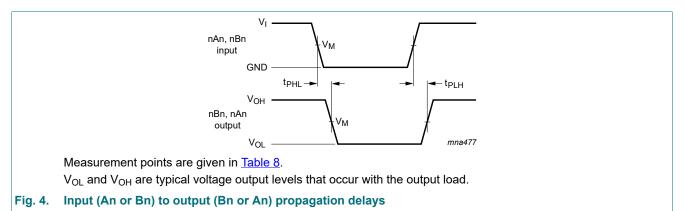
## 10. Dynamic characteristics

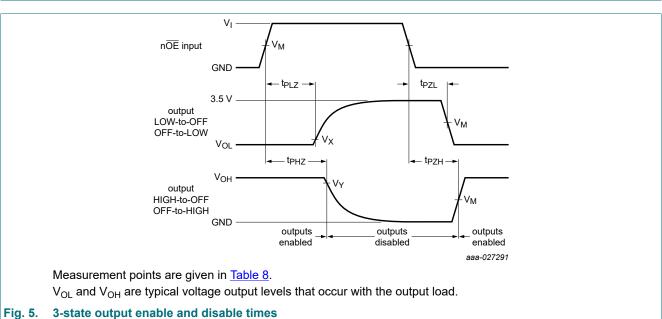
#### **Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C; V <sub>CC</sub> = 5.0 V							Unit
			Min	Тур	Max	Min	Max			
t <sub>PLH</sub>	LOW to HIGH propagation delay	nAn to nBn or nBn to nAn; see Fig. 4	1.0	2.0	3.3	1.0	3.5	ns		
t <sub>PHL</sub>	HIGH to LOW propagation delay	nAn to nBn or nBn to nAn; see Fig. 4	1.5	3.0	4.5	1.5	4.9	ns		
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	nOE to nAn or nBn; see Fig. 5	1.5	3.1	4.3	1.5	5.0	ns		
t <sub>PZL</sub>	OFF-state to LOW propagation delay	nOE to nAn or nBn; see Fig. 5	2.0	5.0	6.1	2.0	7.0	ns		
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	nOE to nAn or nBn; see Fig. 5	1.7	3.5	4.8	1.7	5.4	ns		
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	nOE to nAn or nBn; see Fig. 5	1.5	3.2	4.5	1.5	4.9	ns		

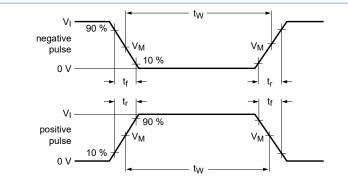
#### 10.1. Waveforms and test circuit

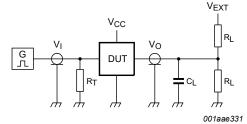




**Table 8. Measurement points** 

Input		Output		
V <sub>I</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
3.0 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V





Test data is given in Table 9.

Definitions test circuit:

R<sub>L</sub> = Load resistance;

C<sub>L</sub> = Load capacitance including jig and probe capacitance;

R<sub>T</sub> = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator;

 $V_{EXT}$  = Test voltage for switching times.

Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Input	put			Load V <sub>EXT</sub>				
VI	fi	t <sub>W</sub>	t <sub>r</sub> , t <sub>f</sub>	CL	$R_L$	t <sub>PHZ</sub> , t <sub>PZH</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>
3.0 V	≤ 1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	7 V	open

## 11. Package outline

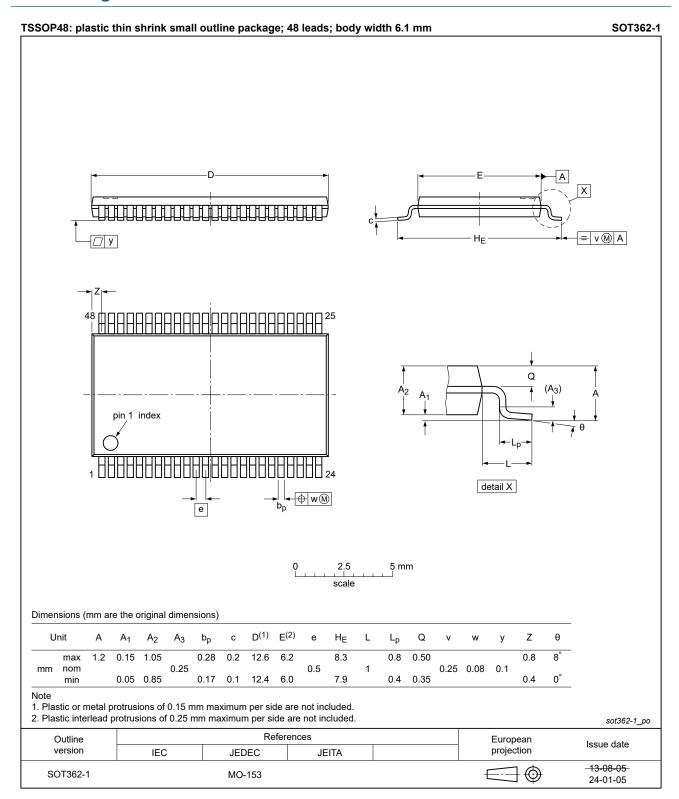


Fig. 7. Package outline SOT362-1 (TSSOP48)

74ABT\_ABTH162245A

## 12. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description			
ANSI	American National Standards Institute			
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor			
CDM	Charged Device Model			
DUT	Device Under Test			
ESD	ElectroStatic Discharge			
ESDA	ElectroStatic Discharge Association			
НВМ	Human Body Model			
JEDEC	Joint Electron Device Engineering Council			

## 13. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74ABT_ABTH162245A v.7	20240624	Product data sheet	-	74ABT_ABTH162245A v.6				
Modifications:	<u>Section 2</u> : ESD specification updated according to the latest JEDEC standard.							
74ABT_ABTH162245A v.6	20240222	Product data sheet	-	74ABT_ABTH162245A v.5				
Modifications:	• <u>Fig. 7</u> : Upda	ated package outline drawi	ng SOT362-1 (TS	SOP48).				
74ABT_ABTH162245A v.5	20210702	Product data sheet	-	74ABT_H162245A v.4				
Modifications:		er 74ABT162245ADL (SOT and <u>Section 2</u> updated.	370-1 / SSOP48)	removed.				
74ABT_H162245A v.4	20190220	Product data sheet	-	74ABT_H162245A v.3				
Modifications:	Type number	er 74ABTH162245ADL (SC	T370-1) removed	1.				
74ABT_H162245A v.3	20170831	Product data sheet	-	74ABT_H162245A v.2				
Modifications:	guidelines o	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>						
74ABT_H162245A v.2	19980225	Product specification	-	74ABT_H162245A v.1				
74ABT_H162245A v.1	19961120	Product specification	-	-				

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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