74HC173-Q100; 74HCT173-Q100

Quad D-type flip-flop; positive-edge trigger; 3-state

Rev. 1 — 15 January 2024 Product data sheet

1. General description

The 74HC173-Q100; 74HCT173-Q100 is a quad positive-edge triggered D-type flip-flop. The device features clock (CP), master reset (MR), two input enable ($\overline{E}1$, $\overline{E}2$) and two output enable ($\overline{OE}1$, $\overline{OE}2$) inputs. When the input enables are LOW, the outputs Qn will assume the state of their corresponding Dn inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on either input enable will cause the device to go into a hold mode, outputs hold their previous state independently of clock and data inputs. A HIGH on MR forces the outputs LOW independently of clock and data inputs. A HIGH on either output enable pin causes the outputs to assume a high-impedance OFF-state. Operation of the output enable inputs does not affect the state of the flip-flops. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Complies with JEDEC standard no. 7A
- Input levels:
  - For 74HC173-Q100: CMOS level
  - For 74HCT173-Q100: TTL level
- Gated input enable for hold (do nothing) mode
- Gated output enable control mode
- Edge-triggered D-type register
- Asynchronous master reset
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC173D-Q100 74HCT173D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

nexperia

4. Functional diagram

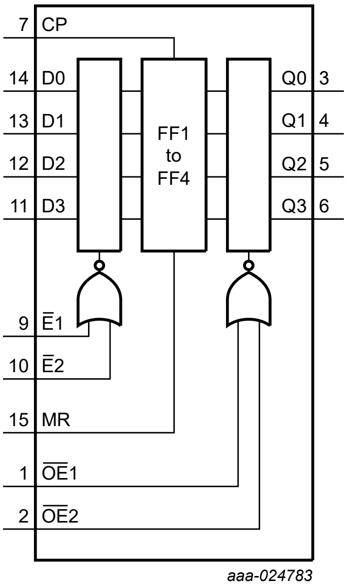


Fig. 1. Functional diagram

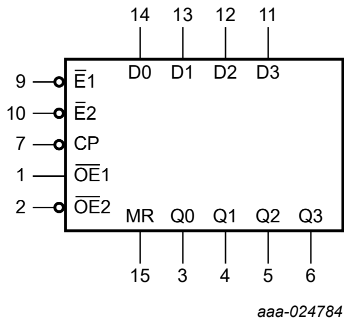


Fig. 2. Logic symbol

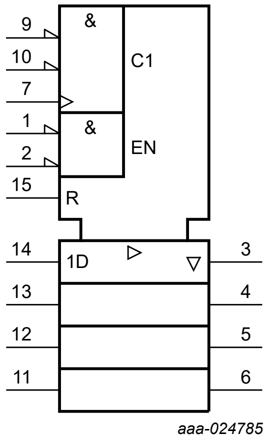


Fig. 3. IEC logic symbol

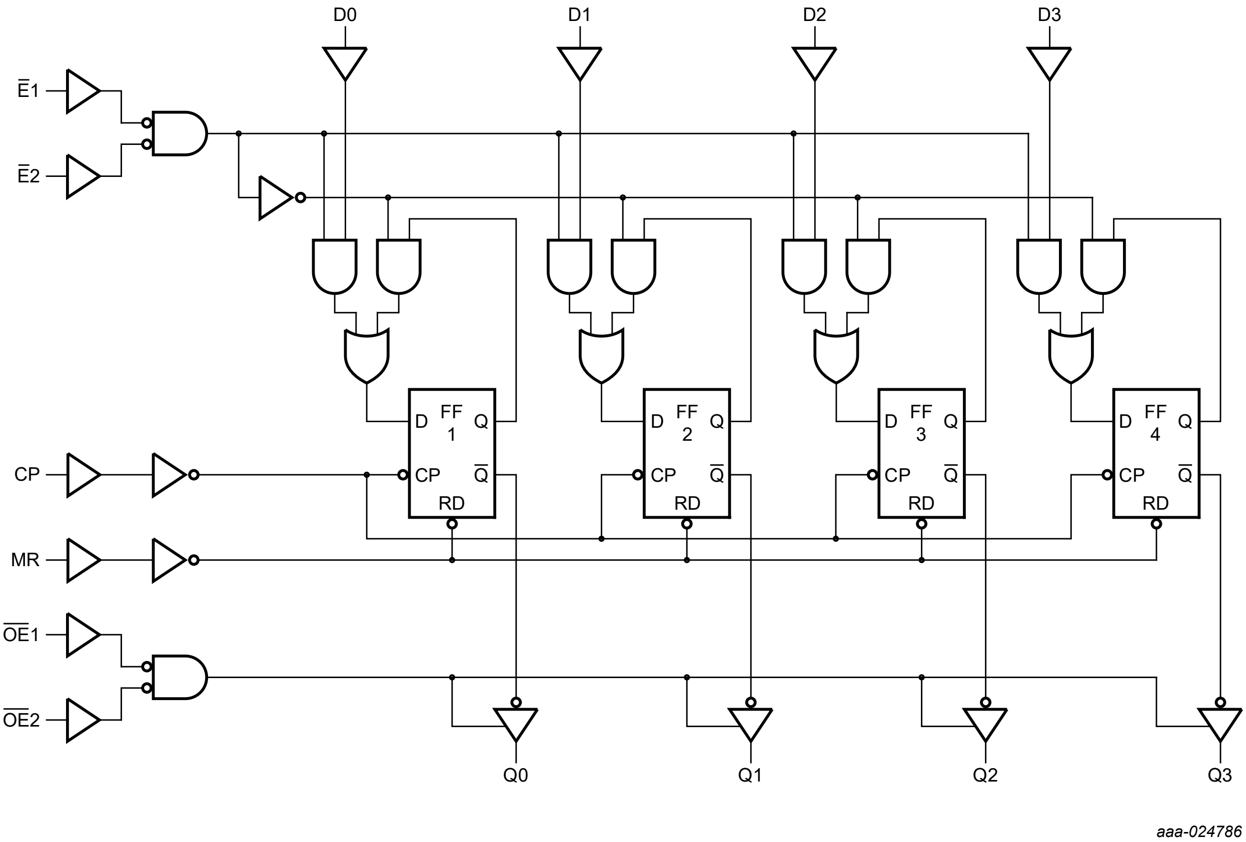
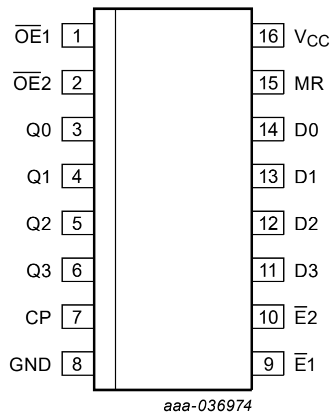


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning

D package
SOT109-1 (SO16)



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$1, $\overline{OE}$2	1, 2	output enable input (active LOW)
Q0, Q1, Q2, Q3	3, 4, 5, 6	3-state flip-flop output
CP	7	clock input (LOW-to-HIGH, edge triggered)
GND	8	ground (0 V)
$\overline{E}$1, $\overline{E}$2	9, 10	data enable input (active LOW)
D0, D1, D2, D3	14, 13, 12, 11	data input
MR	15	asynchronous master reset (active HIGH)
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;

q_n = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition; X = don't care; ↑ = LOW-to-HIGH clock transition.

Register operating mode	Inputs					Outputs
	MR	CP	$\overline{E}$1	$\overline{E}$2	Dn	Qn (register)
Reset (clear)	H	X	X	X	X	L
Parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (do nothing)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance OFF-state.

3-state buffer operating mode	Inputs			Outputs			
	Qn (register)	$\overline{OE}1$	$\overline{OE}2$	Q0	Q1	Q2	Q3
Read	L	L	L	L	L	L	L
	H	L	L	H	H	H	H
Disabled	X	H	X	Z	Z	Z	Z
	X	X	H	Z	Z	Z	Z

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±35	mA
I_{CC}	supply current		-	+70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[1]	-	500	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC173-Q100			74HCT173-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5$ V	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC173-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_{CC} = 6.0 V; V_O = V_{CC} or GND	-	-	±0.5	-	±5.0	-	±10	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT173-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -6.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		$\overline{OE}1$, $\overline{OE}2$	-	50	180	-	225	-	245	μA
		MR	-	60	216	-	270	-	294	μA
		$\overline{E}1$, $\overline{E}2$	-	40	144	-	180	-	196	μA
		Dn	-	25	90	-	112.5	-	122.5	μA
		CP	-	100	360	-	450	-	490	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 9.

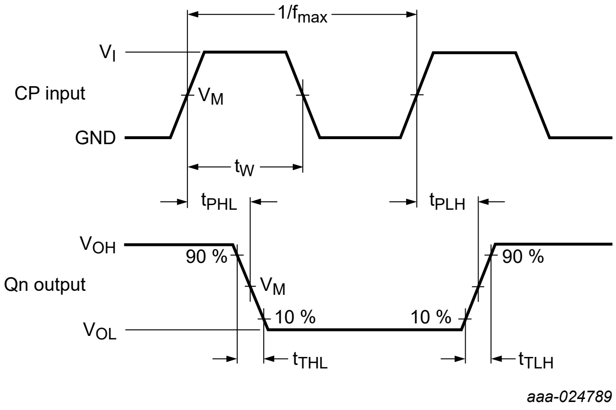
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC173-Q100										
t_{pd}	propagation delay	CP to Qn; see Fig. 5 [1]								
		V_{CC} = 2.0 V	-	55	175	-	220	-	265	ns
		V_{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	16	30	-	37	-	45	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 6								
		V_{CC} = 2.0 V	-	44	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	16	30	-	38	-	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	13	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	13	26	-	33	-	38	ns
t_{en}	enable time	$\overline{OE}$n to Qn; see Fig. 7 [2]								
		V_{CC} = 2.0 V	-	52	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	19	30	-	38	-	45	ns
		V_{CC} = 6.0 V	-	15	26	-	33	-	38	ns
t_{dis}	disable time	$\overline{OE}$n to Qn; see Fig. 7 [3]								
		V_{CC} = 2.0 V	-	52	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	19	30	-	38	-	45	ns
		V_{CC} = 6.0 V	-	15	26	-	33	-	38	ns
t_t	transition time	see Fig. 5 [4]								
		V_{CC} = 2.0 V	-	14	60	-	75	-	90	ns
		V_{CC} = 4.5 V	-	5	12	-	15	-	18	ns
		V_{CC} = 6.0 V	-	4	10	-	13	-	15	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 5								
		V_{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	4	-	17	-	20	-	ns
		MR HIGH; see Fig. 6								
		V_{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	4	-	17	-	20	-	ns
t_{rec}	recovery time	MR to CP; see Fig. 6								
		V_{CC} = 2.0 V	60	-8	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	-3	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	-2	-	13	-	15	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	$\overline{En}$ to CP; see Fig. 8								
		V_{CC} = 2.0 V	100	33	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	12	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	10	-	21	-	26	-	ns
		Dn to CP; see Fig. 8								
		V_{CC} = 2.0 V	60	17	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	6	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	5	-	13	-	15	-	ns
t_h	hold time	$\overline{En}$ to CP; see Fig. 8								
		V_{CC} = 2.0 V	0	-17	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	-6	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	-5	-	0	-	0	-	ns
		Dn to CP; see Fig. 8								
		V_{CC} = 2.0 V	1	-11	-	1	-	1	-	ns
		V_{CC} = 4.5 V	1	-4	-	1	-	1	-	ns
		V_{CC} = 6.0 V	1	-3	-	1	-	1	-	ns
f_{max}	maximum frequency	CP; see Fig. 5								
		V_{CC} = 2.0 V	6	26	-	4.8	-	4	-	MHz
		V_{CC} = 4.5 V	30	80	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	88	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	95	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; f_i = 1 MHz [5]	-	20	-	-	-	-	-	pF

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
74HCT173-Q100											
t_{pd}	propagation delay	CP to Qn; see Fig. 5	[1]								
		V_{CC} = 4.5 V		-	20	40	-	50	-	60	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	17	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 6									
		V_{CC} = 4.5 V		-	20	37	-	46	-	56	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	17	-	-	-	-	-	ns
t_{en}	enable time	$\overline{OE}$n to Qn; V_{CC} = 4.5 V; see Fig. 7	[2]	-	20	35	-	44	-	53	ns
t_{dis}	disable time	$\overline{OE}$n to Qn; V_{CC} = 4.5 V; see Fig. 7	[3]	-	19	30	-	38	-	45	ns
t_t	transition time	V_{CC} = 4.5 V; see Fig. 5	[4]	-	5	12	-	15	-	19	ns
t_W	pulse width	CP HIGH or LOW; V_{CC} = 4.5 V; see Fig. 5		16	7	-	20	-	24	-	ns
		MR HIGH; V_{CC} = 4.5 V; see Fig. 6		15	6	-	19	-	22	-	ns
t_{rec}	recovery time	MR to CP; V_{CC} = 4.5 V; see Fig. 6		12	-2	-	15	-	18	-	ns
t_{su}	set-up time	$\overline{E}$n to CP; V_{CC} = 4.5 V; see Fig. 8		22	13	-	28	-	33	-	ns
		Dn to CP; V_{CC} = 4.5 V; see Fig. 8		12	7	-	15	-	18	-	ns
t_h	hold time	$\overline{E}$n to CP; V_{CC} = 4.5 V; see Fig. 8		0	-6	-	0	-	0	-	ns
		Dn to CP; V_{CC} = 4.5 V; see Fig. 8		0	-3	-	0	-	0	-	ns
f_{max}	maximum frequency	CP; see Fig. 5									
		V_{CC} = 4.5 V		30	80	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF		-	88	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} - 1.5 V; V_{CC} = 5 V; f_i = 1 MHz	[5]	-	20	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_{en} is the same as t_{PZH} and t_{PZL}.
[3] t_{dis} is the same as t_{PHZ} and t_{PLZ}.
[4] t_t is the same as t_{THL} and t_{TLH}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

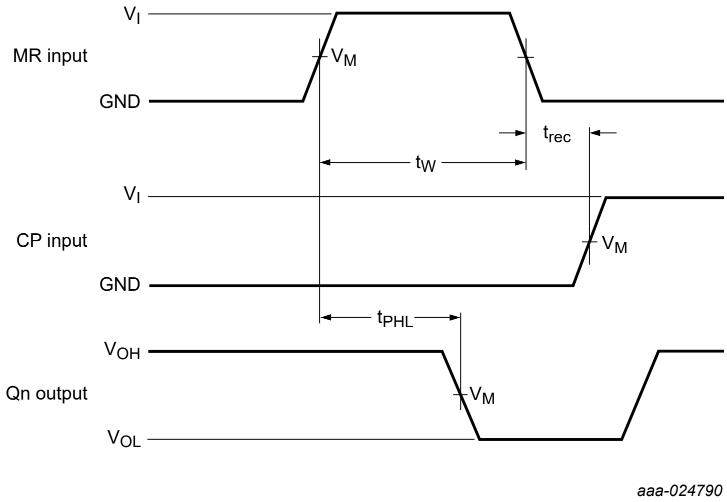
10.1. Waveforms and test circuit



Measurement points are given in Table 9.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

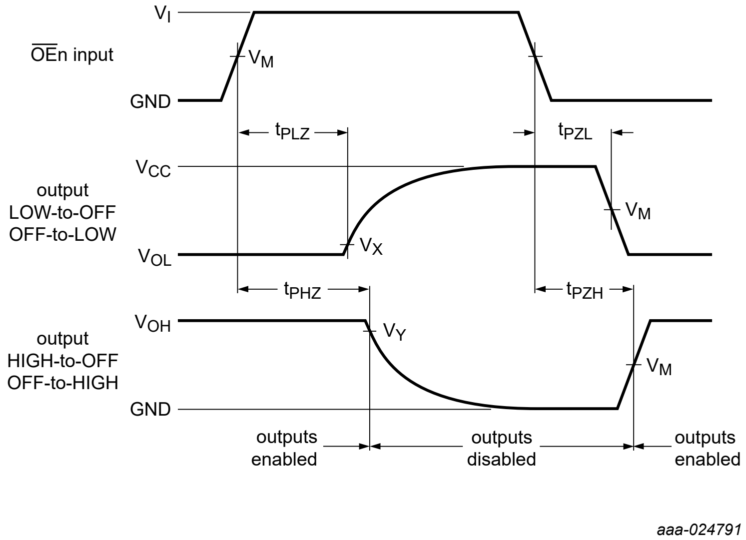
Fig. 5. The clock (CP) to outputs (Qn) propagation delays, clock pulse width, output transition times and maximum frequency



Measurement points are given in Table 9.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

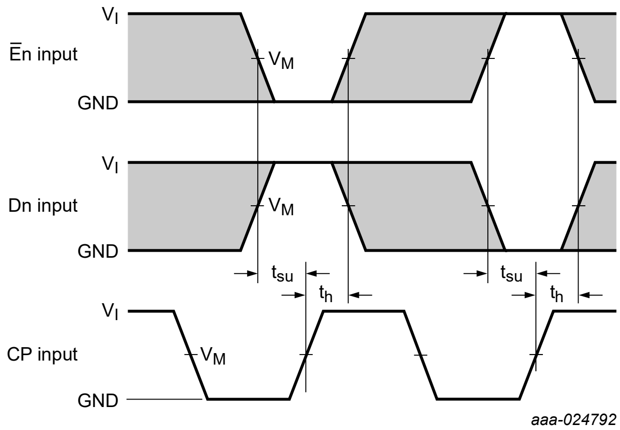
Fig. 6. The master reset (MR) pulse width, master reset to output (Qn) propagation delays, and the master reset to clock (CP) recovery times



Measurement points are given in Table 9.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. 3-state enable and disable times



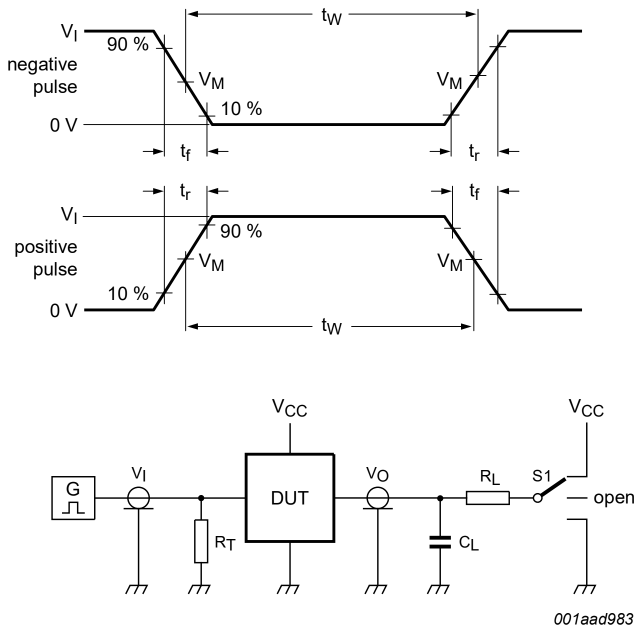
The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 9.

Fig. 8. The data set-up and hold times from input (Ēn, Dn) to clock (CP)

Table 9. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC173-Q100	0.5 × V_{CC}	0.5 × V_{CC}	0.1 × V_{CC}	0.9 × V_{CC}
74HCT173-Q100	1.3 V	1.3 V	0.1 × V_{CC}	0.9 × V_{CC}



Test data is given in Table 10.
Test circuit definitions:
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator
C_L = Load capacitance including jig and probe capacitance
R_L = Load resistance.
S1 = Test selection switch

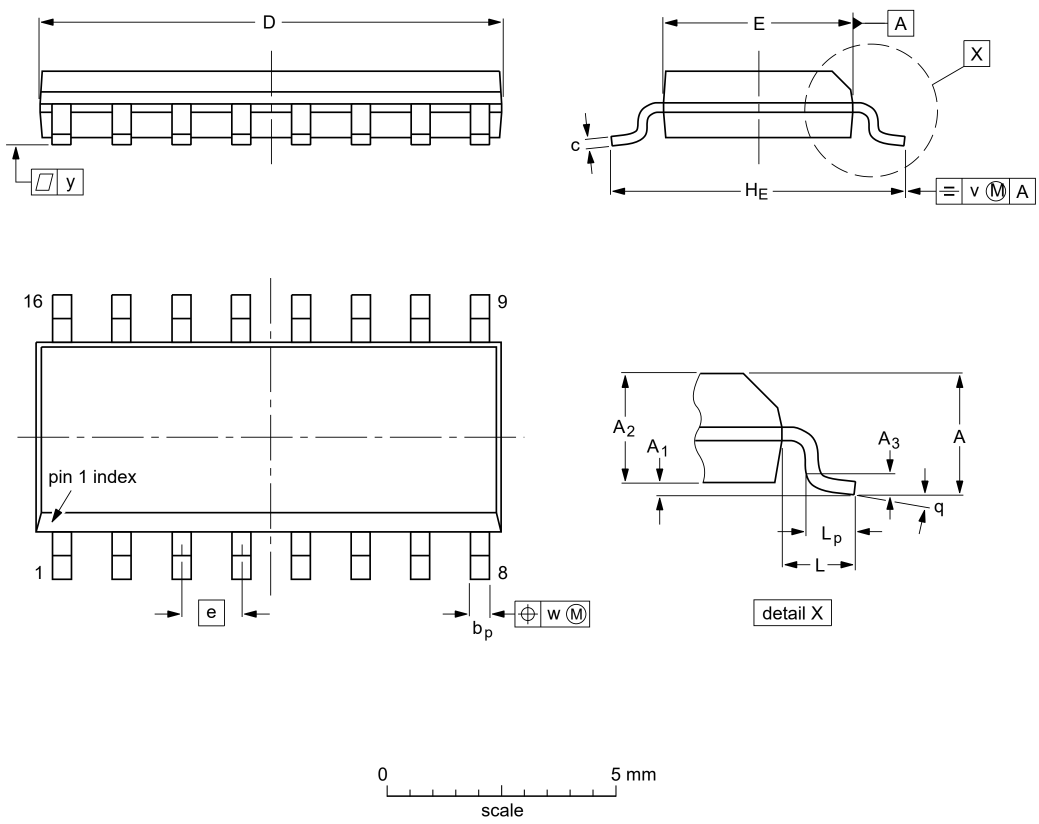
Fig. 9. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC173-Q100	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT173-Q100	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 10. Package outline SOT109-1 (SO16)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT173_Q100 v.1	20240115	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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