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Kind regards,

Team Nexperia



# BSS84 P-channel enhancement mode vertical DMOS transistor Rev. 06 – 16 December 2008 Product data sheet

# 1. Product profile

#### 1.1 General description

P-channel enhancement mode vertical Diffusion Metal-Oxide Semiconductor (DMOS) transistor in a small Surface-Mounted Device (SMD) plastic package.

#### Table 1. Product overview

Type number <sup>[1]</sup>	Package	
	NXP	JEDEC
BSS84	SOT23	TO-236AB
BSS84/DG		

[1] /DG: halogen-free

#### 1.2 Features

 Low threshold voltage
 Direct interface to CMOS and Transistor-Transistor Logic (TTL)
 High-speed switching
 No secondary breakdown

#### **1.3 Applications**

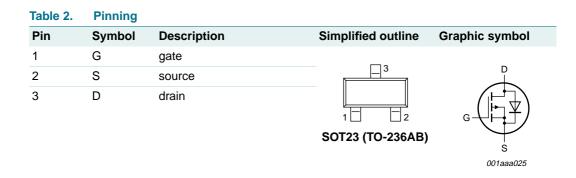
Line current interrupter in telephone sets Relay, high-speed and line transformer drivers

#### 1.4 Quick reference data

- V<sub>DS</sub>  $\leq$  -50 V R<sub>DSon</sub>  $\leq$  10 Ω
- $I_D \le -130 \text{ mA}$ ■  $P_{tot} \le 250 \text{ mW}$



# 2. Pinning information



# 3. Ordering information

Type number <sup>[1]</sup>	Package	age			
	Name	Description	Version		
BSS84	TO-236AB	plastic surface-mounted package; 3 leads	SOT23		
BSS84/DG					

[1] /DG: halogen-free

# 4. Marking

Table 4. Marking codes	
Type number <sup>[1]</sup>	Marking code <sup>[2]</sup>
BSS84	13*
BSS84/DG	ZV*

[1] /DG: halogen-free

[2] \* = -: made in Hong Kong

\* = p: made in Hong Kong\* = t: made in Malaysia

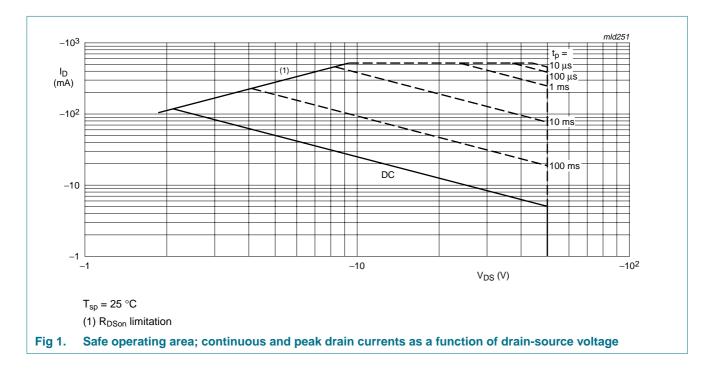
\* = W: made in China

2 of 11

# 5. Limiting values

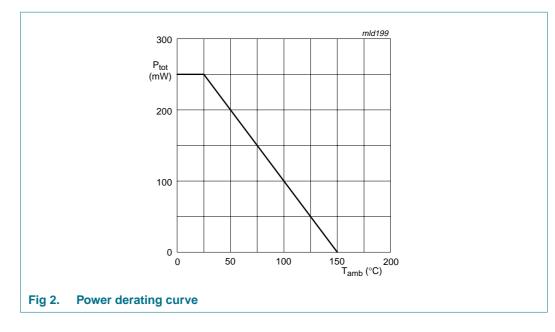
Table 5. In accorda	Limiting values ance with the Absolute Ma.	ximum Rating System (IEC 6	0134).		
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C $\leq$ T <sub>j</sub> $\leq$ 150 °C	-	-50	V
V <sub>GS</sub>	gate-source voltage		-	±20	V
I <sub>D</sub>	drain current	$T_{sp} = 25 \text{ °C}; V_{GS} = -10 \text{ V};$ see Figure 1	-	-130	mA
		T <sub>sp</sub> = 100 °C; V <sub>GS</sub> = -10 V	-	-75	mA
I <sub>DM</sub>	peak drain current	$T_{sp}$ = 25 °C; $t_p \le 10 \ \mu s$ ; see <u>Figure 1</u>	-	-520	mA
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C; see Figure 2	<u>[1]</u> _	250	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
Ti	junction temperature		-65	+150	°C

[1] Device mounted on a Printed-Circuit Board (PCB).



# **BSS84**

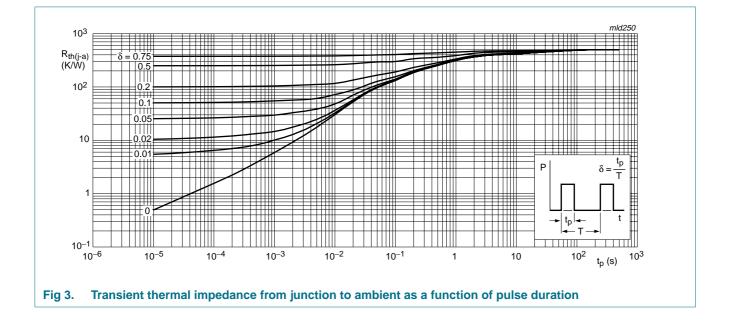
#### P-channel enhancement mode vertical DMOS transistor



### 6. Thermal characteristics

Table 6.	Thermal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	see Figure 3	<u>[1]</u> -	-	500	K/W

[1] Mounted on a PCB, vertical in still air.

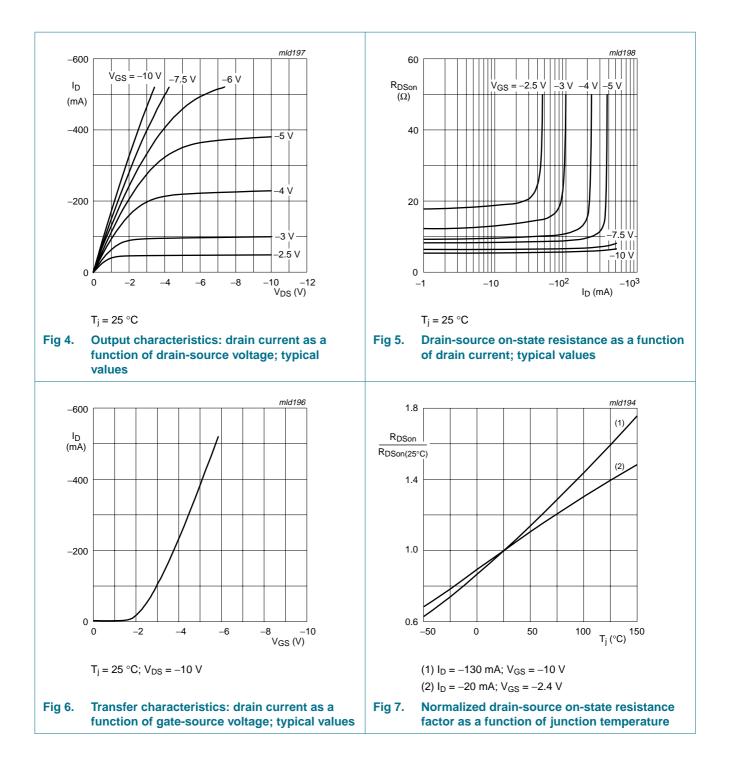


# 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	$I_D = -10 \ \mu A; \ V_{GS} = 0 \ V$	-50	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = -1 \text{ mA}; V_{DS} = V_{GS};$ see <u>Figure 8</u>				
		T <sub>j</sub> = 25 °C	-0.8	-	-2	V
		T <sub>j</sub> = −55 °C	-	-	-1.8	V
I <sub>DSS</sub>	drain leakage current	$V_{DS}$ = -40 V; $V_{GS}$ = 0 V				
		T <sub>j</sub> = 25 °C	-	-	-100	nA
		$V_{DS} = -50 \text{ V};  V_{GS} = 0 \text{ V}$				
		T <sub>j</sub> = 25 °C	-	-	-10	μΑ
		T <sub>j</sub> = 125 °C	-	-	-60	μΑ
I <sub>GSS</sub>	gate leakage current	$V_{GS}$ = +20 V; $V_{DS}$ = 0 V	-	-	100	nA
		$V_{GS} = -20 \text{ V};  V_{DS} = 0 \text{ V}$	-	-	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = -10 \text{ V};$ $I_D = -130 \text{ mA};$ see Figure 5 and 7	-	6	10	Ω
Dynamic o	characteristics					
Y <sub>fs</sub>	transfer admittance	$V_{DS} = -25 V;$ $I_{D} = -130 mA$	50	-	-	mS
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 V; V_{DS} = -25 V;$	-	25	45	pF
C <sub>oss</sub>	output capacitance	f = 1 MHz; see <u>Figure 9</u>	-	15	25	pF
C <sub>rss</sub>	reverse transfer capacitance		-	3.5	12	pF
t <sub>on</sub>	turn-on time	$V_{DS} = -40 \text{ V}; V_{GS} = 0 \text{ V}$ to -10 V; I <sub>D</sub> = -200 mA; see <u>Figure 10</u> and <u>11</u>	-	3	-	ns
t <sub>off</sub>	turn-off time	$V_{DS} = -40 \text{ V};$ $V_{GS} = -10 \text{ V to 0 V};$ $I_D = -200 \text{ mA};$ see Figure 10 and 11	-	7	-	ns

# **BSS84**

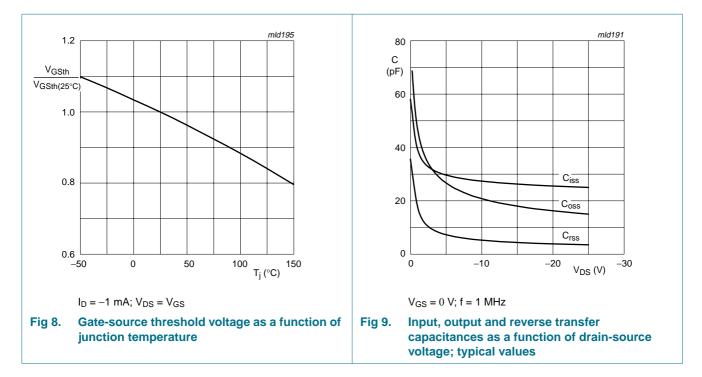
#### P-channel enhancement mode vertical DMOS transistor



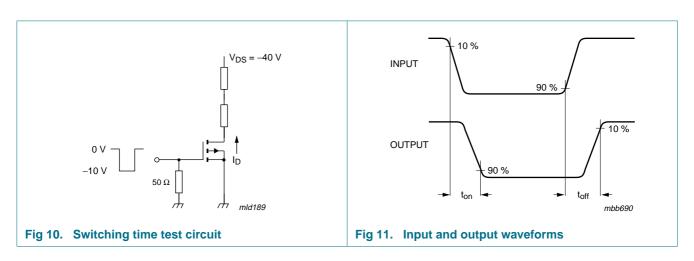
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#### P-channel enhancement mode vertical DMOS transistor

**BSS84** 



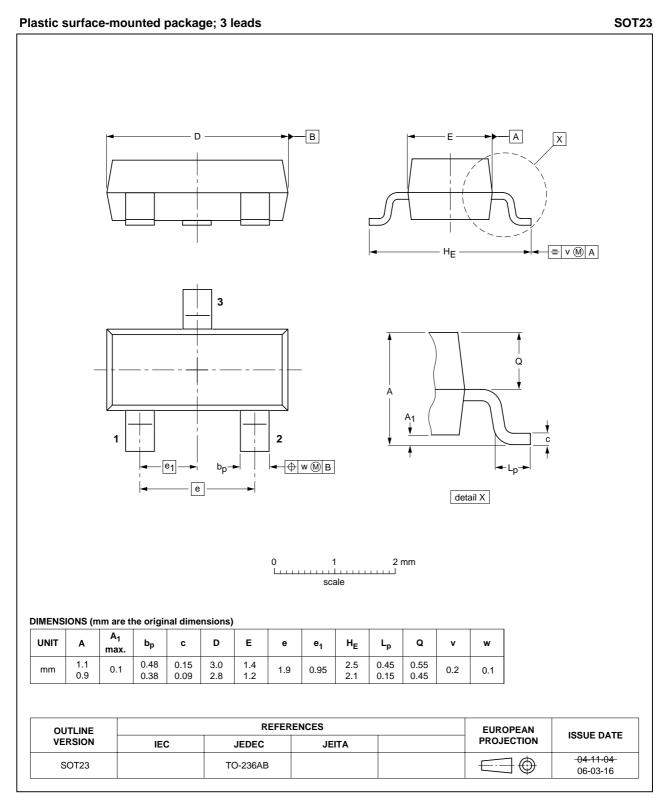
### 8. Test information



BSS84 6

**BSS84** 

### 9. Package outline



#### Fig 12. Package outline SOT23 (TO-236AB)

BSS84\_6 Product data sheet

# 10. Revision history

Table 8. Revision	history			
Document ID	Release date	Data sheet status	Change notice	Supersedes
BSS84_6	20081216	Product data sheet	-	BSS84_5
Modifications:	• Table 5 "Lim	niting values": P <sub>tot</sub> figure ref	erence updated	
BSS84_5	20081209	Product data sheet	-	BSS84_4
BSS84_4	20070717	Product data sheet	-	BSS84_3
BSS84_3	20030804	Product specification	-	BSS84_2
BSS84_2	19970618	Product specification	-	BSS84_1
BSS84_1	19950407	Product specification	-	-

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#### 11.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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10 of 11

# **BSS84**

#### P-channel enhancement mode vertical DMOS transistor

### 13. Contents

1	Product profile 1
1.1	General description
1.2	Features 1
1.3	Applications 1
1.4	Quick reference data 1
2	Pinning information 2
3	Ordering information 2
4	Marking 2
5	Limiting values 3
6	Thermal characteristics 4
7	Characteristics 5
8	Test information 7
9	Package outline 8
10	Revision history 9
11	Legal information 10
11.1	Data sheet status 10
11.2	Definitions 10
11.3	Disclaimers 10
11.4	Trademarks 10
12	Contact information 10
13	Contents 11



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