

1. General description

The 74HC107-Q100; 74HCT107-Q100 is a dual negative edge triggered JK flip-flop featuring individual J and K inputs, clock (\overline{CP}) and reset (\overline{R}) inputs and complementary Q and \overline{Q} outputs. The reset is an asynchronous active LOW input and operates independently of the clock input. The J and K inputs control the state changes of the flip-flops as described in the mode select function table. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC107-Q100: CMOS level
 - For 74HCT107-Q100: TTL level
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

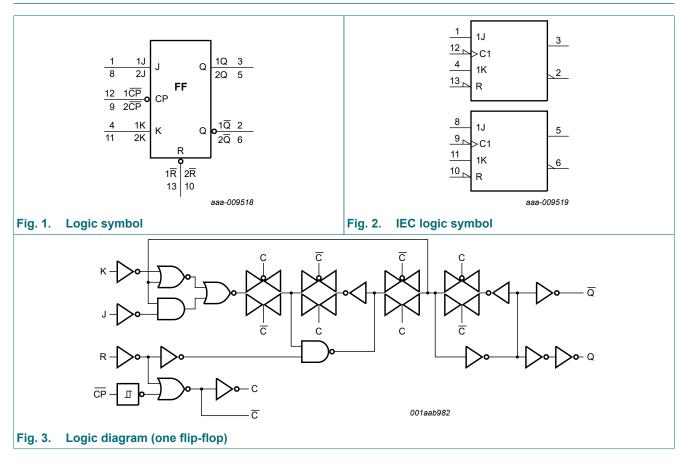
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC107D-Q100 74HCT107D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<u>SOT108-1</u>
74HC107PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<u>SOT402-1</u>

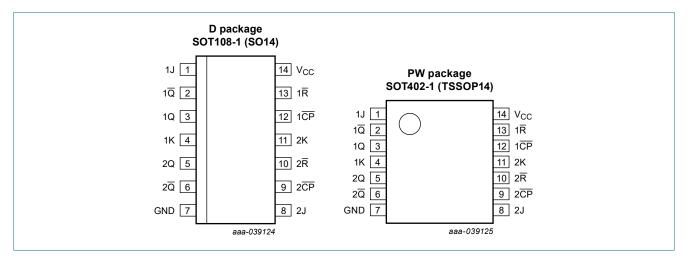
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4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description	1	
Symbol	Pin	Description
1J, 2J	1, 8	synchronous J input
1 <u>Q</u> , 2 <u>Q</u>	2, 6	complement output
1Q, 2Q	3, 5	true output
1K, 2K	4, 11	synchronous K input
1 <u>CP</u> , 2 <u>CP</u>	12, 9	clock input (HIGH-to-LOW edge-triggered)
1R, 2R	13, 10	asynchronous reset input (active LOW)
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;

L = LOW voltage level; I = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;

q = state of referenced output one set-up time prior to the HIGH-to-LOW clock transition; X = don't care;

 \downarrow = HIGH-to-LOW clock transition.

Input				Output		Operating mode
R	CP	J	к	Q	Q	
L	Х	X	X	L	Н	asynchronous reset
Н	Ļ	h	h	q	q	toggle
Н	Ļ	1	h	L	Н	load 0 (reset)
Н	Ļ	h	I	н	L	load 1 (set)
Н	Ļ	I	I	q	q	hold (no change)

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7.0	V
I _{IK}	input clamping current	V_{I} < -0.5 V or V_{I} > V_{CC} + 0.5 V	[1]	-	±20	mA
I _{OK}	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V	[1]	-	±20	mA
lo	output current	V_{O} = -0.5 V to V_{CC} + 0.5 V		-	±25	mA
I _{CC}	supply current			-	50	mA
I _{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: Ptot derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC107-Q100			74H	2100	Unit	
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

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9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	1
74HC10	7-Q100								1	1
VIH	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l _l	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	4.0	-	40	-	80	μA
CI	input capacitance		-	3.5	-					pF
74HCT1	07-Q100	1	1		1				1	-
V _{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								<u> </u>
	output voltage	I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
II	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA

Dual JK flip-flop with reset; negative-edge trigger

Symbol	Parameter	Conditions	25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit	
			Min	Тур	Max	Min	Max	Min	Мах	
ΔI _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 V$; $I_O = 0 A$; other inputs at V_{CC} or GND; $V_{CC} = 4.5 V$ to 5.5 V								
		pin n CP , nJ	-	100	360	-	450	-	490	μA
		pin nR	-	65	234	-	293	-	319	μA
		pin nK	-	60	216	-	270	-	294	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 6

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Тур	Мах	Min	Max	Min	Max	
74HC10	7-Q100									
t _{pd}	propagation	nCP to nQ; see Fig. 4 [1]								
	delay	V _{CC} = 2.0 V	-	52	160	-	200	-	240	ns
		V _{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	16	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	15	27	-	34	-	41	ns
		$n\overline{CP}$ to $n\overline{Q}$; see <u>Fig. 4</u>								
		V _{CC} = 2.0 V	-	52	160	-	200	-	240	ns
		V _{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	16	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	15	27	-	34	-	41	ns
		$n\overline{R}$ to nQ , $n\overline{Q}$; see <u>Fig. 5</u>								
		V _{CC} = 2.0 V	-	52	155	-	195	-	235	ns
		V _{CC} = 4.5 V	-	19	31	-	39	-	47	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	16	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	15	26	-	33	-	40	ns
tt	transition	nQ, nQ; see <u>Fig. 4</u> [2]								
	time	V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns

Dual JK flip-flop with reset; negative-edge trigger

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Тур	Max	Min	Мах	Min	Max	1
t _W	pulse width	n CP input, HIGH or LOW; see <u>Fig. 4</u>								
		V _{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		nR input, HIGH or LOW; see <u>Fig. 5</u>								
		V _{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t _{rec}	recovery	nR to nCP; see <u>Fig. 5</u>								
	time	V _{CC} = 2.0 V	60	19	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	7	-	15	-	18	-	ns
		V _{CC} = 6.0 V	20	6	-	13	-	15	-	ns
t _{su}	set-up time	nJ, nK to nCP; see <u>Fig. 4</u>								
		V _{CC} = 2.0 V	100	22	-	125	-	150	-	ns
		V _{CC} = 4.5 V	20	8	-	25	-	30	-	ns
		V _{CC} = 6.0 V	17	6	-	21	-	26	-	ns
t _h	hold time	nJ, nK to n CP ; see <u>Fig. 4</u>								
		V _{CC} = 2.0 V	3	-6	-	3	_	3	-	ns
		V _{CC} = 4.5 V	3	-2	-	3	-	3	-	ns
		V _{CC} = 6.0 V	3	-2	-	3	_	3	-	ns
f _{max}	maximum	nCP input; see <u>Fig. 4</u>								
	frequency	V _{CC} = 2.0 V	6	23	-	4.8	-	4.0	-	MHz
		V _{CC} = 4.5 V	30	70	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	78	-	-	-	-	-	MHz
		V _{CC} = 6.0 V	35	85	-	28	_	24	-	MHz
C _{PD}	power dissipation capacitance	per flip-flop; [3] $V_I = GND$ to V_{CC}	-	30	-	-	-	-	-	pF
74HCT1	07-Q100									
t _{pd}	propagation	$n\overline{CP}$ to nQ; see <u>Fig. 4</u> [1]								
	delay	V _{CC} = 4.5 V	-	19	36	-	45	-	54	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	16	-	-	-	-	-	ns
		$n\overline{CP}$ to $n\overline{Q}$; see Fig. 4								
		V _{CC} = 4.5 V	-	21	36	-	45	-	54	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	18	-	-	-	-	-	ns
		nR to nQ, nQ; see <u>Fig. 5</u>								
		V _{CC} = 4.5 V	-	20	38	-	48	-	57	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
t _t	transition	nQ, nQ; see <u>Fig. 4</u> [2]								
	time	V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns

Dual JK flip-flop with reset; negative-edge trigger

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	1
t _W	pulse width	nCP input, HIGH or LOW; see Fig. 4								
		V _{CC} = 4.5 V	16	9	-	20	-	24	-	ns
		nR input, HIGH or LOW; see <u>Fig. 5</u>								
		V _{CC} = 4.5 V	20	11	-	25	-	30	-	ns
t _{rec}	recovery	nR to nCP; see <u>Fig. 5</u>								
	time	V _{CC} = 4.5 V	14	8	-	18	-	21	-	ns
t _{su}	set-up time	nJ, nK to nCP; see Fig. 4								
		V _{CC} = 4.5 V	20	7	-	25	-	30	-	ns
t _h	hold time	nJ, nK to nCP; see Fig. 4								
		V _{CC} = 4.5 V	5	-2	-	5	-	5	-	ns
f _{max}	maximum	n CP input; see <u>Fig. 4</u>								
	frequency	V _{CC} = 4.5 V	30	66	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	73	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	per flip-flop; [3] $V_I = GND$ to $V_{CC} - 1.5 V$	-	30	-	-	-	-	-	pF

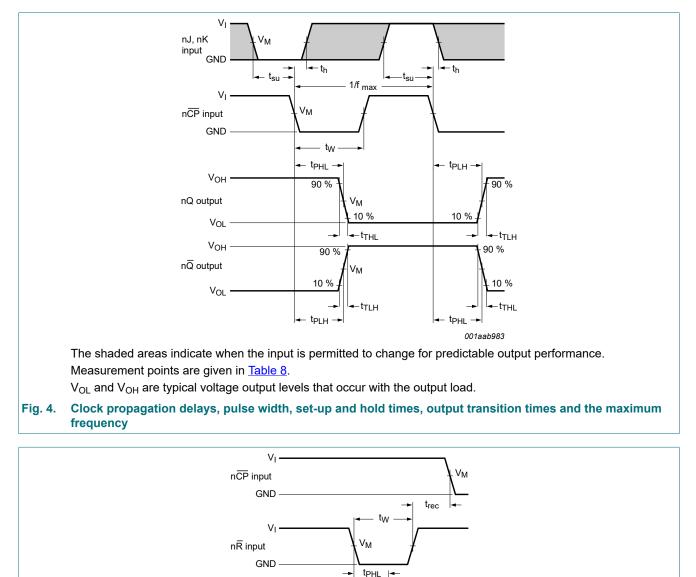
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_0)$ = sum of outputs.



10.1. Waveforms and test circuit

Table 8. Measurement points

Measurement points are given in Table 8.

Туре	Input		Output
	VI	V _M	V _M
74HC107-Q100	V _{CC}	0.5V _{CC}	0.5V _{CC}
74HCT107-Q100	3 V	1.3 V	1.3 V

t_{PLH} →

001aab984

V_{OH} nQ output V_{OL}

V_{OH} nQ output V_{OL}

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Reset propagation delays, pulse width and recovery time

Fig. 5.

Dual JK flip-flop with reset; negative-edge trigger

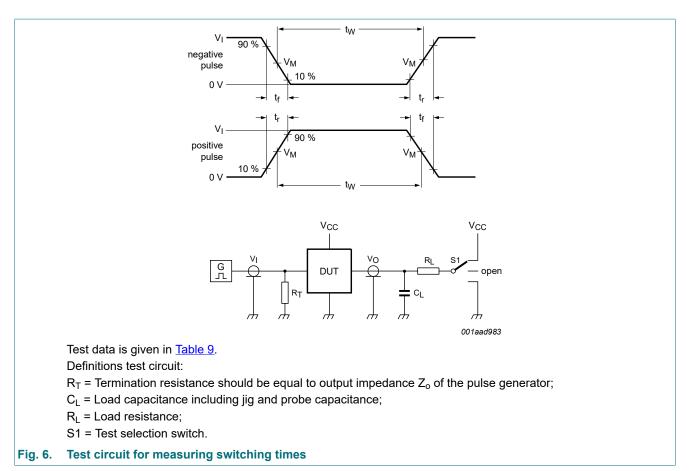


Table 9. Test data

Туре	Input		Load		S1 position			
	VI	t _r , t _f	C _L R _L 1		t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	
74HC107-Q100	V _{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}	
74HCT107-Q100	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}	

11. Package outline

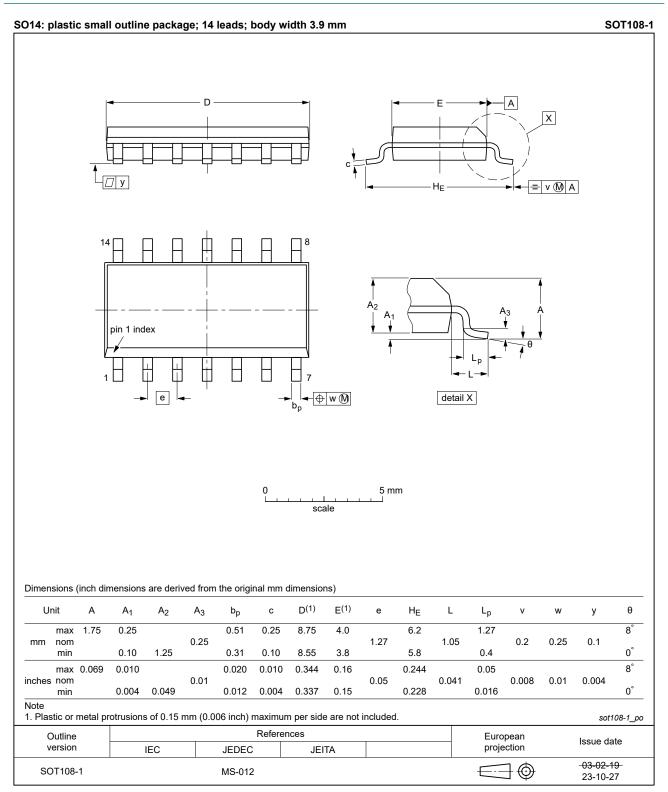


Fig. 7. Package outline SOT108-1 (SO14)

Dual JK flip-flop with reset; negative-edge trigger

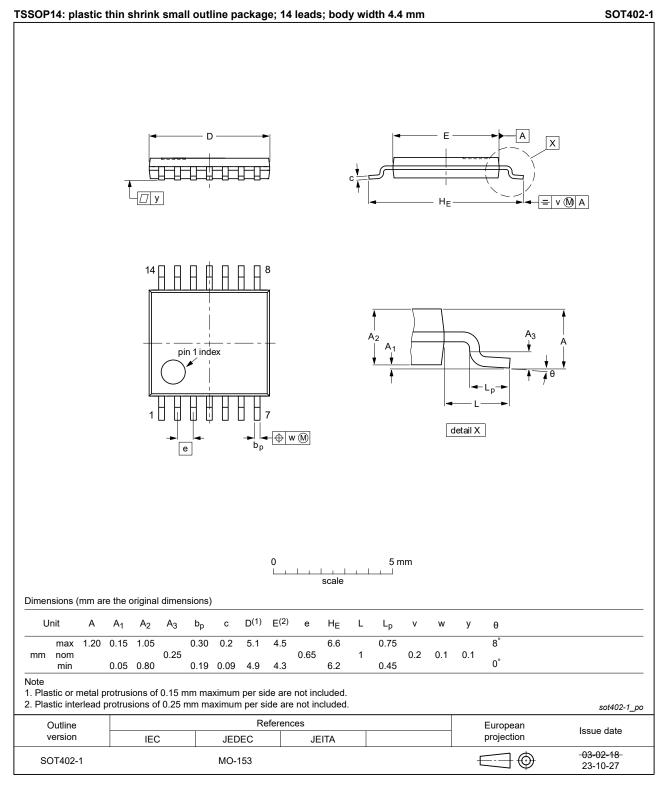


Fig. 8. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 10. Abbreviations			
Acronym	Description		
CDM	Charged Device Model		
CMOS	Complementary Metal-Oxide Semiconductor		
DUT	Device Under Test		
ESD	ElectroStatic Discharge		
НВМ	Human Body Model		
TTL	Transistor-Transistor Logic		

13. Revision history

Table 11. Revision history **Document ID Release date** Data sheet status Change notice Supersedes 74HC_HCT107_Q100 v.4 20240220 Product data sheet 74HC_HCT107_Q100 v.3 Modifications: Section 2: ESD specification updated according to the latest JEDEC standard. • • Fig. 7, Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153 20210707 74HC_HCT107_Q100 v.3 Product data sheet 74HC_HCT107_Q100 v.2 Modifications: • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. • Section 2 updated. <u>Section 7</u>: Derating values for P_{tot} total power dissipation have changed. 74HC_HCT107_Q100 v.2 20150126 Product data sheet 74HC_HCT107_Q100 v.1 Modifications: Table 7: Power dissipation capacitance condition for 74HCT107-Q100 is corrected. 74HC_HCT107_Q100 v.1 Product data sheet 20131118

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <u>https://www.nexperia.com</u>.

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Dual JK flip-flop with reset; negative-edge trigger

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