



PESD5V0X2UM-Q

Ultra low capacitance unidirectional double ESD protection diode

8 August 2023

Product data sheet

1. General description

Ultra low capacitance unidirectional double ElectroStatic Discharge (ESD) protection diode in a DFN1006-3 (SOT883) leadless ultra small Surface-Mounted Device (SMD) plastic package, designed to protect up to two signal lines from the damage caused by ESD and other transients.

2. Features and benefits

- Ultra low diode capacitance: $C_d = 0.50$ pF typ.
- ESD protection up to 10 kV (IEC 61000-4-2; contact discharge)
- $I_{PPM} = 1.5$ A (IEC 61000-4-5; surge)
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- High-speed data lines
- Portable electronics
- Communication systems
- Computers and peripherals

4. Quick reference data

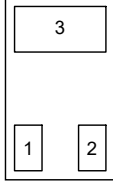
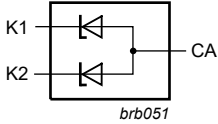
Table 1. Quick reference data

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------|--------------------------|---|-----|-----|-----|------|------|
| V_{RWM} | reverse standoff voltage | $T_{amb} = 25$ °C | [1] | - | - | 5 | V |
| C_d | diode capacitance | $f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C | [1] | - | 0.5 | 0.65 | pF |

[1] Measured from pin 1 or 2 to 3.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------------|---|--|
| 1 | K1 | cathode (diode 1) |  <p>Transparent top view DFN1006-3 (SOT883)</p> |  <p><i>brb051</i></p> |
| 2 | K2 | cathode (diode 2) | | |
| 3 | A | common anode | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|---------------|-----------|---|---------|
| | Name | Description | Version |
| PESD5V0X2UM-Q | DFN1006-3 | plastic, leadless ultra small package; 3 terminals; 0.35 mm pitch; 1 mm x 0.6 mm x 0.48 mm body | SOT883 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|---------------|--------------|
| PESD5V0X2UM-Q | ZH |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|----------------------------|---------------------------------|-----------------------------------|---------|-----|-----|------|
| I_{PPM} | rated peak pulse current | $t_p = 8/20 \mu s$ | [1] [2] | - | 1.5 | A |
| T_j | junction temperature | | | - | 150 | °C |
| T_{amb} | ambient temperature | | | -55 | 150 | °C |
| T_{stg} | storage temperature | | | -65 | 150 | °C |
| ESD maximum ratings | | | | | | |
| V_{ESD} | electrostatic discharge voltage | IEC 61000-4-2 (contact discharge) | [3] [2] | - | 10 | kV |
| | | IEC 61000-4-2 (air discharge) | [3] [2] | - | 15 | kV |
| | | machine model | [2] | - | 400 | V |
| | | MIL-STD-883 (human body model) | | - | 10 | kV |

[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Measured from pin 1 or 2 to 3.

[3] Device stressed with ten non-repetitive ESD pulses.

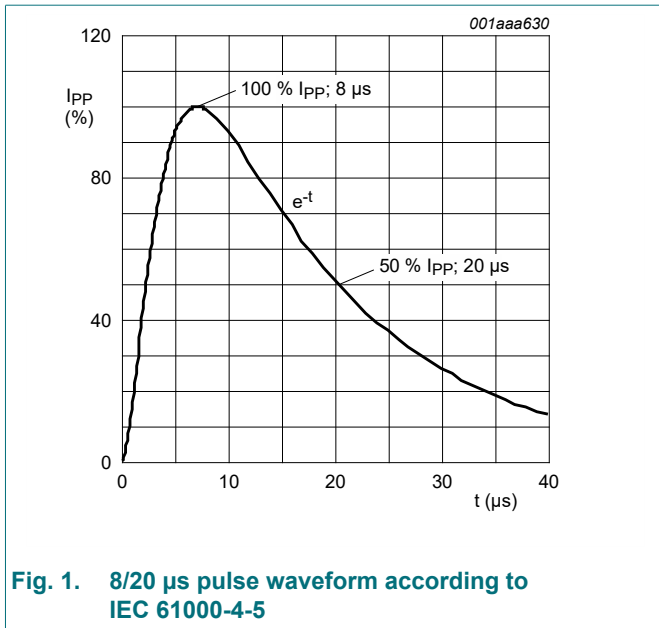


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

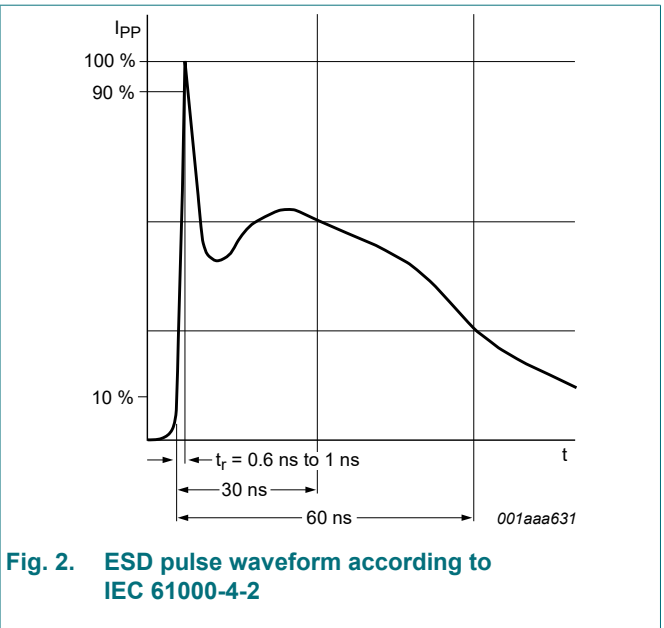


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------|--------------------------|---|---------|-----|-----|------|----------|
| V_{RWM} | reverse standoff voltage | $T_{amb} = 25\text{ }^{\circ}\text{C}$ | [1] | - | - | 5 | V |
| V_{BR} | breakdown voltage | $I_R = 10\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | [1] | 7.5 | 8.8 | 10 | V |
| I_{RM} | reverse leakage current | $V_R = 5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | [1] | - | 1 | 10 | nA |
| C_d | diode capacitance | $f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | [1] | - | 0.5 | 0.65 | pF |
| V_{CL} | clamping voltage | $I_{PP} = 1\text{ A}; t_p = 8/20\text{ }\mu\text{s}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | [2] [1] | - | - | 13 | V |
| | | $I_{PPM} = 1.5\text{ A}; t_p = 8/20\text{ }\mu\text{s}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | [2] [1] | - | - | 14 | V |
| R_{dyn} | dynamic resistance | $I_R = 10\text{ A}; t_p = 100\text{ ns}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | [3] [1] | - | 0.9 | - | Ω |

- [1] Measured from pin 1 or 2 to 3.
- [2] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.
- [3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.1-2008.

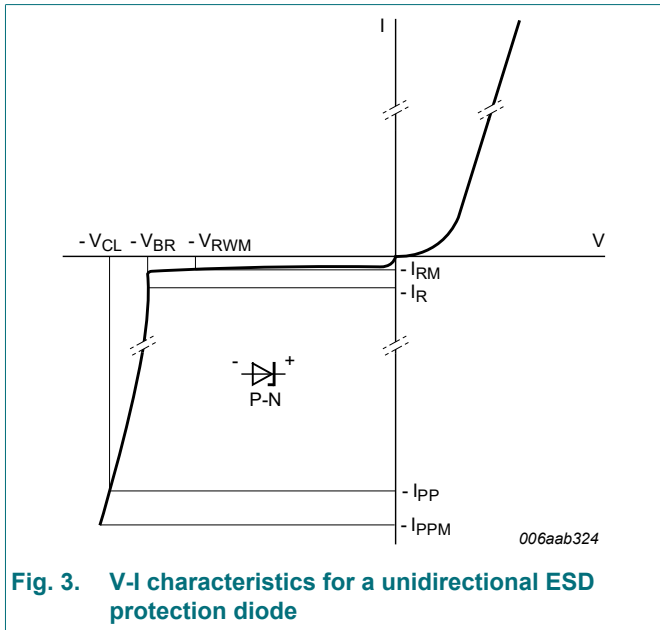


Fig. 3. V-I characteristics for a unidirectional ESD protection diode

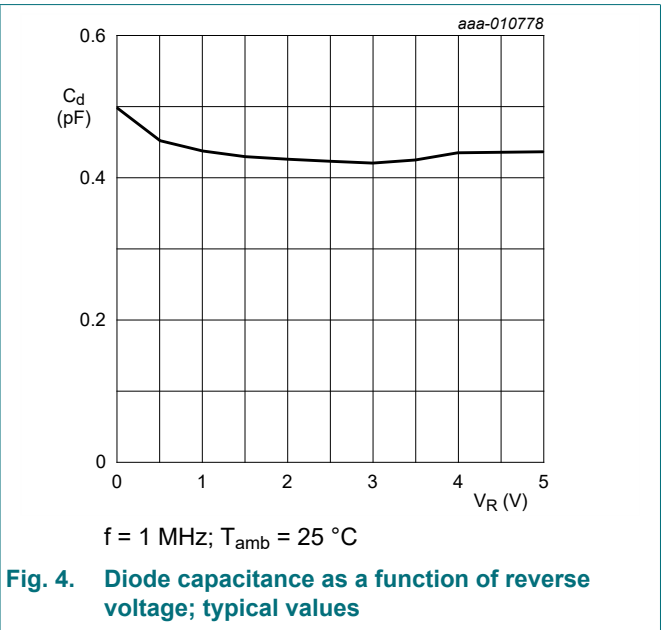
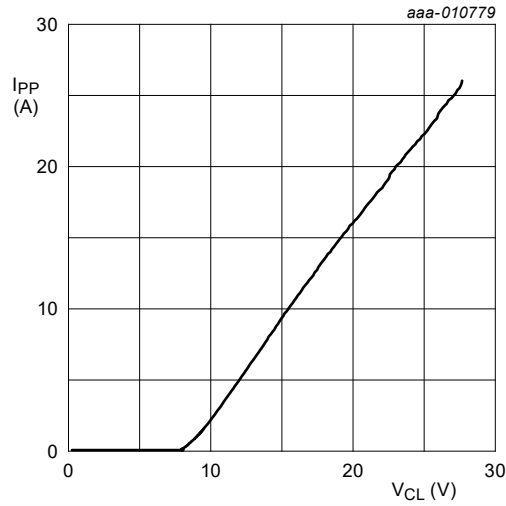


Fig. 4. Diode capacitance as a function of reverse voltage; typical values



Transmission Line Pulse (TLP);
 $t_p = 100$ ns; $t_r = 1$ ns

Fig. 5. Dynamic resistance with positive clamping; typical values

Ultra low capacitance unidirectional double ESD protection diode

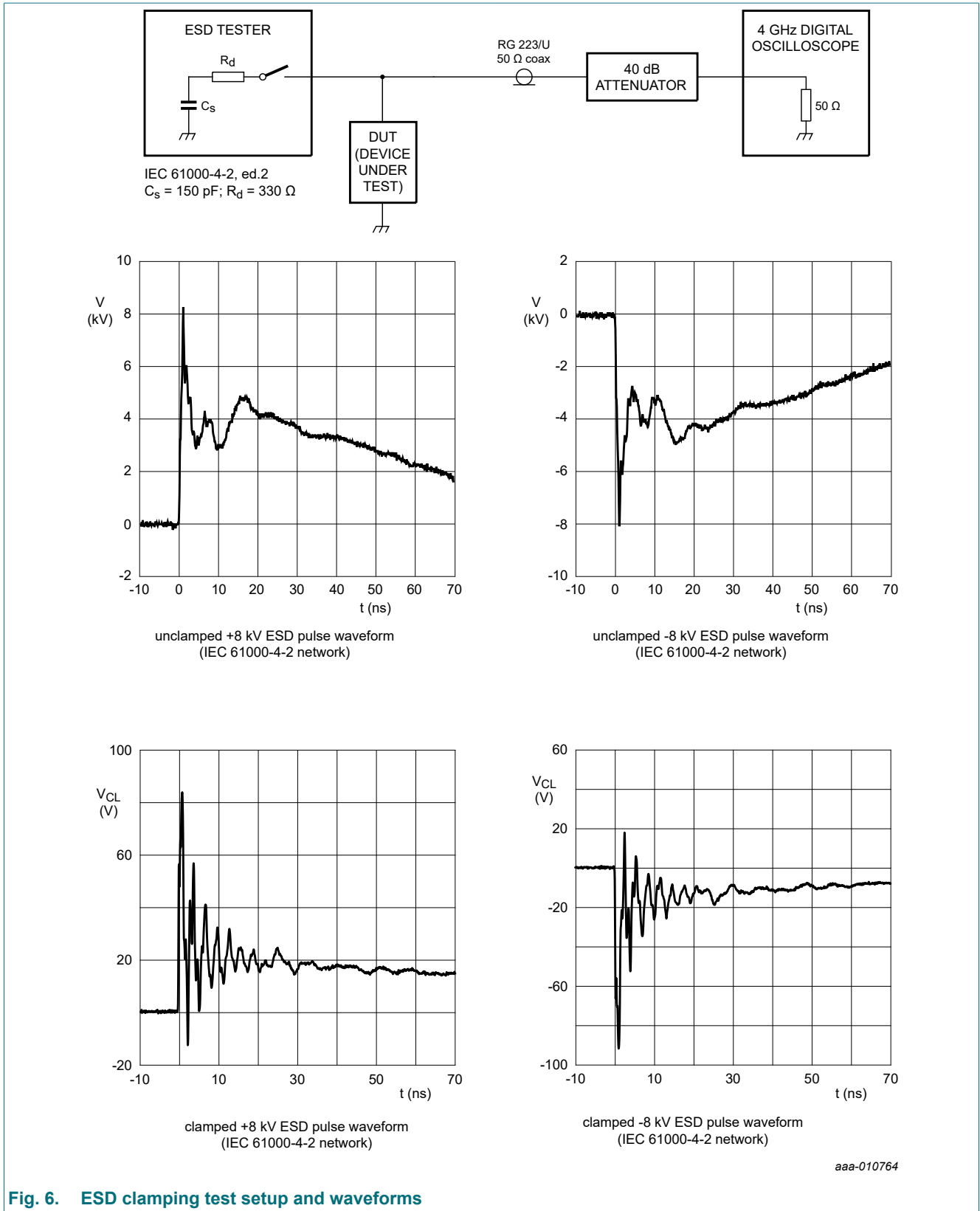


Fig. 6. ESD clamping test setup and waveforms

10. Application information

The device is designed for the protection of one bidirectional data or signal line from the damage caused by ESD. The device may be used on lines where the signal polarities are both, positive and negative with respect to ground.

The device may also be used for the protection of two unidirectional data or signal lines, which have positive signal polarities with respect to ground.

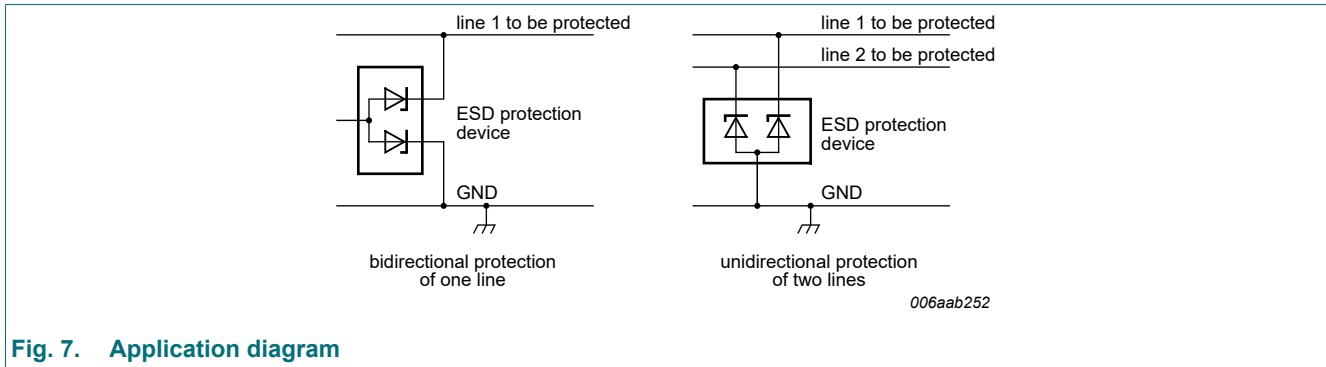


Fig. 7. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. The path length between the device and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

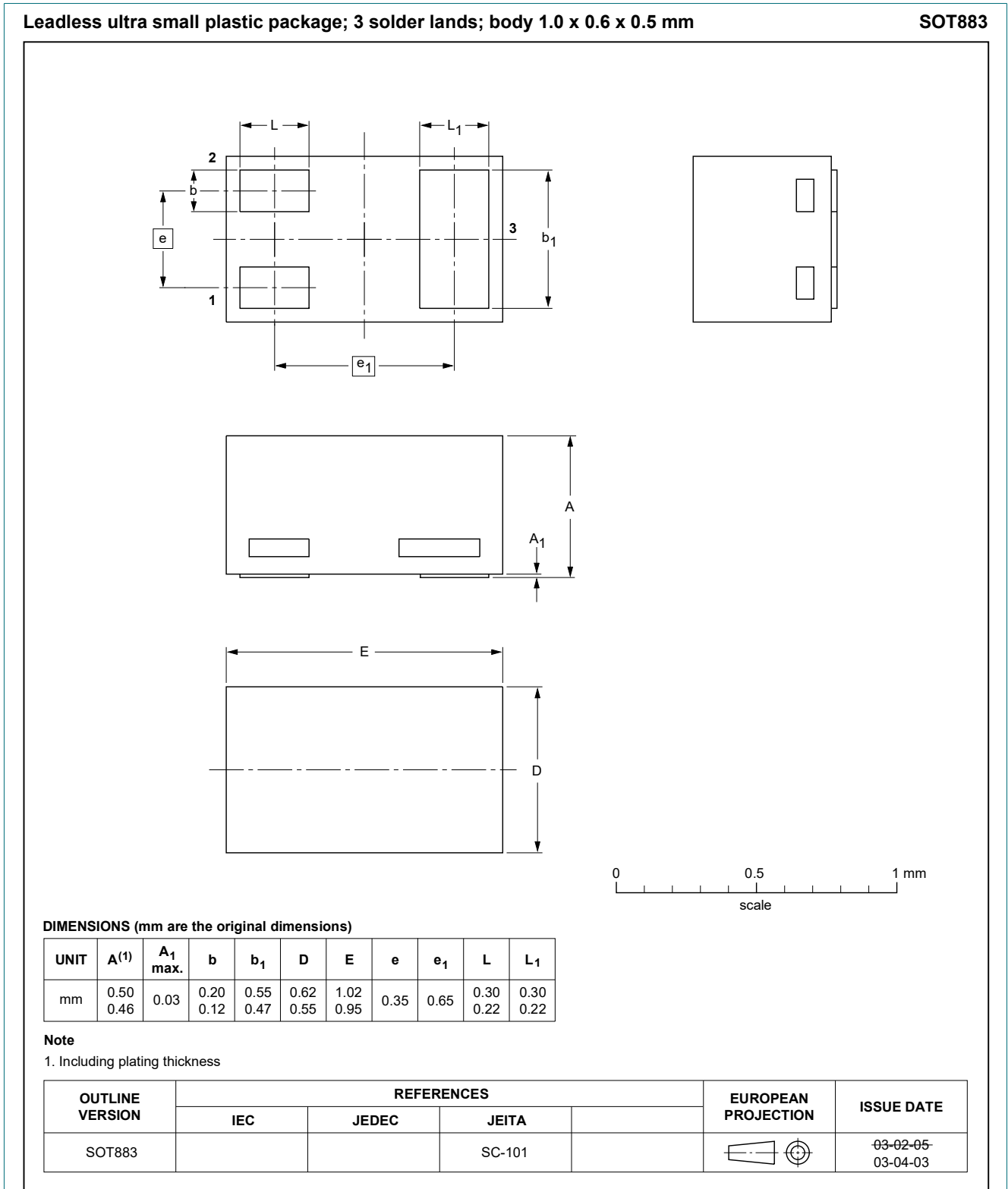


Fig. 8. Package outline DFN1006-3 (SOT883)

13. Soldering

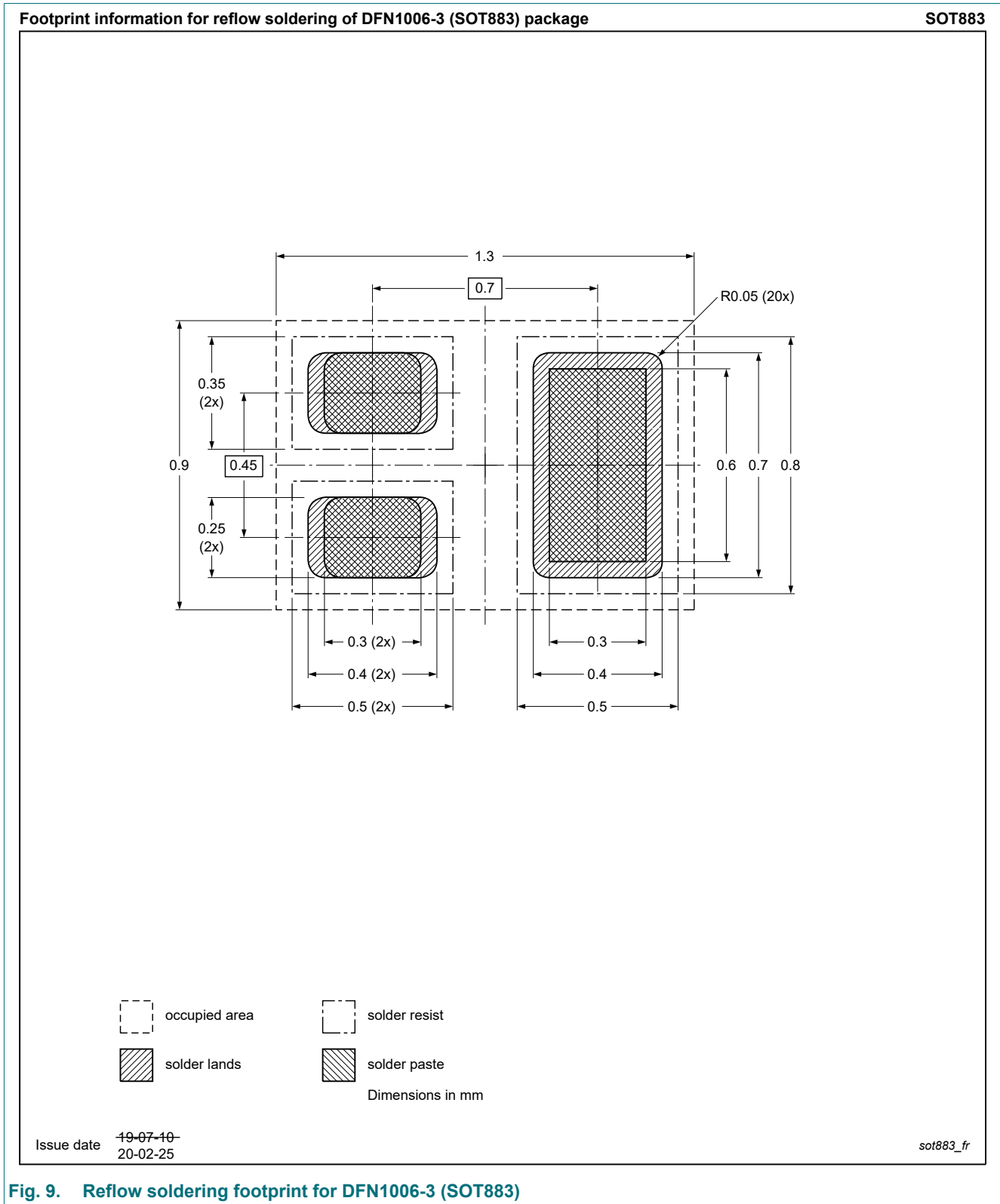


Fig. 9. Reflow soldering footprint for DFN1006-3 (SOT883)

14. Revision history

Table 7. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--------------|--------------------|---------------|------------|
| PESD5V0X2UM-Q v.1 | 20230808 | Product data sheet | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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