



BUK9215-55A

N-channel TrenchMOS logic level FET

7 April 2014

Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

3. Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	55	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; Fig. 2 ; Fig. 3	[1]	-	-	62	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	115	W
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C		-	11	13.6	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C		-	-	16.6	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; Fig. 11 ; Fig. 12		-	13	15	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 5 V; I _D = 25 A; V _{DS} = 44 V; T _j = 25 °C; Fig. 9		-	20	-	nC

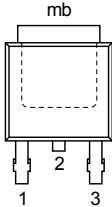
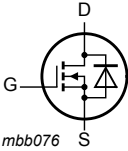
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 62\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ }^\circ\text{C}$; unclamped		-	-	211	mJ

[1] Current is limited by power dissipation chip rating.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9215-55A	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 175\text{ }^{\circ}\text{C}$		-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	55	V
V_{GS}	gate-source voltage			-15	15	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 1		-	115	W
I_D	drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 5\text{ V}$; Fig. 2 ; Fig. 3	[1]	-	62	A
			[2]	-	55	A
		$T_{mb} = 100\text{ }^{\circ}\text{C}$; $V_{GS} = 5\text{ V}$; Fig. 2	[1]	-	44	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 3		-	248	A
T_{stg}	storage temperature			-55	175	$^{\circ}\text{C}$
T_j	junction temperature			-55	175	$^{\circ}\text{C}$
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ }^{\circ}\text{C}$	[2]	-	55	A
			[1]	-	62	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$		-	248	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 62\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; unclamped		-	211	mJ

[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by bond wires.

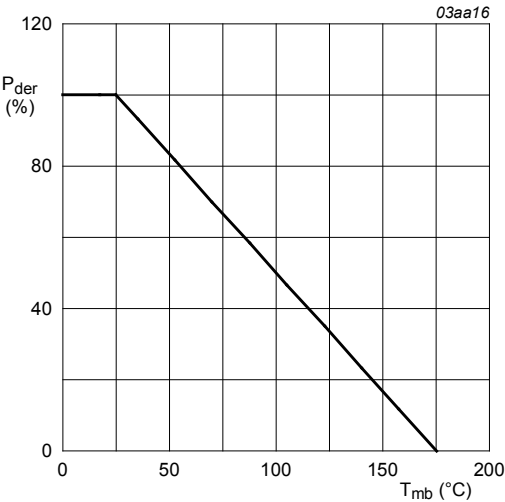


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

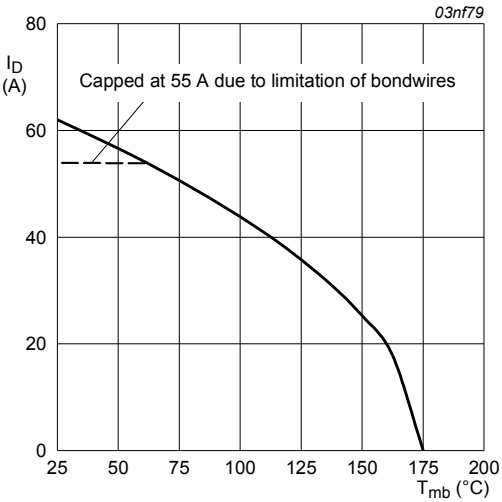


Fig. 2. Continuous drain current as a function of mounting base temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

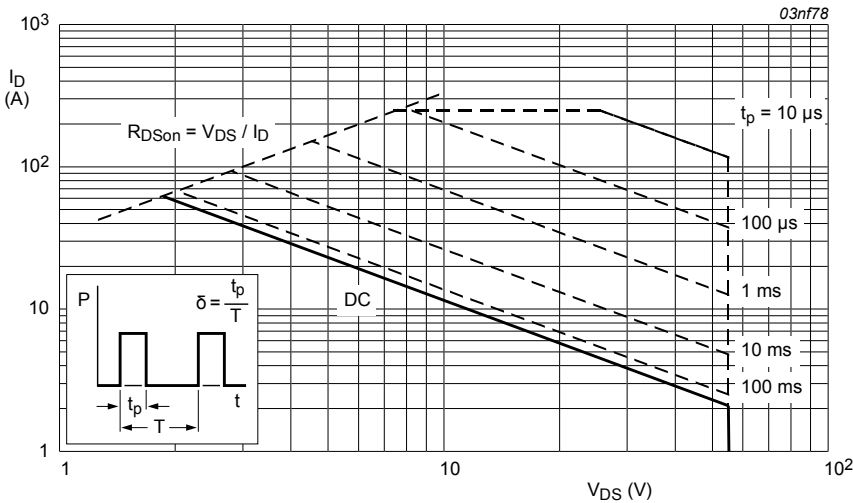


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25^{\circ}C; I_{DM} \text{ is single pulse}$$

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	-	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient			-	71.4	-	K/W

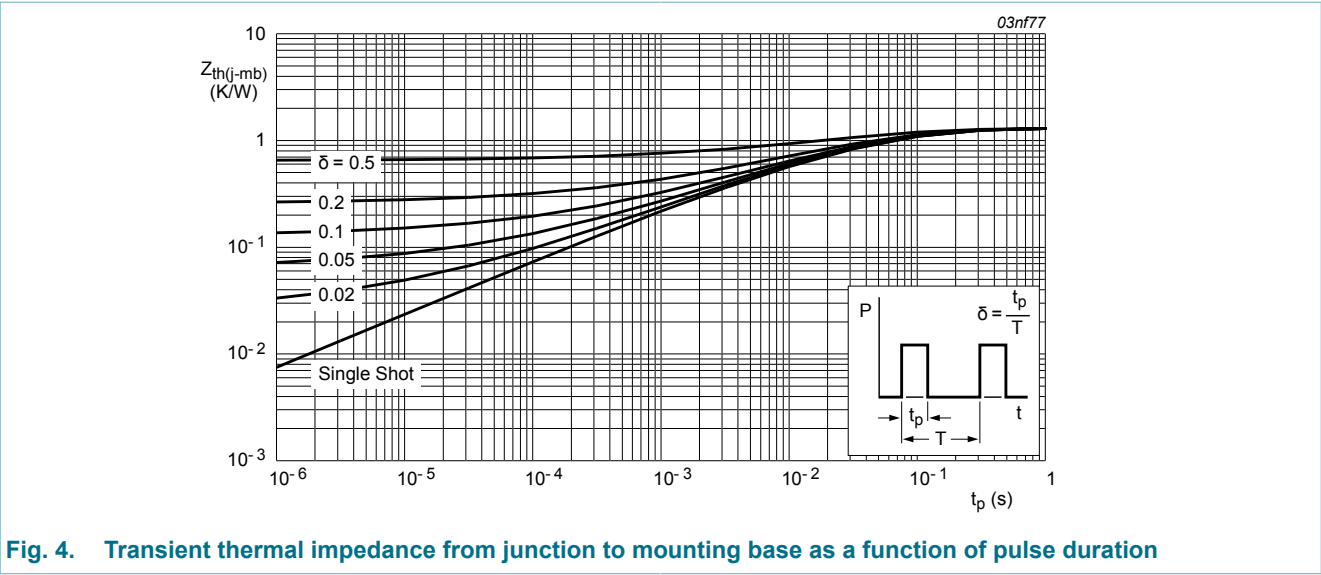


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C		55	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C		50	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 10		-	-	2.3	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 10		0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 10		1	1.5	2	V
I _{DSS}	drain leakage current	V _{DS} = 55 V; V _{GS} = 0 V; T _j = 25 °C		-	0.05	10	μA
		V _{DS} = 55 V; V _{GS} = 0 V; T _j = 175 °C		-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C		-	11	13.6	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C		-	-	16.6	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; Fig. 11 ; Fig. 12		-	-	30	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; Fig. 11 ; Fig. 12		-	13	15	mΩ
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 44 V; V _{GS} = 5 V; T _j = 25 °C; Fig. 9		-	48	-	nC
Q _{GS}	gate-source charge			-	6	-	nC
Q _{GD}	gate-drain charge			-	20	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; Fig. 13		-	2190	2916	pF
C _{oss}	output capacitance			-	380	450	pF
C _{rss}	reverse transfer capacitance			-	250	344	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 5 V; R _{G(ext)} = 10 Ω; T _j = 25 °C		-	19	-	ns
t _r	rise time			-	161	-	ns
t _{d(off)}	turn-off delay time			-	138	-	ns
t _f	fall time			-	165	-	ns
L _D	internal drain inductance	measured from drain to centre of die		-	2.5	-	nH

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L_S	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 20\text{ A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$; Fig. 14	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$;	-	51	-	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$	-	102	-	nC

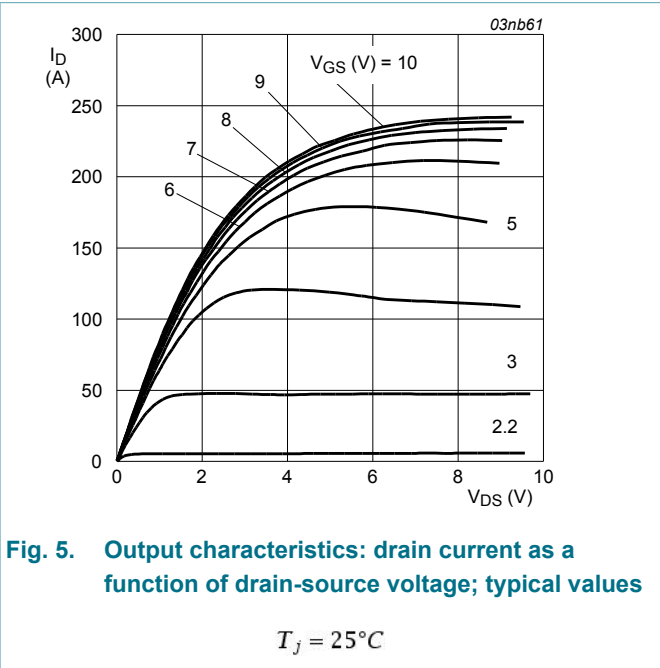


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

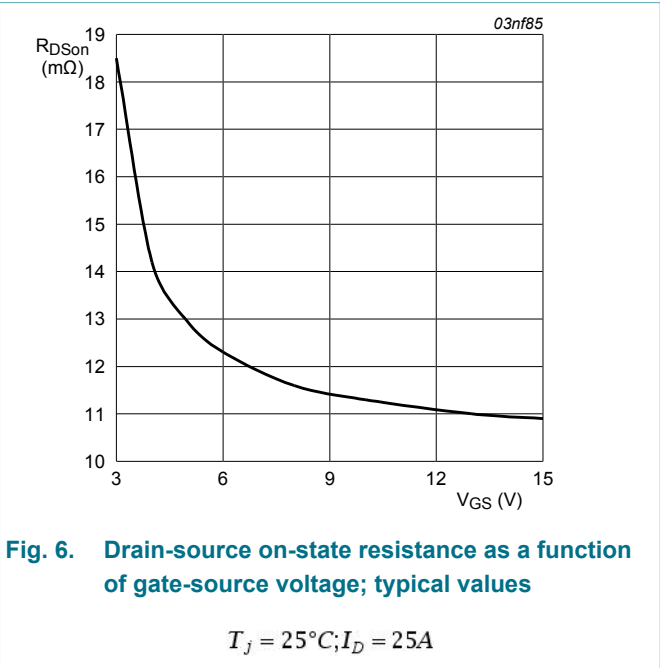


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

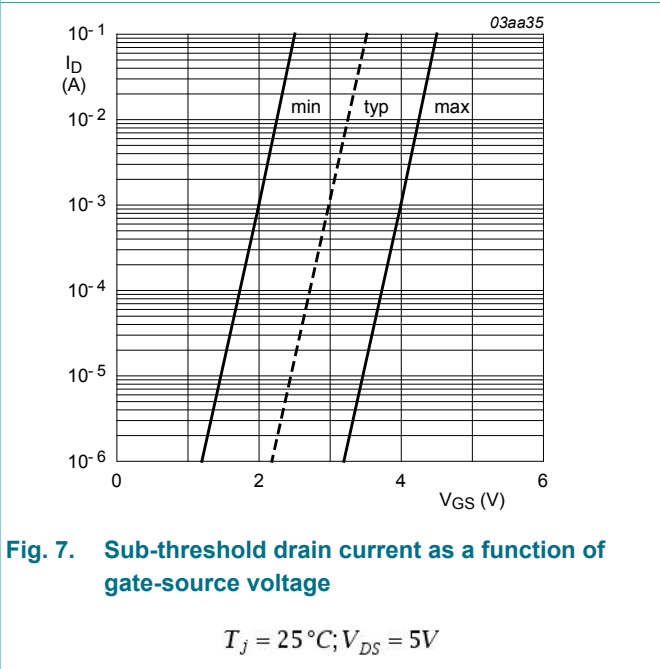


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

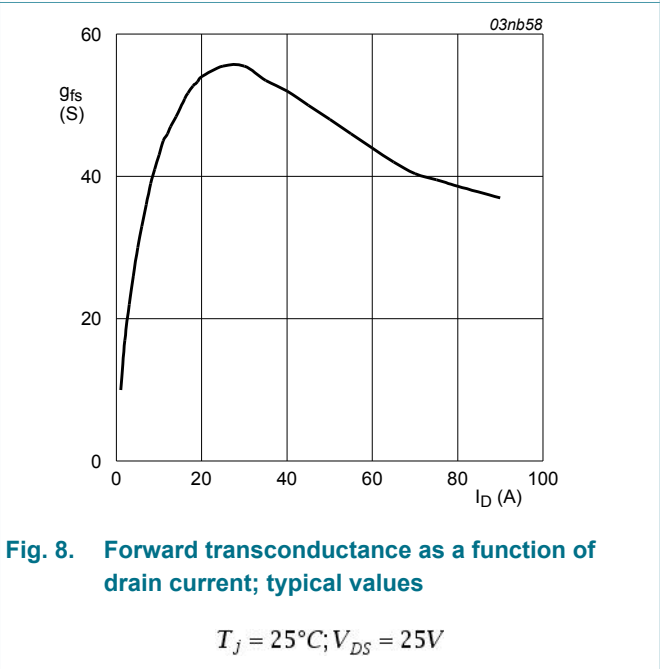


Fig. 8. Forward transconductance as a function of drain current; typical values

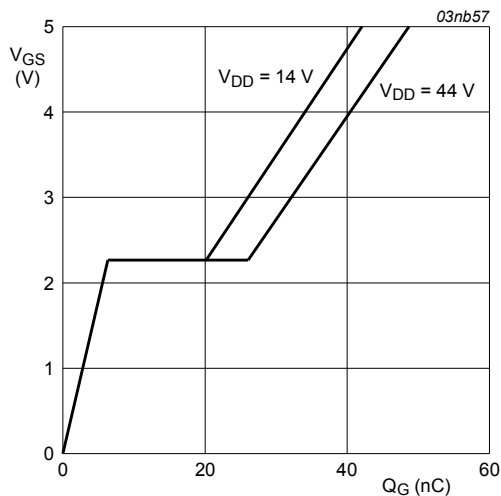


Fig. 9. Gate-source voltage as a function of turn-on gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 25\text{ A}$

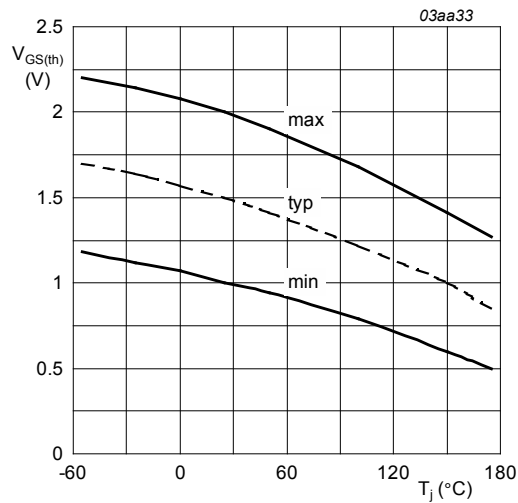


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

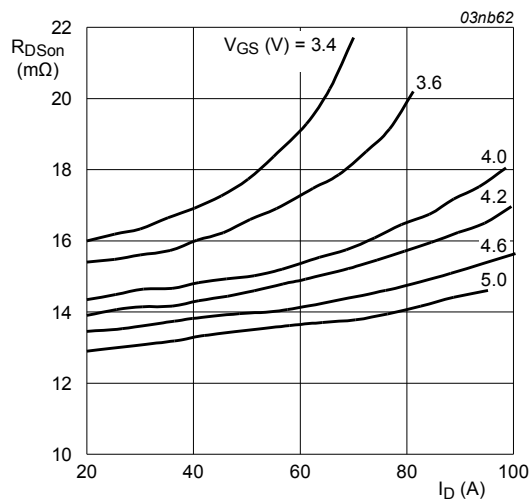


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$

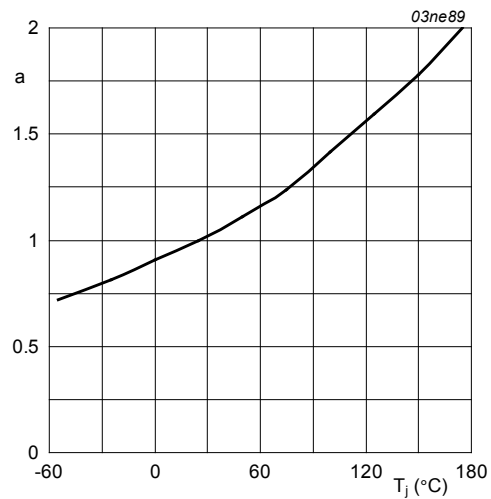


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

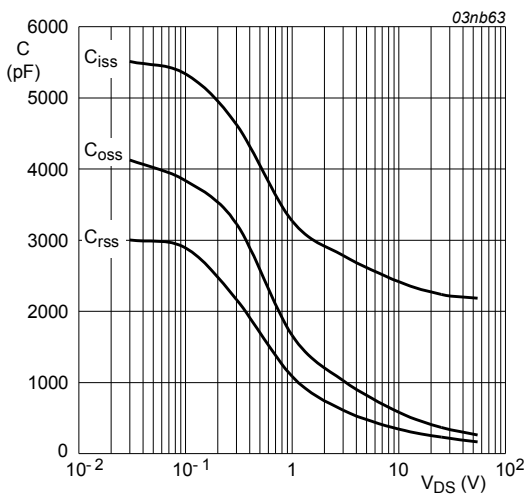


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

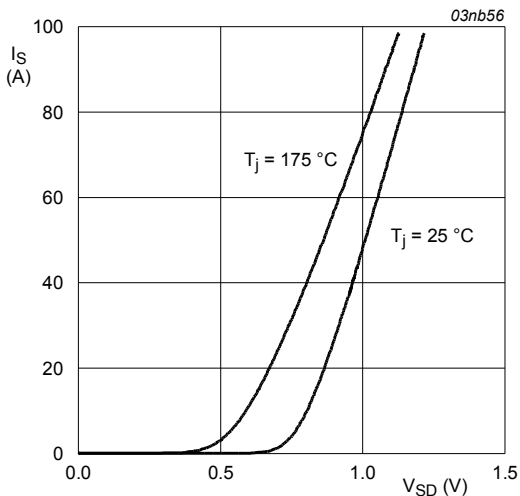


Fig. 14. Reverse diode current; typical value

$$V_{GS} = 0V$$

10. Package outline

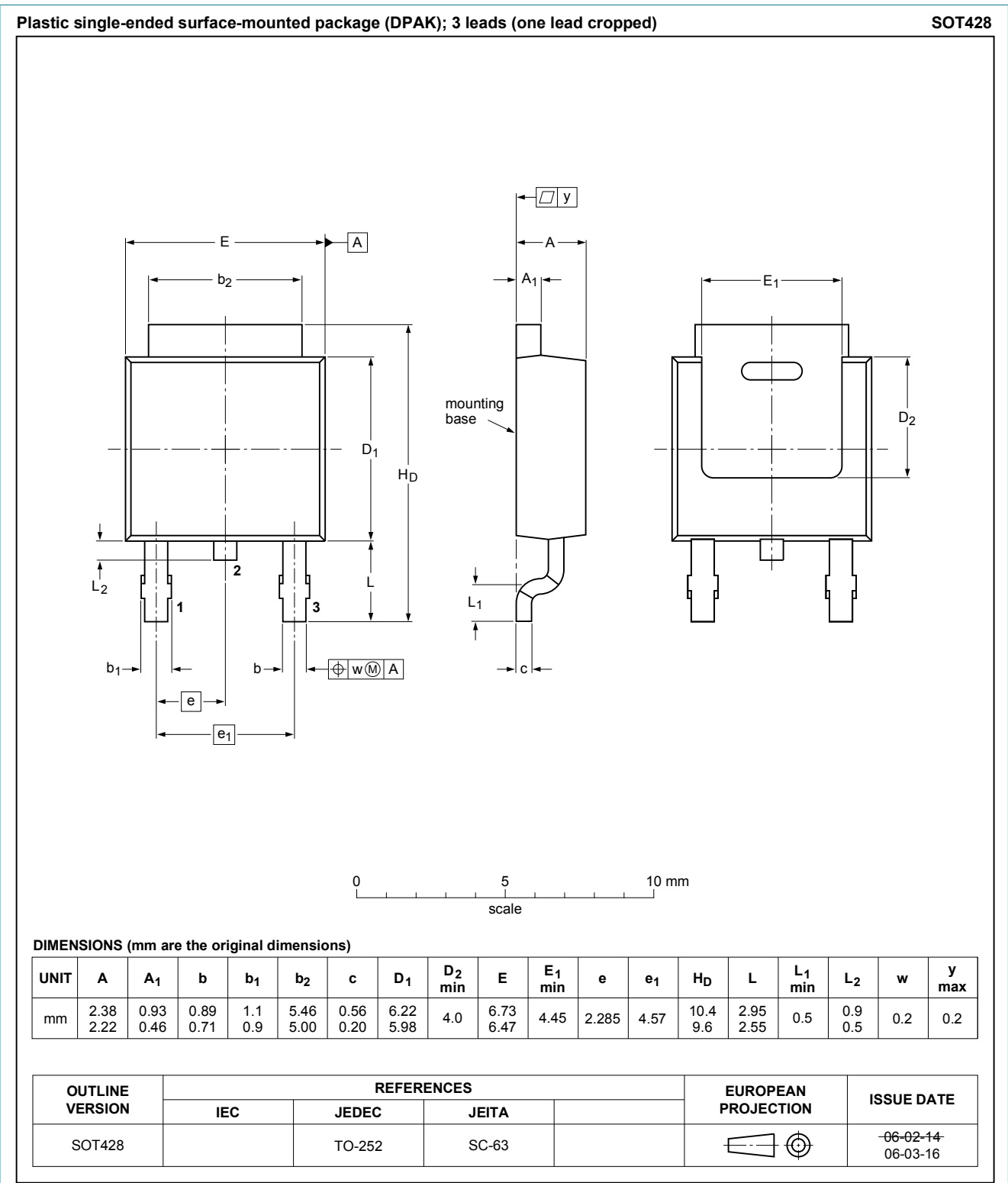


Fig. 15. Package outline DPAK (SOT428)

11. Legal information

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