

# 74AHC00; 74AHCT00

## Quad 2-input NAND gate

Rev. 04 — 28 April 2008

Product data sheet

## 1. General description

The 74AHC00; 74AHCT00 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. JESD7-A.

The 74AHC00; 74AHCT00 provides the quad 2-input NAND function.

## 2. Features

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than  $V_{CC}$
- Input levels:
  - ◆ For 74AHC00: CMOS level
  - ◆ For 74AHCT00: TTL level
- ESD protection:
  - ◆ HBM EIA/JESD22-A114E exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V
  - ◆ CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Ordering information

Table 1. Ordering information

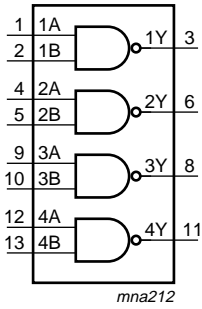
Type number	Package			Version
	Temperature range	Name	Description	
<b>74AHC00</b>				
74AHC00D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHC00PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHC00BQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1

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Table 1. Ordering information ...continued

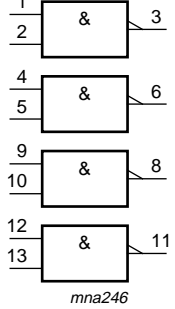
Type number	Package			Version
	Temperature range	Name	Description	
<b>74AHCT00</b>				
74AHCT00D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCT00PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCT00BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

### 4. Functional diagram



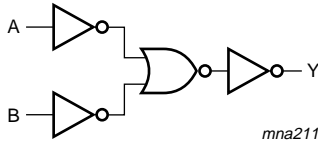
*mna212*

**Fig 1. Logic symbol**



*mna246*

**Fig 2. IEC logic symbol**

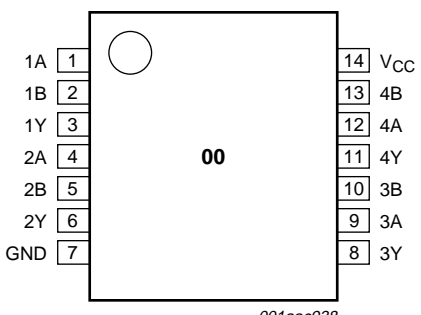


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**Fig 3. Logic diagram (one gate)**

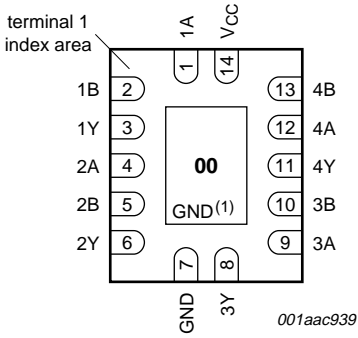
### 5. Pinning information

#### 5.1 Pinning



*001aac938*

**Fig 4. Pin configuration SO14 and TSSOP14**



*001aac939*

Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

**Fig 5. Pin configuration DHVQFN14**

## 5.2 Pin description

**Table 2.** Pin description

Symbol	Pin	Description
1A	1	data input
1B	2	data input
1Y	3	data output
2A	4	data input
2B	5	data input
2Y	6	data output
GND	7	ground (0 V)
3Y	8	data output
3A	9	data input
3B	10	data input
4Y	11	data output
4A	12	data input
4B	13	data input
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3.** Function selection<sup>[1]</sup>

Input		Output
nA	nB	nY
L	X	H
X	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	[1] -20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1] -20	+20	mA
$I_O$	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5)$ V	-25	+25	mA
$I_{CC}$	supply current		-	+75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 packages: above 70 °C the value of  $P_{tot}$  derates linearly at 8 mW/K.  
 For TSSOP14 packages: above 60 °C the value of  $P_{tot}$  derates linearly at 5.5 mW/K.  
 For DHVQFN14 packages: above 60 °C the value of  $P_{tot}$  derates linearly at 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74AHC00</b>						
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0$ V to 3.6 V	-	-	100	ns/V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	20	ns/V
<b>74AHCT00</b>						
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 4.5$ V to 5.5 V	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC00</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2.0	-	20	-	40	μA
C <sub>I</sub>	input capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	-	3.0	10	-	10	-	10	pF
<b>74AHCT00</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA

**Table 6.** Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	2.0	-	20	-	40	$\mu$ A
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other pins at $V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	-	3.0	10	-	10	-	10	pF

## 10. Dynamic characteristics

**Table 7.** Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	

### 74AHC00

$t_{pd}$	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a> <sup>[2]</sup>								
		$V_{CC} = 3.0$ V to 3.6 V								
		$C_L = 15$ pF	-	4.5	7.9	1.0	9.5	1.0	10.0	ns
		$C_L = 50$ pF	-	6.0	11.4	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5$ V to 5.5 V								
		$C_L = 15$ pF	-	3.2	5.5	1.0	6.5	1.0	7.0	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50$ pF; $f_i = 1$ MHz; <sup>[3]</sup>	-	7.0	-	-	-	-	-	pF
		$V_I =$ GND to $V_{CC}$								

### 74AHCT00

$t_{pd}$	propagation delay	nA, nB to nY; see <a href="#">Figure 6</a> <sup>[2]</sup>								
		$V_{CC} = 4.5$ V to 5.5 V								
		$C_L = 15$ pF	-	3.3	6.9	1.0	8.0	1.0	9.0	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50$ pF; $f_i = 1$ MHz; <sup>[3]</sup>	-	7.0	-	-	-	-	-	pF
		$V_I =$ GND to $V_{CC}$								

[1] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3$  V and  $V_{CC} = 5.0$  V).

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

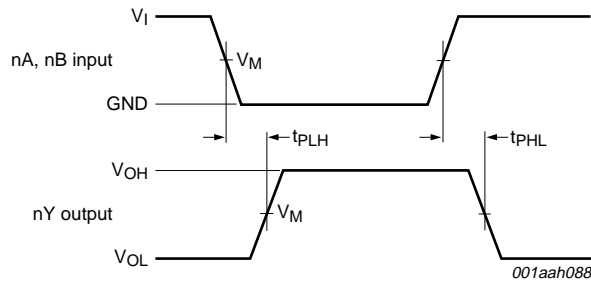
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

11. Waveforms

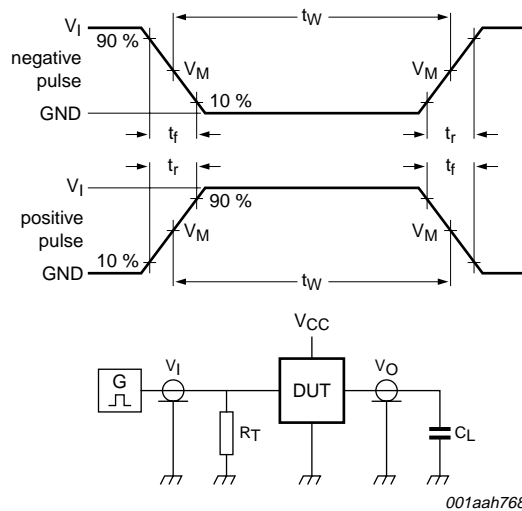


Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. Input to output propagation delays**

**Table 8. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74AHC00	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT00	1.5 V	$0.5 \times V_{CC}$



Test data is given in [Table 9](#).  
 Definitions test circuit:  
 $R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.  
 $C_L$  = load capacitance including jig and probe capacitance.

**Fig 7. Load circuitry for measuring switching times**

Table 9. Test data

Type	Input		Load	Test
	$V_I$	$t_r, t_f$	$C_L$	
74AHC00	$V_{CC}$	$\leq 3.0$ ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74AHCT00	3.0 V	$\leq 3.0$ ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$



12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

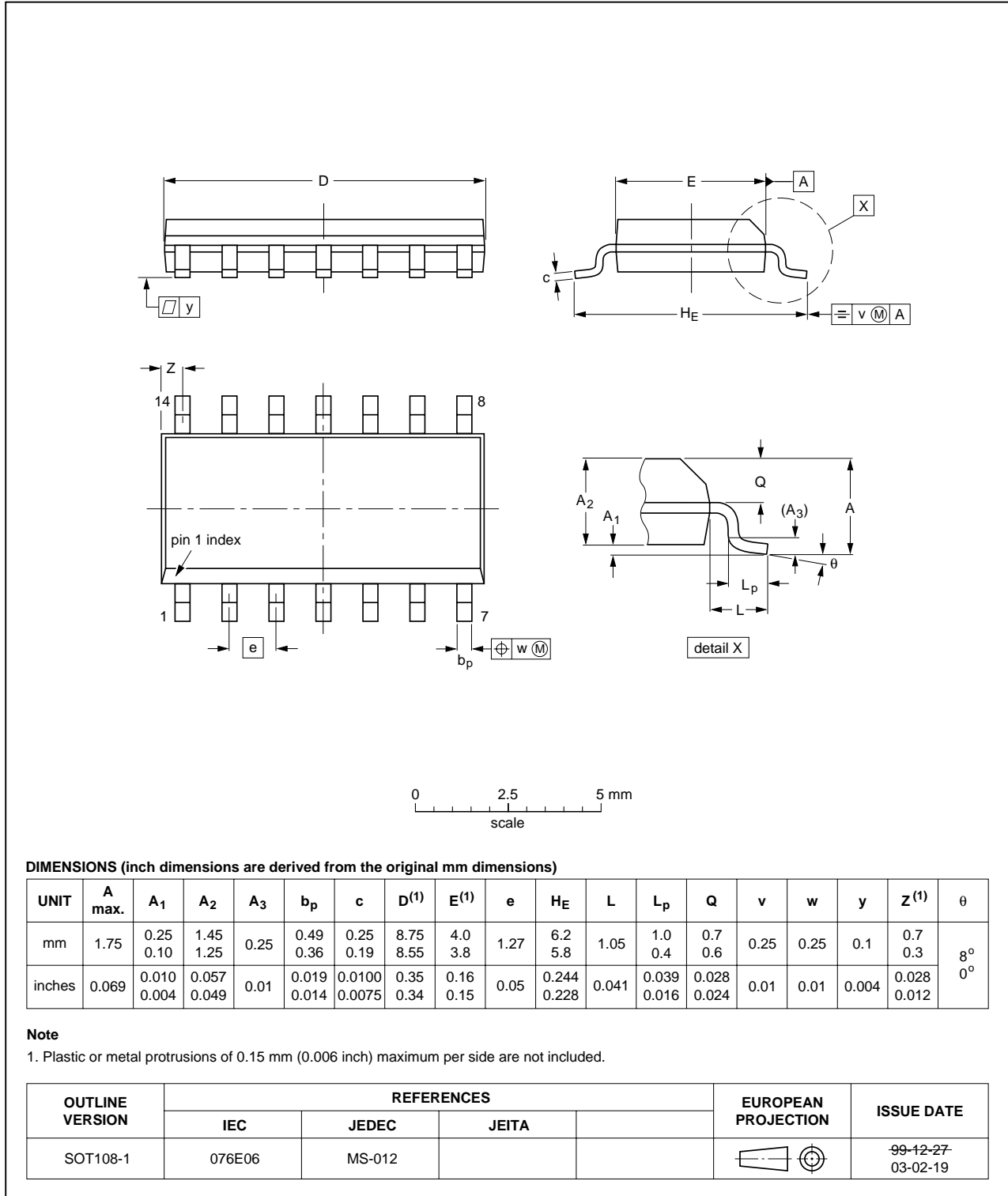


Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

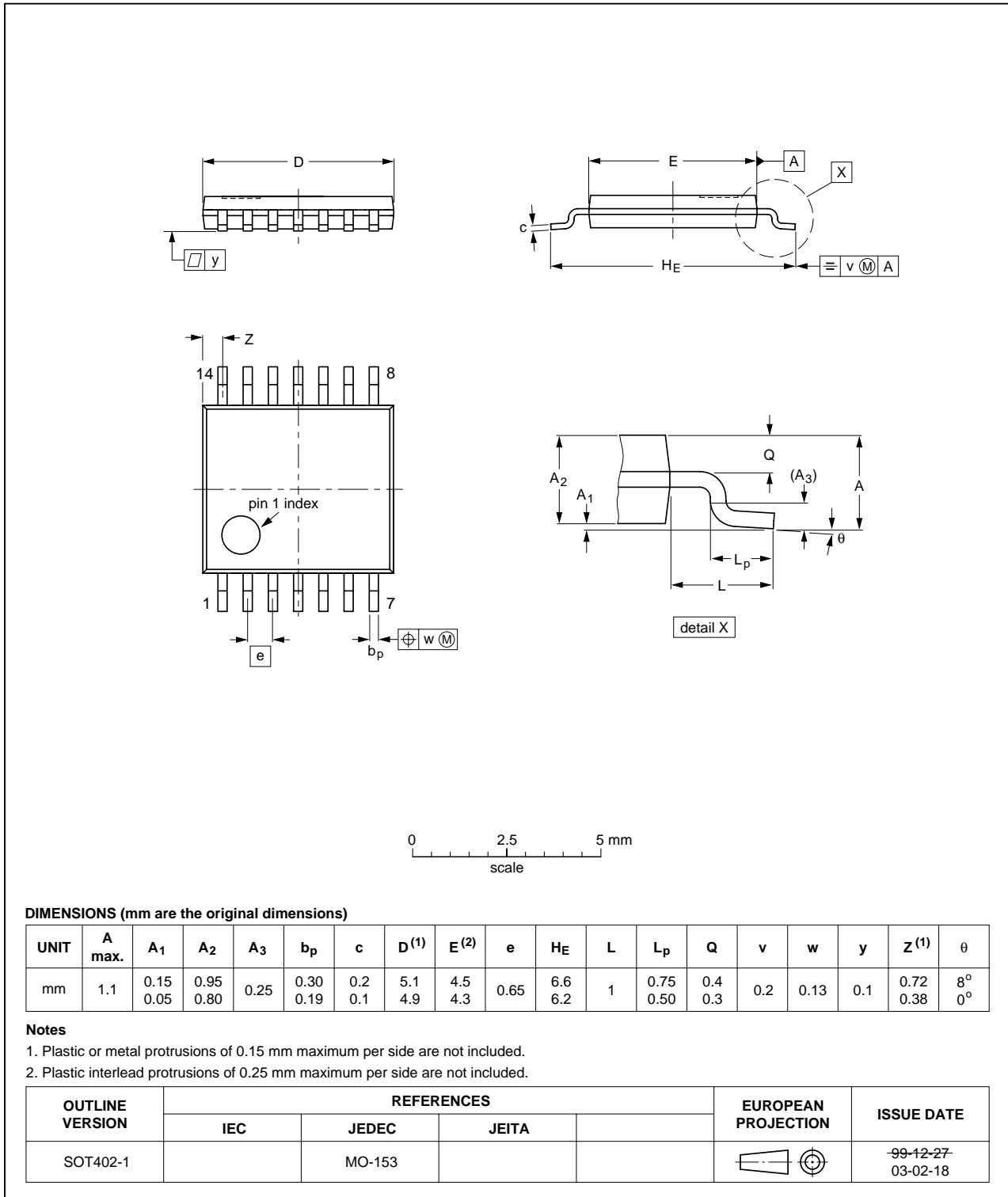


Fig 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

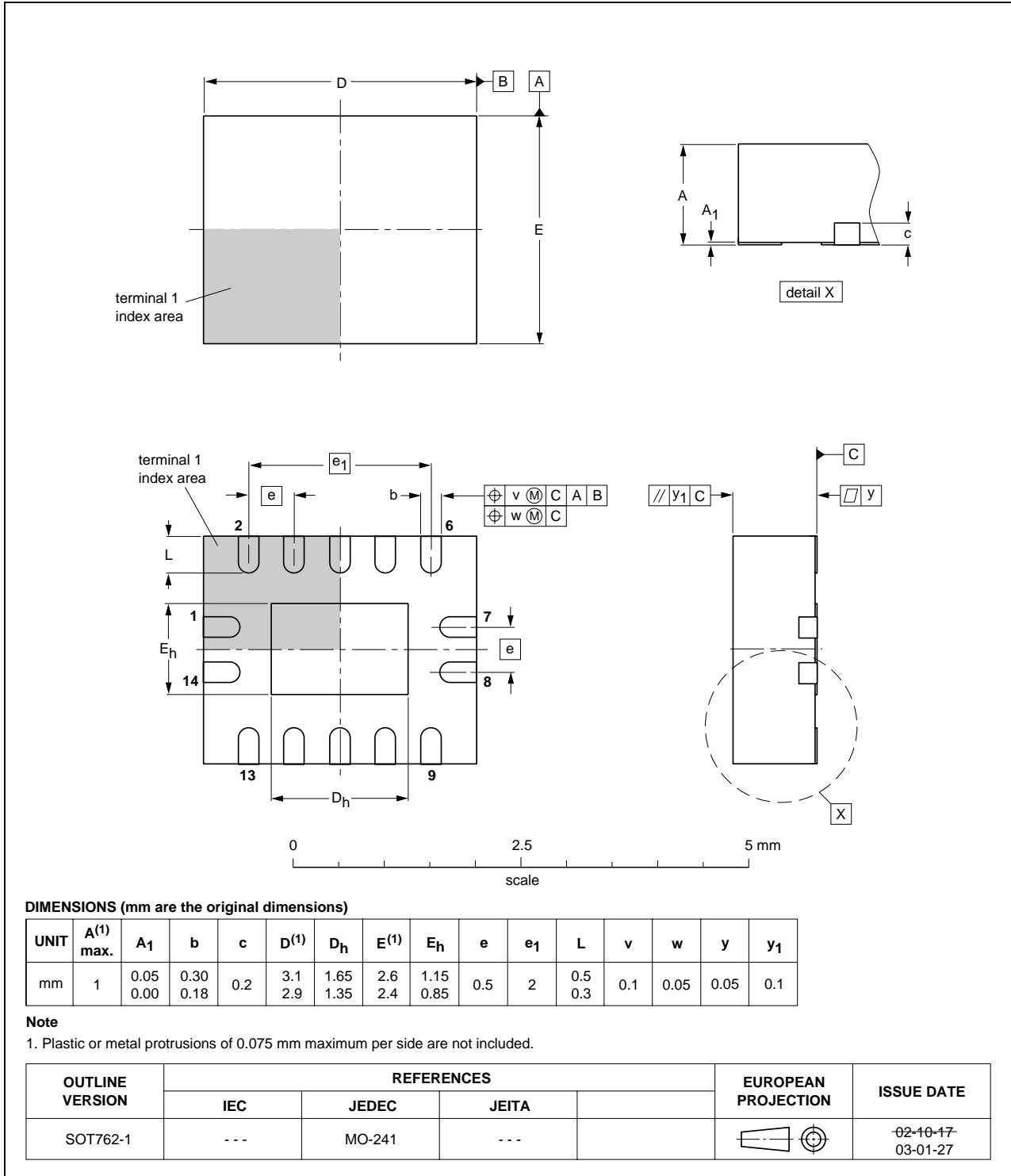


Fig 10. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charge Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT00_4	20080428	Product data sheet	-	74AHC_AHCT00_3
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 6</a>: the conditions for input leakage current have been changed.</li> </ul>			
74AHC_AHCT00_3	20080108	Product data sheet	-	74AHC_AHCT00_2
74AHC_AHCT00_2	19990923	Product specification	-	74AHC_AHCT00_1
74AHC_AHCT00_1	19981209	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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