

74AHC2G125-Q100; 74AHCT2G125-Q100

Dual buffer/line driver; 3-state

Rev. 2 — 2 January 2019

Product data sheet

1. General description

The 74AHC2G125-Q100 and 74AHCT2G125-Q100 are high-speed Si-gate CMOS devices. They provide a dual non-inverting buffer/line driver with 3-state output. The output enable input (nOE) controls the 3-state output. A HIGH at nOE causes the output to assume a high-impedance OFF-state.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AHC2G125DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74AHCT2G125DP-Q100				
74AHC2G125DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AHCT2G125DC-Q100				

4. Marking

Table 2. Marking codes

Type number	Marking[1]
74AHC2G125DP-Q100	A25
74AHCT2G125DP-Q100	C25
74AHC2G125DC-Q100	A25
74AHCT2G125DC-Q100	C25

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

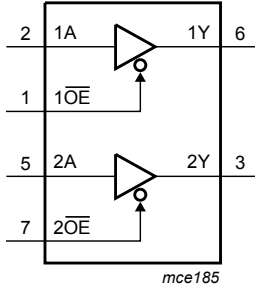


Fig. 1. Logic symbol

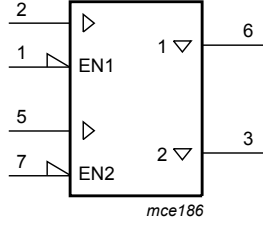


Fig. 2. IEC logic symbol

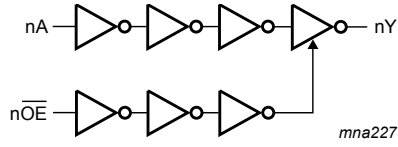


Fig. 3. Logic diagram (one buffer)

6. Pinning information

6.1. Pinning

74AHC2G125-Q100
74AHCT2G125-Q100

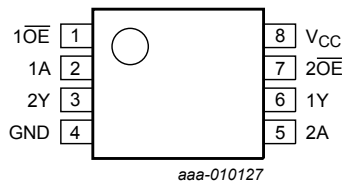


Fig. 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 7	output enable input (active LOW)
1A, 2A	2, 5	data input
GND	4	ground (0 V)
1Y, 2Y	6, 3	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V [1]	-20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±20	mA
I_O	output current	-0.5 V < V_O < $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC2G125-Q100			74AHCT2G125-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V ± 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V ± 0.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC2G125-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 µA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _{OZ}	OFF-state output current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	0.25	-	2.5	-	10	µA
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
C _I	input capacitance		-	1.5	10	-	10	-	10	pF
74AHCT2G125-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _{oZ}	OFF-state output current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	0.25	-	2.5	-	10	µA
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _I = 3.4 V; other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance		-	1.5	10	-	10	-	10	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
74AHC2G125-Q100										
t _{pd}	propagation delay	nA to nY; see Fig. 5 [2]								
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	4.7	8.0	1.0	9.5	1.0	11.5	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	-	6.6	11.5	1.0	13.0	1.0	14.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
t _{en}	enable time	nOE to nY; see Fig. 6 [2]								
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	5.0	8.0	1.0	9.5	1.0	11.5	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	-	6.9	11.5	1.0	13.0	1.0	14.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.6	5.1	1.0	6.0	1.0	6.5	ns
t _{dis}	disable time	nOE to nY; see Fig. 6 [2]								
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	6.0	9.7	1.0	11.5	1.0	12.5	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	-	8.3	13.2	1.0	15.0	1.0	16.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	4.1	6.8	1.0	8.0	1.0	8.5	ns
C _{PD}	power dissipation capacitance	V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.7	8.8	1.0	10.0	1.0	11.0	ns
		per buffer; C _L = 50 pF; f _i = 1 MHz; [3] V _I = GND to V _{CC}	-	9	-	-	-	-	-	pF
74AHCT2G125-Q100										
t _{pd}	propagation delay	nA to nY; see Fig. 5 [2]								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.4	5.5	1.0	6.5	1.0	6.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	4.8	7.5	1.0	8.5	1.0	8.5	ns
t _{en}	enable time	nOE to nY; see Fig. 6 [2]								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.9	5.1	1.0	6.0	1.0	6.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.1	7.5	1.0	8.5	1.0	8.5	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
t _{dis}	disable time	n $\overline{\text{OE}}$ to nY; see Fig. 6 [2]								
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	4.5	6.8	1.0	8.0	1.0	8.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	6.1	8.8	1.0	10.0	1.0	10.0	ns
C _{PD}	power dissipation capacitance	per buffer; C _L = 50 pF; f _i = 1 MHz; [3] V _i = GND to V _{CC}	-	11	-	-	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V and 5.0 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.
- [3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in Volts.

11.1. Waveforms and test circuit

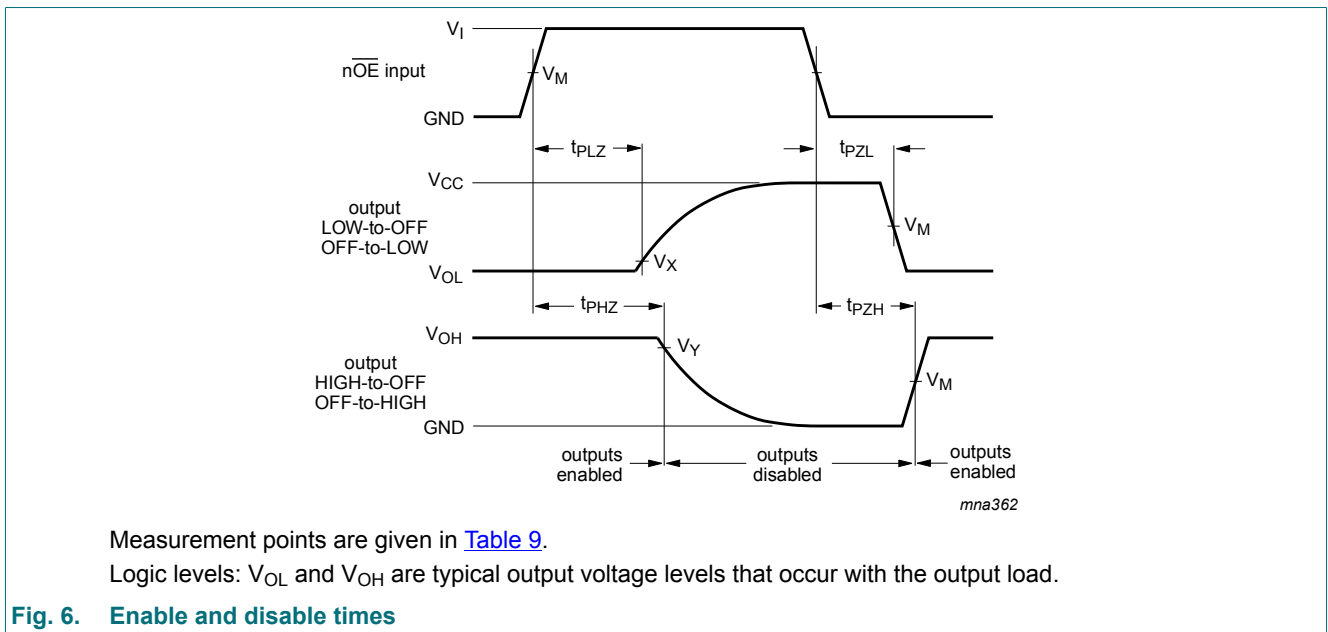
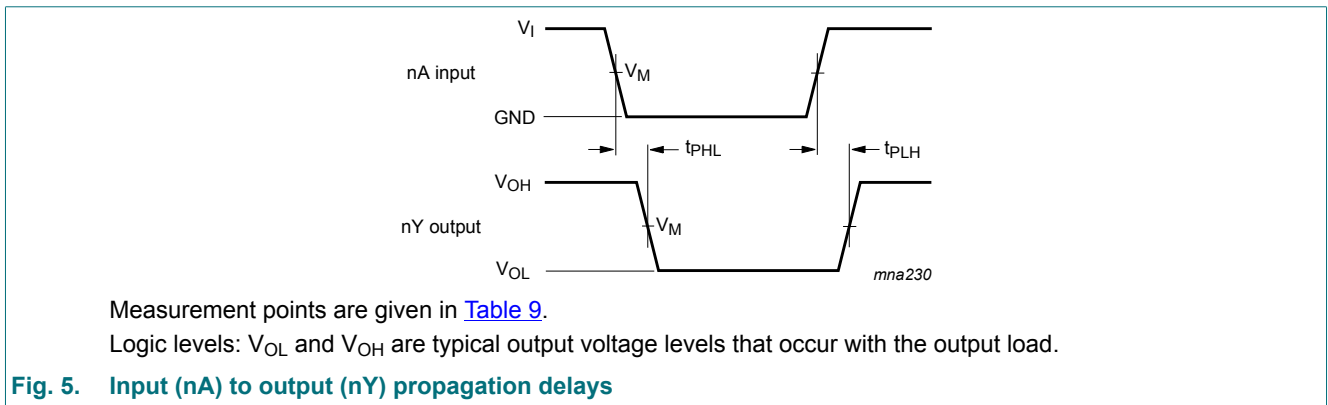


Table 9. Measurement points

Type	Input		Output	
	V_M		V_M	V_X
74AHC2G125-Q100	$0.5V_{CC}$		$0.5V_{CC}$	$V_{OL} + 0.3 V$
74AHCT2G125-Q100	1.5 V		$0.5V_{CC}$	$V_{OH} - 0.3 V$

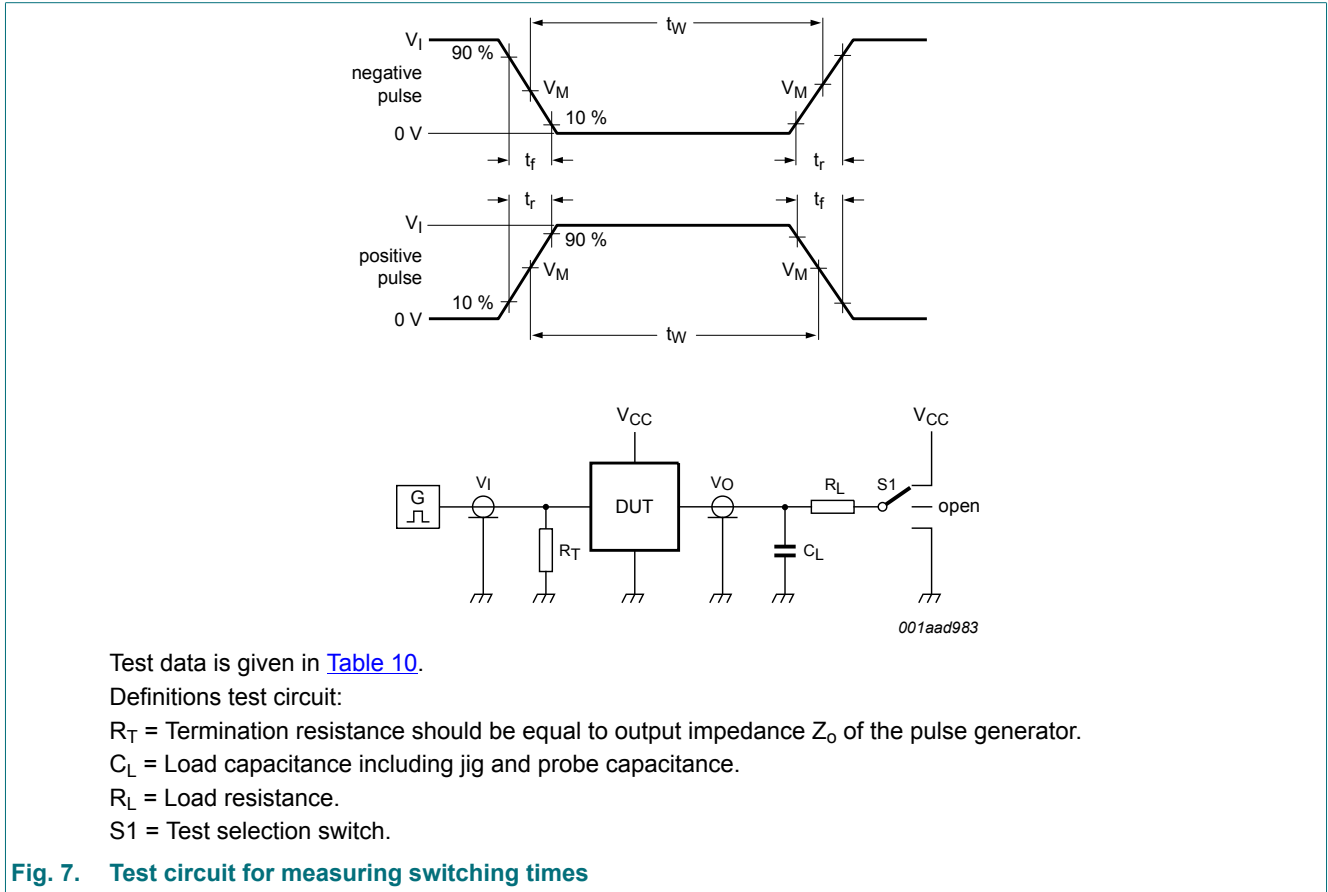


Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC2G125-Q100	V_{CC}	$\leq 3 \text{ ns}$	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74AHCT2G125-Q100	3 V	$\leq 3 \text{ ns}$	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

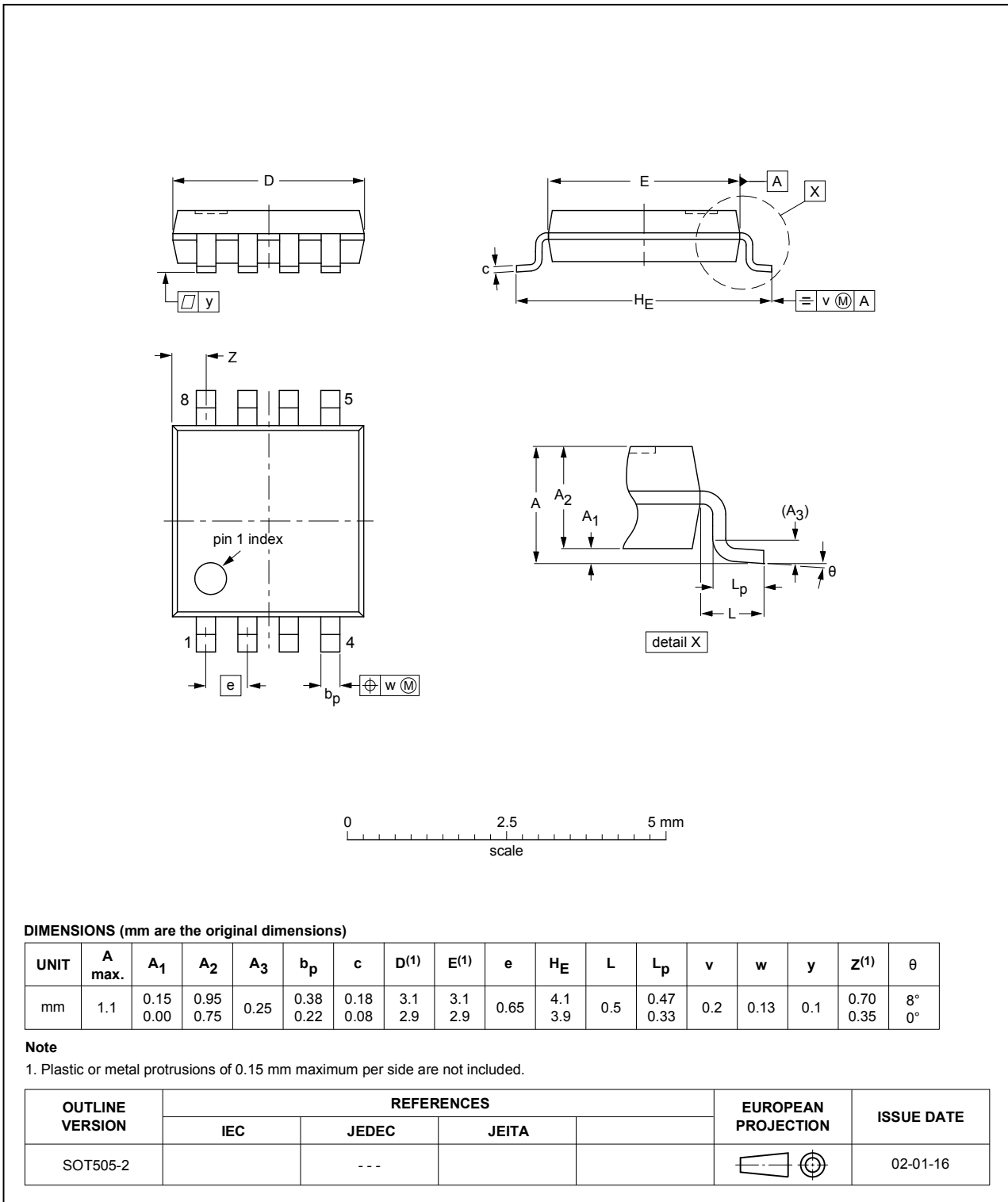


Fig. 8. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Fig. 9. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT2G125_Q100 v.2	20190102	Product data sheet	-	74AHC_AHCT2G125_Q100 v.1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Package outline drawing SOT765-1 (VSSOP8) updated. 			
74AHC_AHCT2G125_Q100 v.1	20140311	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 2 January 2019

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