

# 74ALVC14

Hex inverting Schmitt trigger

Rev. 4 — 14 August 2018

Product data sheet

## 1. General description

The 74ALVC14 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74ALVC14 provides six inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

## 2. Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Unlimited input rise and fall times
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVC14D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ALVC14PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ALVC14BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

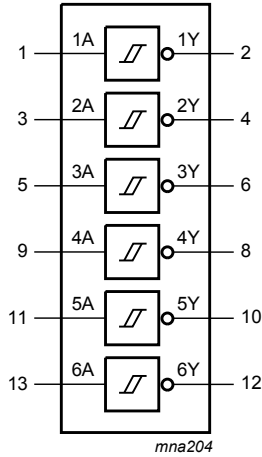


Fig. 1. Logic symbol

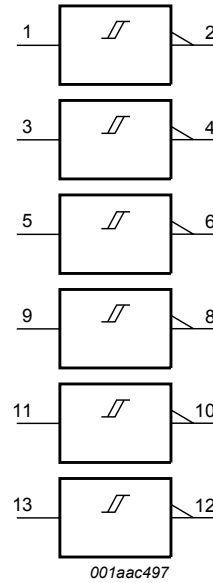


Fig. 2. IEC logic symbol

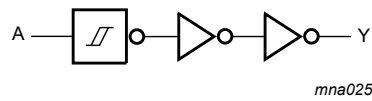


Fig. 3. Logic diagram (one Schmitt trigger)

## 5. Pinning information

### 5.1. Pinning

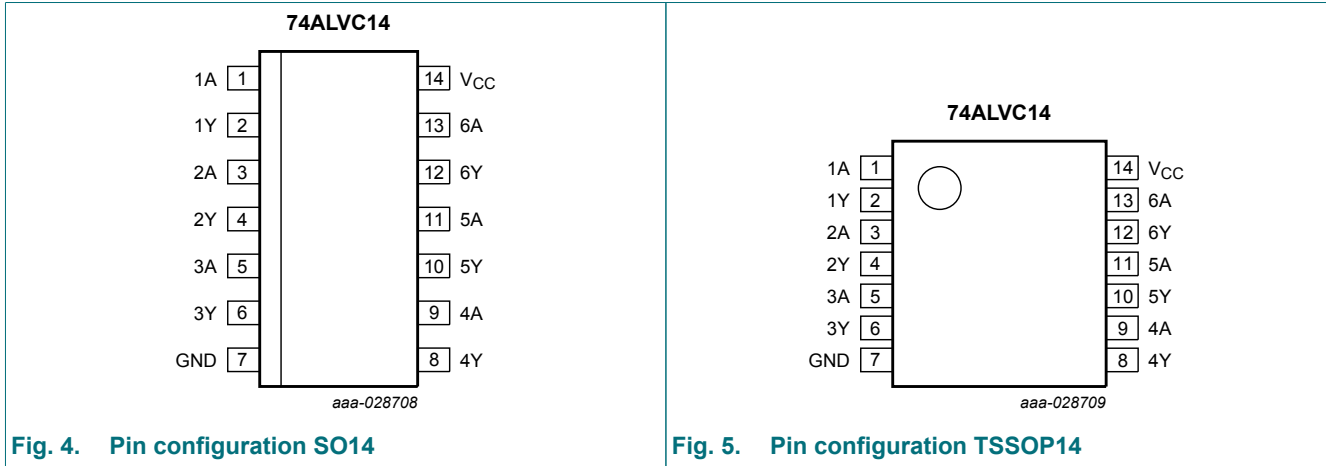


Fig. 4. Pin configuration SO14

Fig. 5. Pin configuration TSSOP14

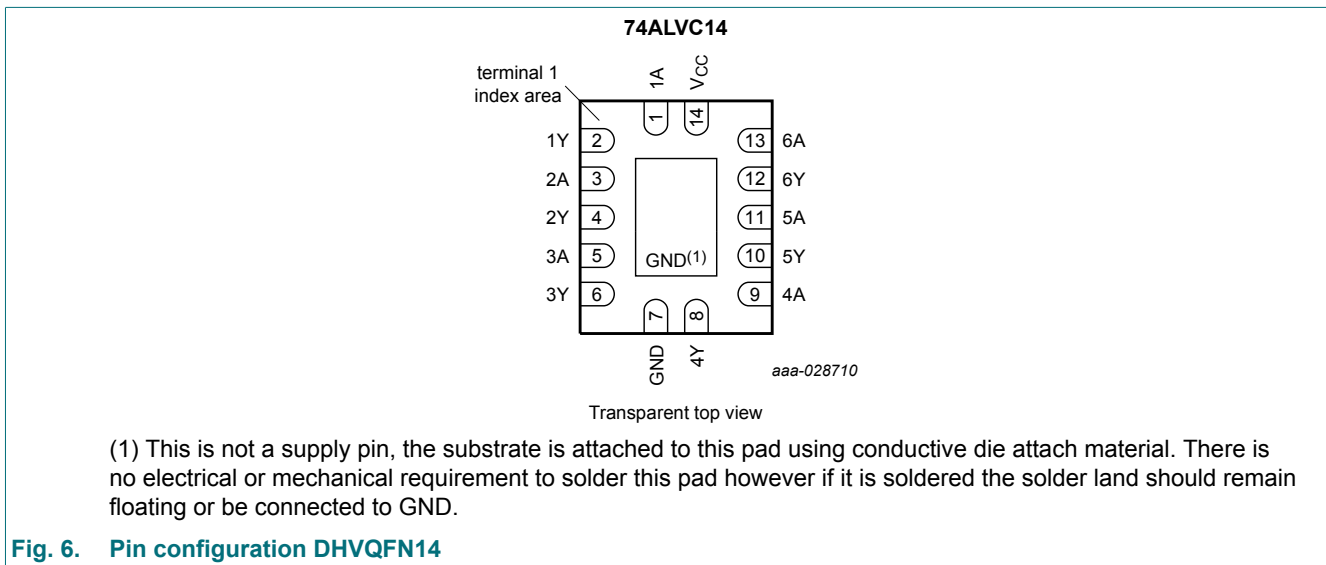


Fig. 6. Pin configuration DHVQFN14

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level;*

Input nA	Output nY
L	H
H	L

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage		[1] -0.5	+4.6	V
$V_O$	output voltage	active mode	[1] -0.5	$V_{CC} + 0.5$	V
		power-down mode, $V_{CC} = 0$ V	-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-	-50	mA
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$I_{O(sink/source)}$	output sink or source current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C	[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 packages: above 70 °C derate linearly with 8 mW/K.

For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	$V_{CC} = 1.65$ to 3.6 V	0	$V_{CC}$	V
		power-down mode; $V_{CC} = 0$ V	0	3.6	V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 1.65 V	-	0.11	0.3	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.3 V	-	0.17	0.4	V
		I <sub>O</sub> = 18 mA; V <sub>CC</sub> = 2.3 V	-	0.25	0.6	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V;	-	0.16	0.4	V
		I <sub>O</sub> = 18 mA; V <sub>CC</sub> = 3.0 V	-	0.23	0.4	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	0.30	0.55	V
V <sub>OH</sub>	HIGH-level voltage output	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 1.65 V	1.25	1.51	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.3 V	1.8	2.10	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 2.3 V	1.7	2.01	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V;	2.2	2.53	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	2.76	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	2.68	-	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 3.6 V or GND	-	±0.1	±5	μA
I <sub>off</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 3.6 V	-	±0.1	±10	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.2	10	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	750	μA
C <sub>I</sub>	input capacitance		-	3.5	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 8.

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
t <sub>pd</sub>	propagation delay	nA to nY; see Fig. 7 [2]				
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	2.9	4.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.2	3.7	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.8	3.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.4	3.4	ns
C <sub>PD</sub>	power dissipation capacitance	per inverter; V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V [3]	-	25	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

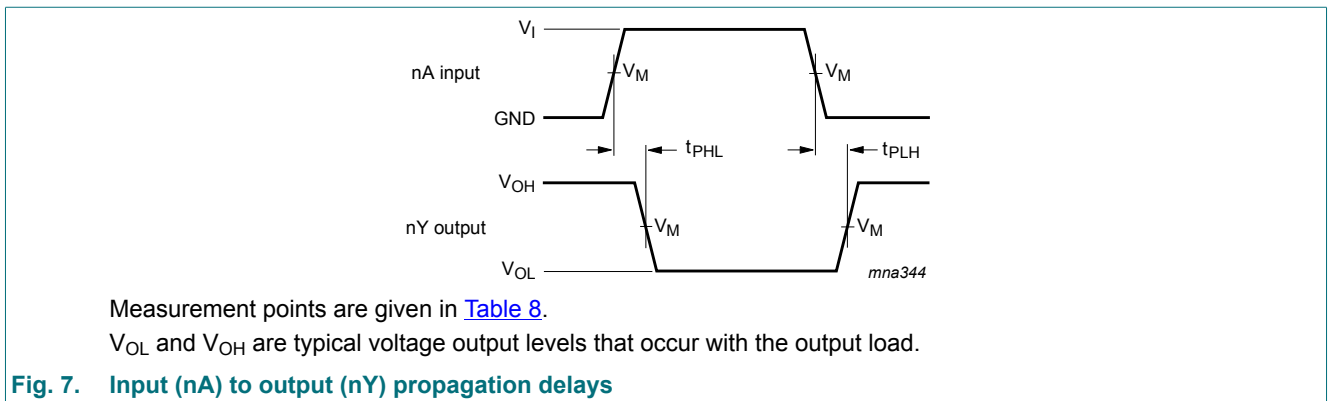
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

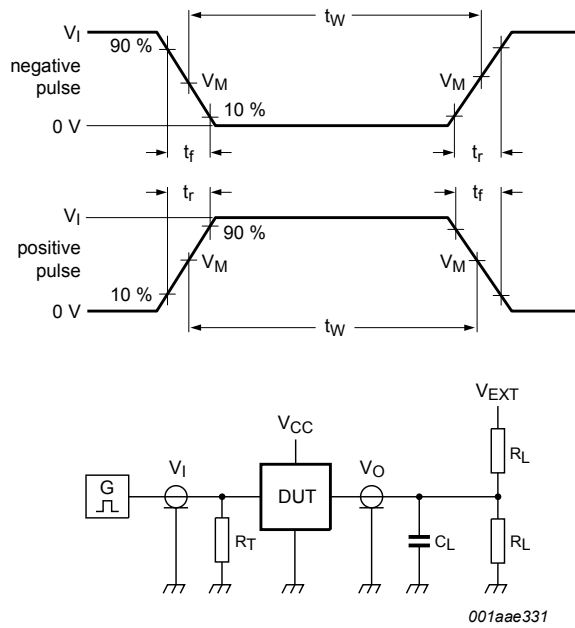
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs

### 10.1. Waveforms and test circuit



**Table 8. Measurement points**

Supply voltage	Input		Output
V <sub>CC</sub>	V <sub>I</sub>	V <sub>M</sub>	V <sub>M</sub>
1.65 V to 1.95 V	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>
2.3 V to 2.7 V	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

$V_{EXT}$  = Test voltage for switching times.

**Fig. 8. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open

## 11. Transfer characteristics

**Table 10. Transfer characteristics**

Voltages are referenced to GND (ground = 0 V); see [Fig. 9](#).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V <sub>T+</sub>	positive-going threshold voltage	V <sub>CC</sub> = 1.65 V	0.7	0.98	1.24	V
		V <sub>CC</sub> = 1.95 V	0.75	1.12	1.46	V
		V <sub>CC</sub> = 2.3 V	0.9	1.27	1.7	V
		V <sub>CC</sub> = 2.7 V	1.0	1.43	2.0	V
		V <sub>CC</sub> = 3.0 V [2]	1.1	1.56	2.0	V
		V <sub>CC</sub> = 3.6 V	1.1	1.81	2.0	V
V <sub>T-</sub>	negative-going threshold voltage	V <sub>CC</sub> = 1.65 V	0.41	0.64	0.9	V
		V <sub>CC</sub> = 1.95 V	0.49	0.76	1.1	V
		V <sub>CC</sub> = 2.3 V	0.6	0.90	1.3	V
		V <sub>CC</sub> = 2.7 V	0.7	1.06	1.4	V
		V <sub>CC</sub> = 3.0 V [2]	0.8	1.19	1.5	V
		V <sub>CC</sub> = 3.6 V	0.8	1.42	1.7	V
V <sub>H</sub>	hysteresis voltage	V <sub>CC</sub> = 1.65 V	0.25	0.34	0.62	V
		V <sub>CC</sub> = 1.95 V	0.25	0.36	0.62	V
		V <sub>CC</sub> = 2.3 V	0.3	0.36	1.0	V
		V <sub>CC</sub> = 2.7 V	0.3	0.38	1.1	V
		V <sub>CC</sub> = 3.0 V [2]	0.3	0.37	1.2	V
		V <sub>CC</sub> = 3.6 V	0.3	0.40	1.2	V

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

[2] The typical transfer characteristic is displayed in [Fig. 10](#).



11.1. Transfer characteristics waveforms

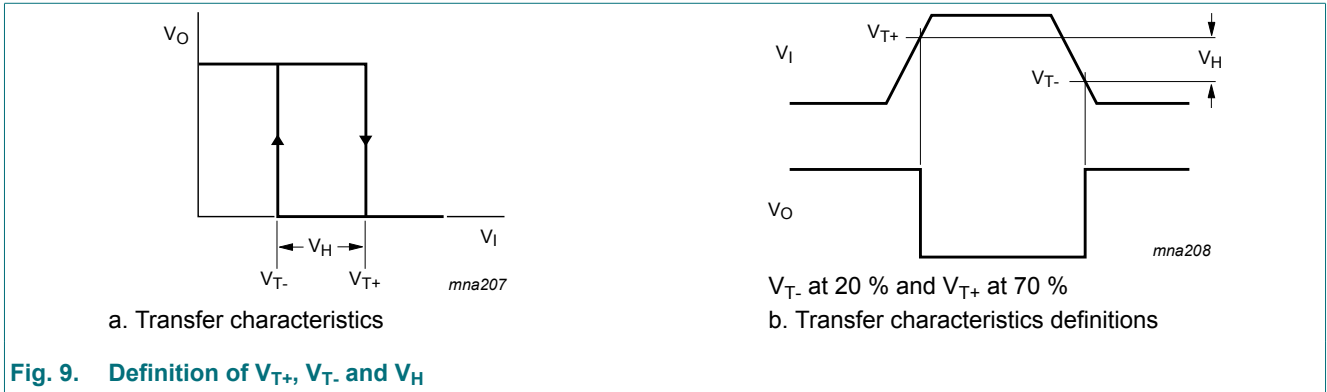
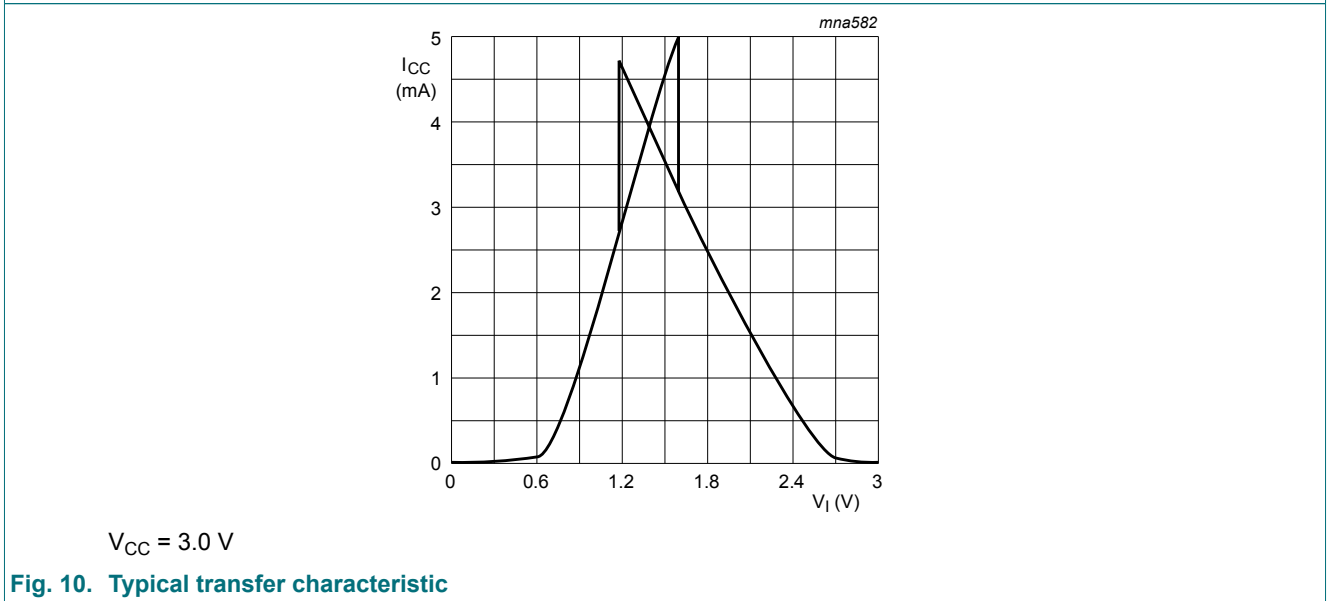
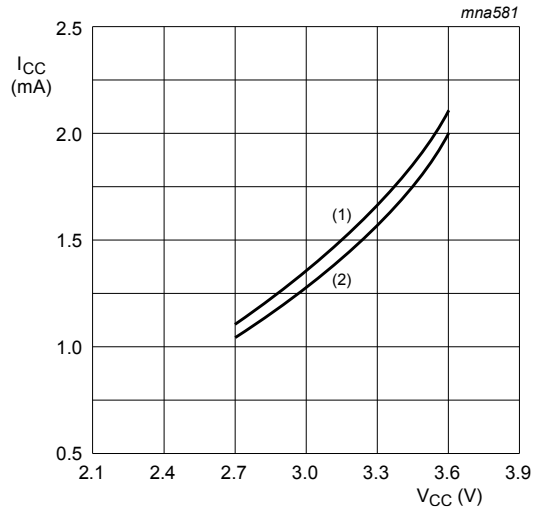


Fig. 9. Definition of  $V_{T+}$ ,  $V_{T-}$  and  $V_H$



## 12. Application information



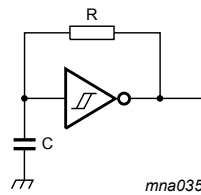
(1) Positive-going edge.

(2) Negative going-edge.

Linear change of  $V_I$  between 0.8 V to 2.0 V.

All values given are typical unless otherwise specified.

**Fig. 11. Average supply current as a function of supply voltage**



$$f = \frac{1}{T} \approx \frac{1}{0.8 \times RC} \text{ at } V_{CC} = 3.0 \text{ V.}$$

**Fig. 12. Relaxation oscillator**

### 13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

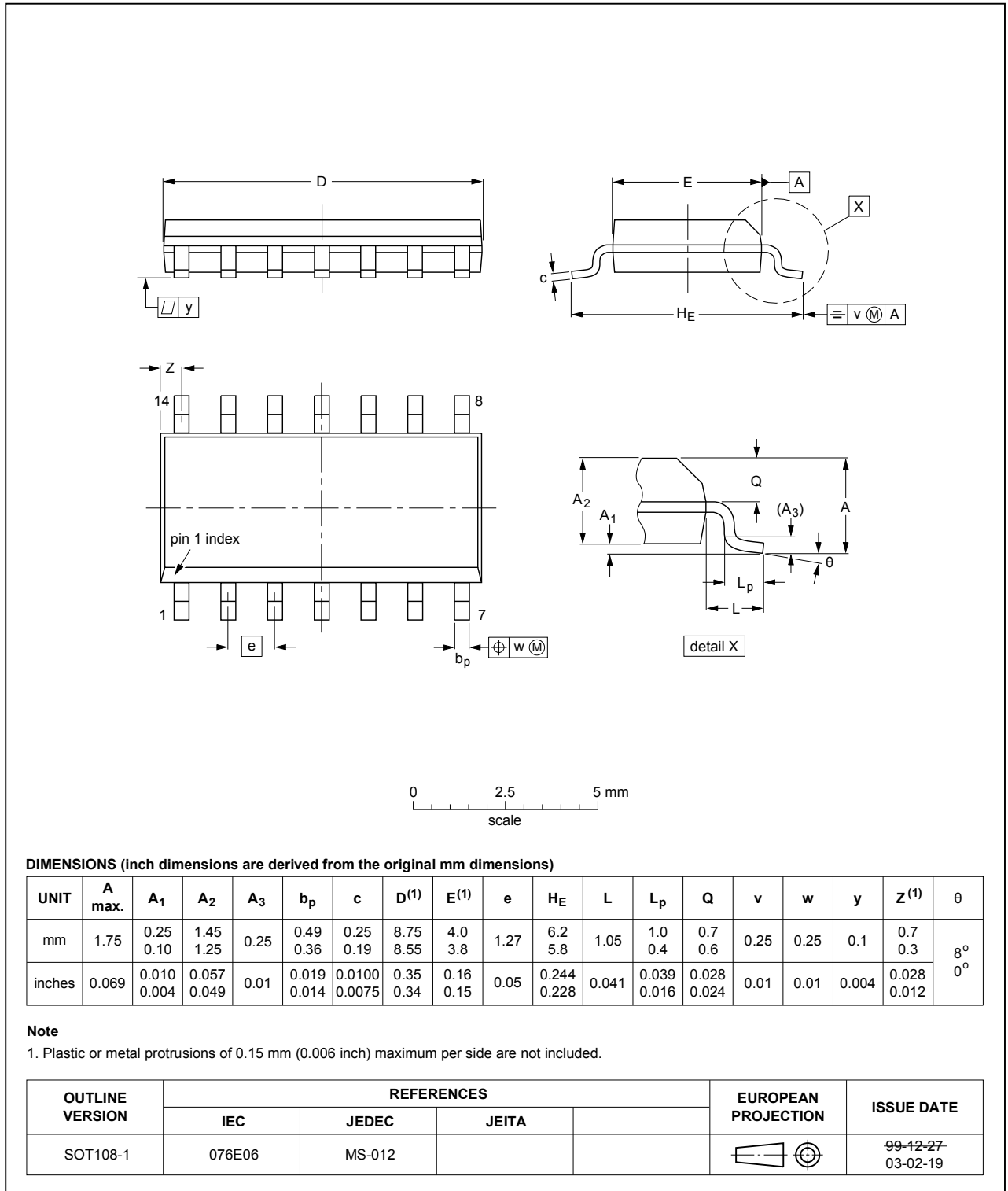
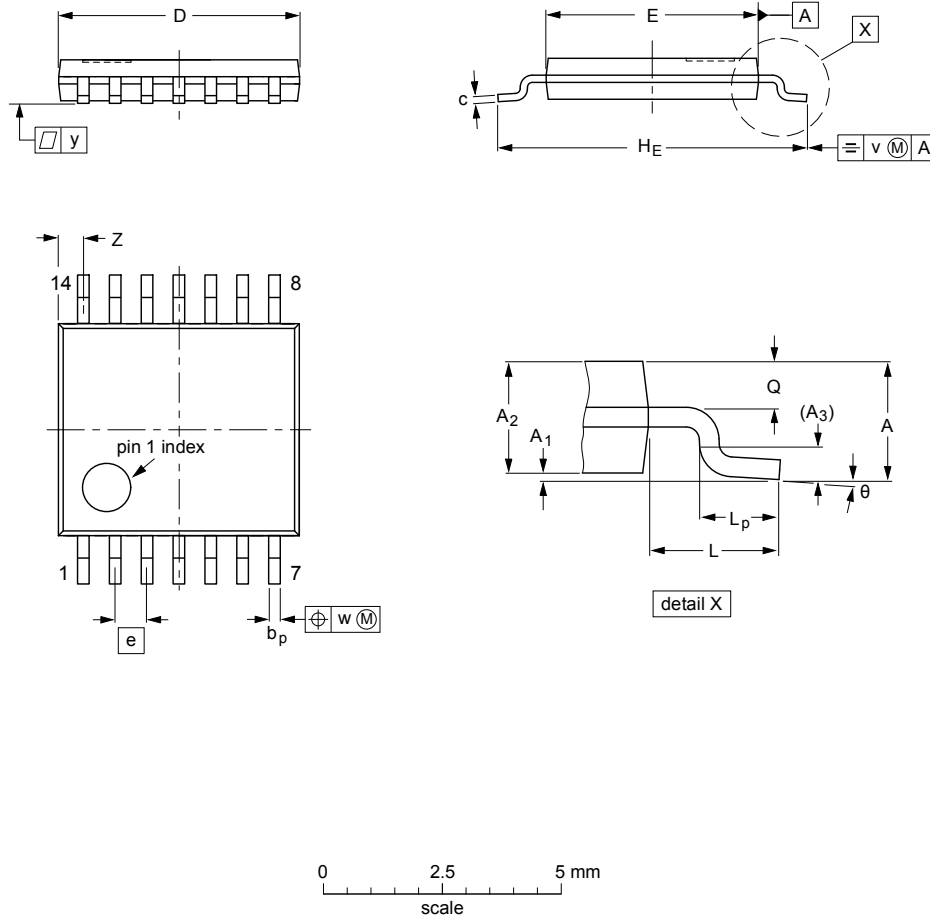


Fig. 13. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

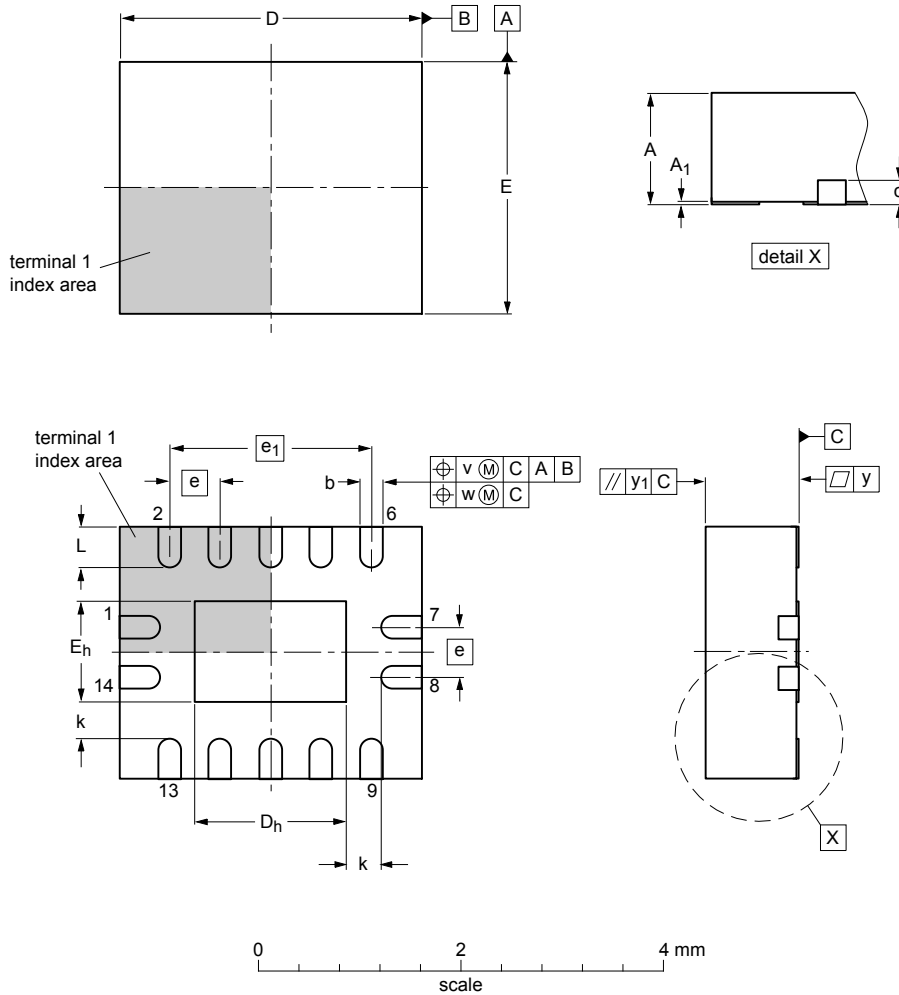
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				99-12-27 03-02-18

Fig. 14. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Dimensions (mm are the original dimensions)

Unit	A <sup>(1)</sup>	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	k	L	v	w	y	y <sub>1</sub>
max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				15-04-10 15-05-05

Fig. 15. Package outline SOT762-1 (DHVQFN14)

## 14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC14 v.4	20180814	Product data sheet	-	74ALVC14 v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74ALVC14 v.3	20050215	Product data sheet	-	74ALVC14 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet is redesigned to comply with the current presentation and information standard of Philips Semiconductors.</li> <li>General text updates.</li> </ul>			
74ALVC14 v.2	20030514	Product specification	-	74ALVC14 v.1
74ALVC14 v.1	20030203	Product specification	-	-

## 16. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 14 August 2018

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