74ALVCH16373

2.5 V/3.3 V 16-bit D-type transparent latch; 3-state

Rev. 7 — 30 January 2019

Product data sheet

1. General description

The 74ALVCH16373 is 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications.

Incorporates bus hold data inputs which eliminate the need for external pull-up or pull-down resistors to hold unused inputs.

One latch enable (LE) input and one output enable (\overline{OE}) are provided per 8-bit section.

The 74ALVCH16373 consists of 2 sections of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the nDn inputs enter the latches. In this condition the latches are transparent, therefore a latch output will change each time its corresponding D-input changes.

When LE is LOW, the latches store the information that was present at the nDn inputs at a set-up time preceding the LOW-to-HIGH transition of LE. When \overline{OE} is LOW, the contents of the eight latches are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standard JESD8-B
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- · Direct interface with TTL levels
- All data inputs have bus hold
- Output drive capability 50 Ω transmission lines at 85 °C
- Current drive ±24 mA at V_{CC} = 3.0 V

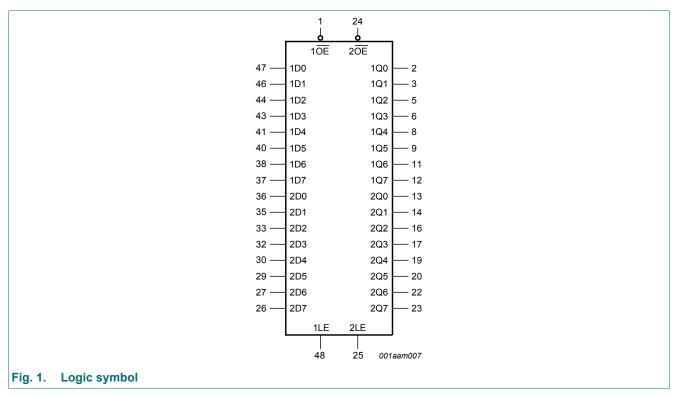
3. Ordering information

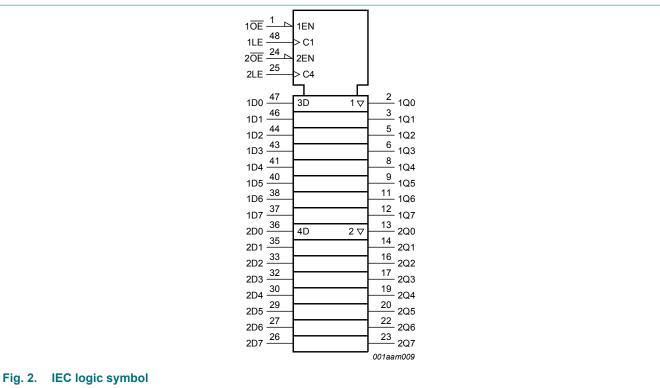
Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74ALVCH16373DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1



4. Functional diagram





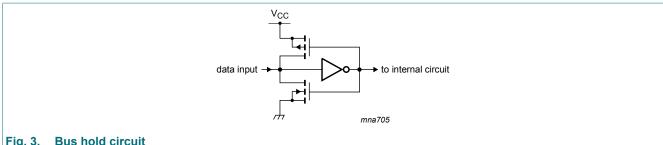
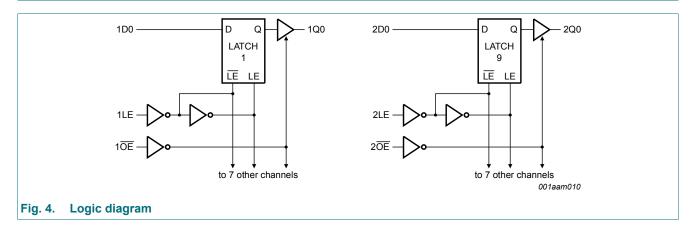
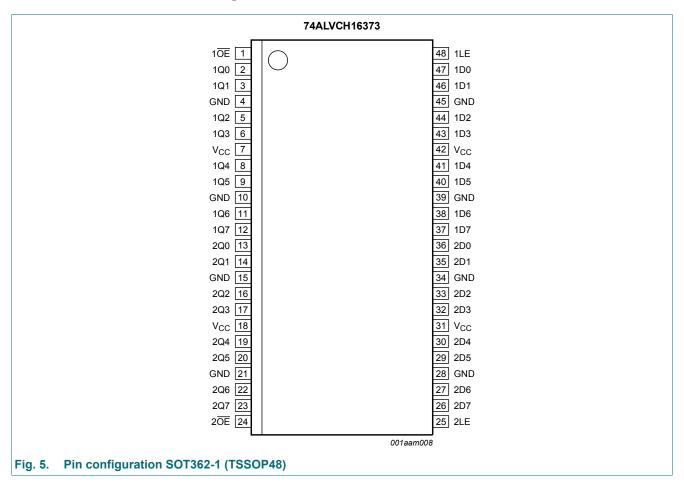


Fig. 3. **Bus hold circuit**



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
10E, 20E	1, 24	output enable input (active LOW)
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7	2, 3, 5, 6, 8, 9, 11, 12	data outputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7	13, 14, 16, 17, 19, 20, 22, 23	data outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V _{CC}	7, 18, 31, 42	positive supply voltage
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7	47, 46, 44, 43, 41, 40, 38, 37	data inputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7	36, 35, 33, 32, 30, 29, 27, 26	data inputs
1LE, 2LE	48, 25	latch enable input (active HIGH)

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH LE transition; L = LOW voltage level; I = LOW voltage level one set-up time prior to the LOW-to-HIGH LE transition; Z = high-impedance OFF-state.

Inputs			Internal latches	Outputs nQn	Operating mode	
nOE	nLE	nDn				
L	Н	L	L	L	enable and read register	
L	Н	Н	Н	Н	(transparent mode)	
L	L	I	L	L	latch and read register	
L	L	h	Н	Н	(hold mode)	
Н	L	I	L	Z	latch register and disable	
Н	L	h	Н	Z	outputs	

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
VI	input voltage	control inputs [1]	-0.5	+4.6	V
		data inputs [1]	-0.5	V _{CC} + 0.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0 V$	-	±50	mA
V _O	output voltage	[1]	-0.5	V _{CC} + 0.5	V
I _O	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±50	mA
I _{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$ [2]	-	600	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^[2] Above 55 $^{\circ}$ C the value of P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage	maximum speed performance				
		C _L = 30 pF	2.3	-	2.7	V
		C _L = 50 pF	3.0	-	3.6	V
		low voltage applications	1.2	-	3.6	V
VI	input voltage	data inputs	0	-	V _{CC}	V
		control inputs	0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.3 V to 3.0 V	0	-	20	ns/V
		V _{CC} = 3.0 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T _{amb} = -4	40 °C to +85 °C		·			
V _{IH}	HIGH-level input	V _{CC} = 1.2 V	V _{CC}	-	-	V
	voltage	V _{CC} = 1.8 V	0.7V _{CC}	0.9	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	1.5	-	V
V _{IL}	LOW-level input	V _{CC} = 1.2 V	-	-	0	V
	voltage	V _{CC} = 1.8 V	-	0.9	0.2V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	1.5	0.8	V
V _{OH}	HIGH-level output	$V_I = V_{IH}$ or V_{IL}				
	voltage	I_{O} = -100 μ A; V_{CC} = 1.8 V to 3.6 V	V _{CC} - 0.2	V _{CC}	-	V
		I_{O} = -6 mA; V_{CC} = 1.8 V	V _{CC} - 0.4	V _{CC} - 0.1	-	V
		I_{O} = -6 mA; V_{CC} = 2.3 V	V _{CC} - 0.3	V _{CC} - 0.08	-	V
		I _O = -12 mA; V _{CC} = 2.3 V	V _{CC} - 0.5	V _{CC} - 0.17	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	V _{CC} - 0.5	V _{CC} - 0.14	-	V
		I_{O} = -18 mA; V_{CC} = 2.3 V	V _{CC} - 0.6	V _{CC} - 0.26	-	V
		I_{O} = -24 mA; V_{CC} = 3.0 V	V _{CC} - 1.0	V _{CC} - 0.28	-	V
V _{OL}	LOW-level output	$V_I = V_{IH}$ or V_{IL}				
	voltage	I_{O} = 100 μ A; V_{CC} = 1.8 V to 3.6 V	-	0	0.20	V
		I _O = 6 mA; V _{CC} = 1.8 V	-	0.09	0.30	V
		I _O = 6 mA; V _{CC} = 2.3 V	-	0.07	0.20	V
		I _O = 12 mA; V _{CC} = 2.3 V	-	0.15	0.40	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	0.14	0.40	V
		I _O = 18 mA; V _{CC} = 2.3 V	-	0.23	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	0.27	0.55	V

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
l _l	input leakage current	V _{CC} = 1.8 V to 3.6 V					
		control input; V _I = 5.5 V or GND		-	0.1	5	μA
		data input; V _I = V _{CC} or GND		-	0.1	5	μA
l _{OZ}	OFF-state output	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND					
	current	V _{CC} = 1.8 V to 2.7 V		-	0.1	5	μA
		V _{CC} = 2.7 V to 3.6 V		-	0.1	10	μA
I _{LIZ}	OFF-state input	V _I = V _{CC} or GND					
	leakage current	V _{CC} = 1.8 V to 2.7 V		-	0.1	10	μA
		V _{CC} = 3.6 V		-	0.1	15	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A;					
		V _{CC} = 1.8 V to 2.7 V		-	0.2	40	μA
		V _{CC} = 2.7 V to 3.6 V		-	0.2	40	μΑ
ΔI _{CC}	additional supply	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A}; V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$,				
	current	per control input		-	5	500	μΑ
		per data I/O input		-	150	750	μΑ
I _{BHL}	bus hold LOW current	$V_{CC} = 2.3 \text{ V}; V_I = 0.7 \text{ V}$	2]	45	-	-	μΑ
		$V_{CC} = 3.0 \text{ V}; V_I = 0.8 \text{ V}$	2]	75	150	-	μΑ
I _{BHH}	bus hold HIGH current	$V_{CC} = 2.3 \text{ V}; V_I = 1.7 \text{ V}$	2]	-45	-	-	μΑ
		$V_{CC} = 3.0 \text{ V}; V_I = 2.0 \text{ V}$	2]	-75	-175	-	μΑ
I _{BHLO}	bus hold LOW	$V_{CC} = 2.7 \text{ V}$	2]	300	-	-	μΑ
	overdrive current	V _{CC} = 3.6 V	2]	450	-	-	μΑ
I _{внно}	bus hold HIGH	$V_{CC} = 2.7 \text{ V}$	2]	-300	-	-	μΑ
	overdrive current	V _{CC} = 3.6 V	2]	-450	-	-	μΑ
Cı	input capacitance			-	5.0	-	pF

 ^[1] All typical values are measured at T_{amb} = 25 °C.
 [2] Valid for data inputs of bus hold parts only.

10. Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
T _{amb} = -	40 °C to +85 °C						
t _{pd}	propagation delay	nDn to nQn; see Fig. 6	[2]				
		V _{CC} = 1.2 V		-	8.8	-	ns
		V _{CC} = 1.8 V		1.5	3.2	5.7	ns
		V _{CC} = 2.3 V to 2.7 V	[3]	1.0	2.1	3.9	ns
		V _{CC} = 2.7 V		1.0	2.3	3.7	ns
		V _{CC} = 3.0 V to 3.6 V	[4]	1.0	2.1	3.3	ns
		nLE to nQn; see Fig. 7	[2]				
		V _{CC} = 1.2 V		-	7.4	-	ns
		V _{CC} = 1.8 V		1.5	3.4	5.9	ns
		V _{CC} = 2.3 V to 2.7 V	[3]	1.0	2.2	3.9	ns
		V _{CC} = 2.7 V		1.0	2.2	3.5	ns
		V _{CC} = 3.0 V to 3.6 V	[4]	1.0	2.2	3.2	ns
t _{en}	enable time	nOE to nQn; see Fig. 8	[5]				
		V _{CC} = 1.2 V		-	8.9	-	ns
		V _{CC} = 1.8 V		1.5	4.0	7.3	ns
		V _{CC} = 2.3 V to 2.7 V	[3]	1.0	2.6	5.2	ns
		V _{CC} = 2.7 V		1.0	2.9	4.9	ns
		V _{CC} = 3.0 V to 3.6 V	[4]	1.0	2.3	4.2	ns
t _{dis}	disable time	nOE to nQn; see Fig. 8	[6]				
		V _{CC} = 1.2 V		-	8.9	-	ns
		V _{CC} = 1.8 V		1.5	3.2	5.6	ns
		V _{CC} = 2.3 V to 2.7 V	[3]	1.0	2.2	4.1	ns
		V _{CC} = 2.7 V		1.0	3.1	4.7	ns
		V _{CC} = 3.0 V to 3.6 V	[4]	1.0	2.8	4.1	ns
t _W	pulse width	nLE HIGH; see Fig. 7					
		V _{CC} = 1.8 V		3.5	1.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	[3]	3.0	1.0	-	ns
		V _{CC} = 2.7 V		3.0	1.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	[4]	2.5	1.0	-	ns
t _{su}	set-up time	nDn to nLE; see Fig. 9					
		V _{CC} = 1.8 V		1.0	-0.1	-	ns
		V _{CC} = 2.3 V to 2.7 V	[3]	1.0	-0.1	-	ns
		V _{CC} = 2.7 V		1.0	-0.1	-	ns
		V _{CC} = 3.0 V to 3.6 V	[4]	1.0	0.0	-	ns

Symbol	Parameter	Conditions	Conditions			Max	Unit
t _h	hold time	nDn to nLE; see Fig. 9					
		V _{CC} = 1.8 V		1.2	0.1	-	ns
		V _{CC} = 2.3 V to 2.7 V	[3]	1.5	0.2	-	ns
		V _{CC} = 2.7 V		1.5	0.4	-	ns
		V _{CC} = 3.0 V to 3.6 V	[4]	1.2	0.2	-	ns
C _{PD}	power dissipation	per flip-flop; V_I = GND to V_{CC}	[7]				
	capacitance	outputs enabled		-	16	-	pF
		outputs disabled		-	10	-	pF

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] Typical values are measured at V_{CC} = 2.5 V.
- [4] Typical values are measured at V_{CC} = 3.3 V.
- [5] t_{en} is the same as t_{PZL} and t_{PZH} .
- 6] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
- [7] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz;

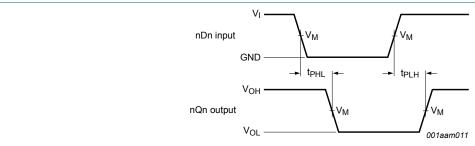
C₁ = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_0)$ = sum of the outputs.

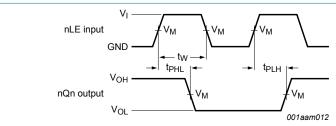
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 6. Propagation delay, input (nDn) to data output (nQn)



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 7. Propagation delay, latch enable input (nLE) to data output (nQn), and pulse width

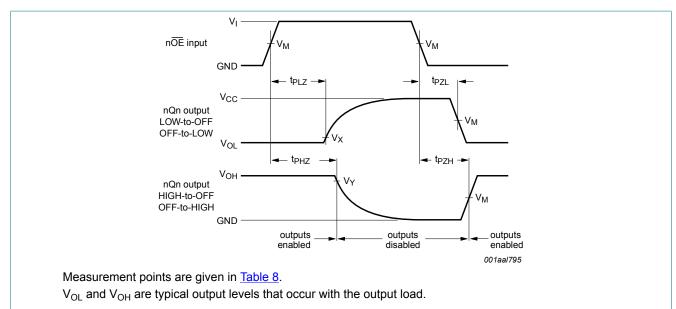


Fig. 8. 3-state enable and disable times

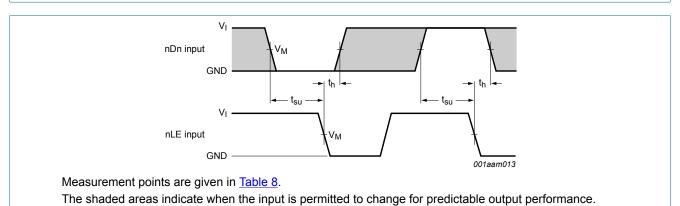
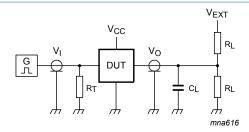


Fig. 9. Data setup and hold times for input (nDn) to input (nLE)

Table 8. Measurement points

Supply voltage	nput Output				
V _{CC}	V _I	V _M	V _M	V _X	V _Y
2.3 V to 2.7 V and < 2.3 V	V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig. 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V _{EXT}		
V _{CC}	VI	t _r , t _f	CL	R_L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
2.3 V to 2.7 V and < 2.3 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V _{CC}	GND
2.7 V	2.7 V	2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND
3.0 V to 3.6 V	2.7 V	2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND

11. Package outline

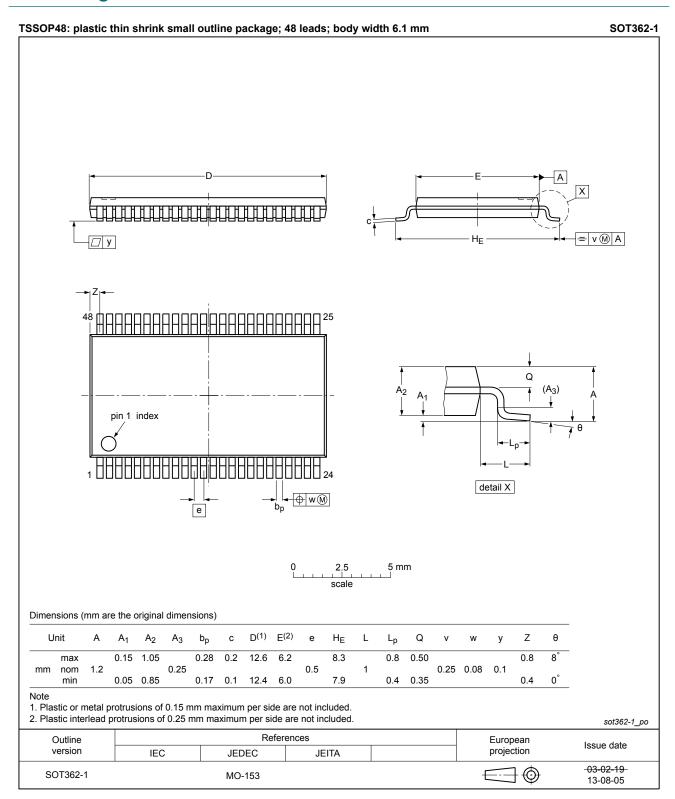


Fig. 11. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description			
CMOS	nplementary Metal-Oxide Semiconductor			
DUT	Device Under Test			
TTL	Transistor-Transistor Logic			

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74ALVCH16373 v.7	20190130	Product data sheet	-	74ALVCH16373 v.6	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74ALVCH16373DL (SOT370-1) removed. Package outline drawing SOT362-1 (TSSOP48) updated. 				
74ALVCH16373 v.6	20120710	Product data sheet	-	74ALVCH16373 v.5	
Modifications:	<u>Table 8</u> corrected (errata).				
74ALVCH16373 v.5	20111117	Product data sheet	-	74ALVCH16373 v.4	
Modifications:	 Legal pages 	updated.	,		
74ALVCH16373 v.4	20100531	Product data sheet	-	74ALVCH16373 v.3	
74ALVCH16373 v.3	19990920	Product specification	-	74ALVCH16373 v.2	
74ALVCH16373 v.2	19980629	Product specification	-	74ALVCH16373 v.1	
74ALVCH16373 v.1	19970321	Product specification	-	-	

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal

2.5 V/3.3 V 16-bit D-type transparent latch; 3-state

injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by sustained.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

74ALVCH16373

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2019. All rights reserved

Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Functional diagram	2
5. Pinning information	4
5.1. Pinning	4
5.2. Pin description	4
6. Functional description	5
7. Limiting values	5
8. Recommended operating conditions	6
9. Static characteristics	6
10. Dynamic characteristics	ε
10.1. Waveforms and test circuit	g
11. Package outline	12
12. Abbreviations	13
13. Revision history	13
14. Legal information	14

For more information, please visit: http://www.nexperia.com For sales office addresses, please send an email to: salesaddresses@nexperia.com Date of release: 30 January 2019

[©] Nexperia B.V. 2019. All rights reserved

单击下面可查看定价,库存,交付和生命周期等信息

>>Nexperia(安世)